



1. Description

1.1. Project

Project Name	reverse_mono_6ks
Board Name	custom
Generated with:	STM32CubeMX 6.12.0
Date	08/06/2024

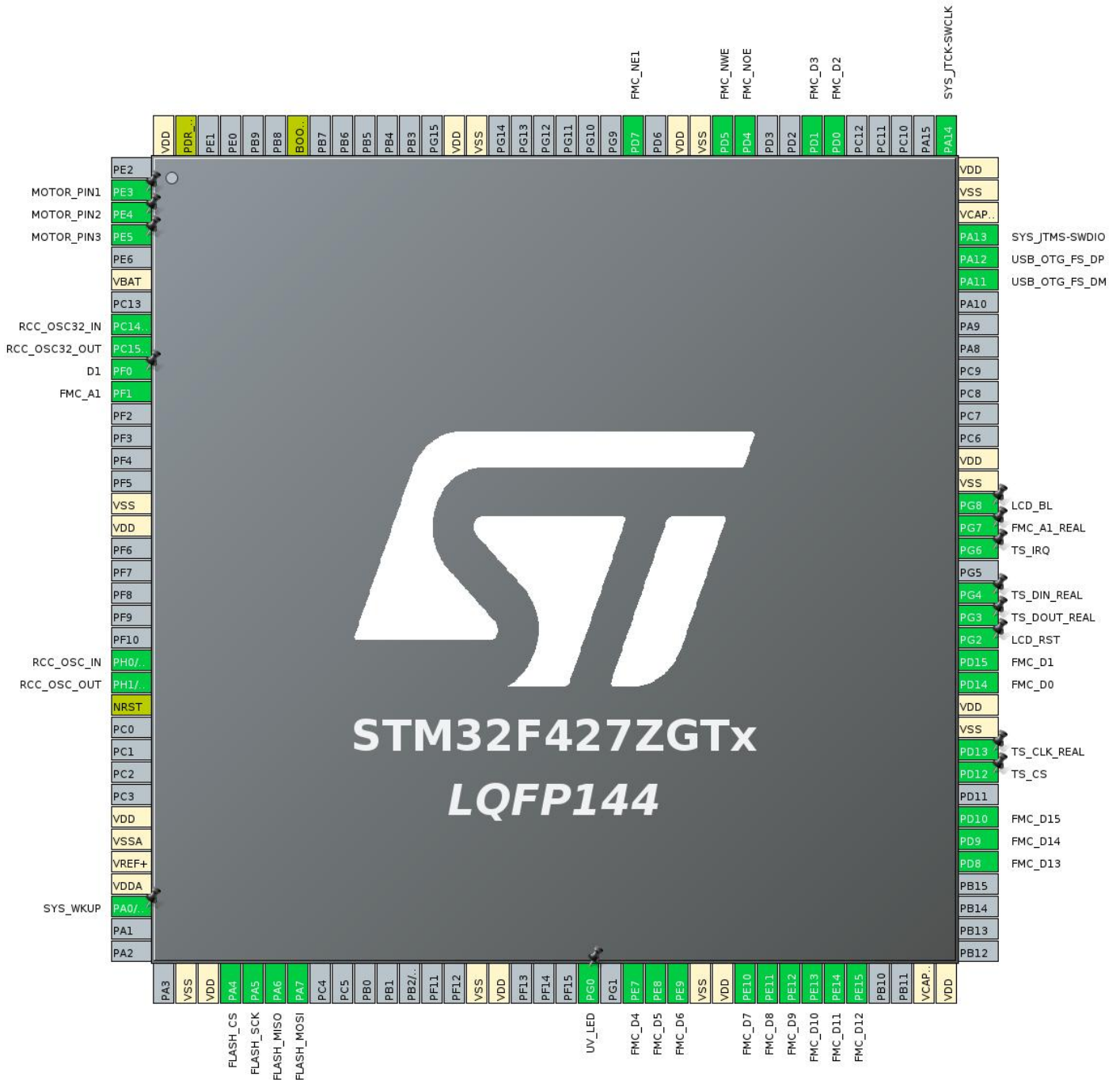
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F427/437
MCU name	STM32F427ZGTx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M4
---------	---------------

2. Pinout Configuration



3. Pins Configuration

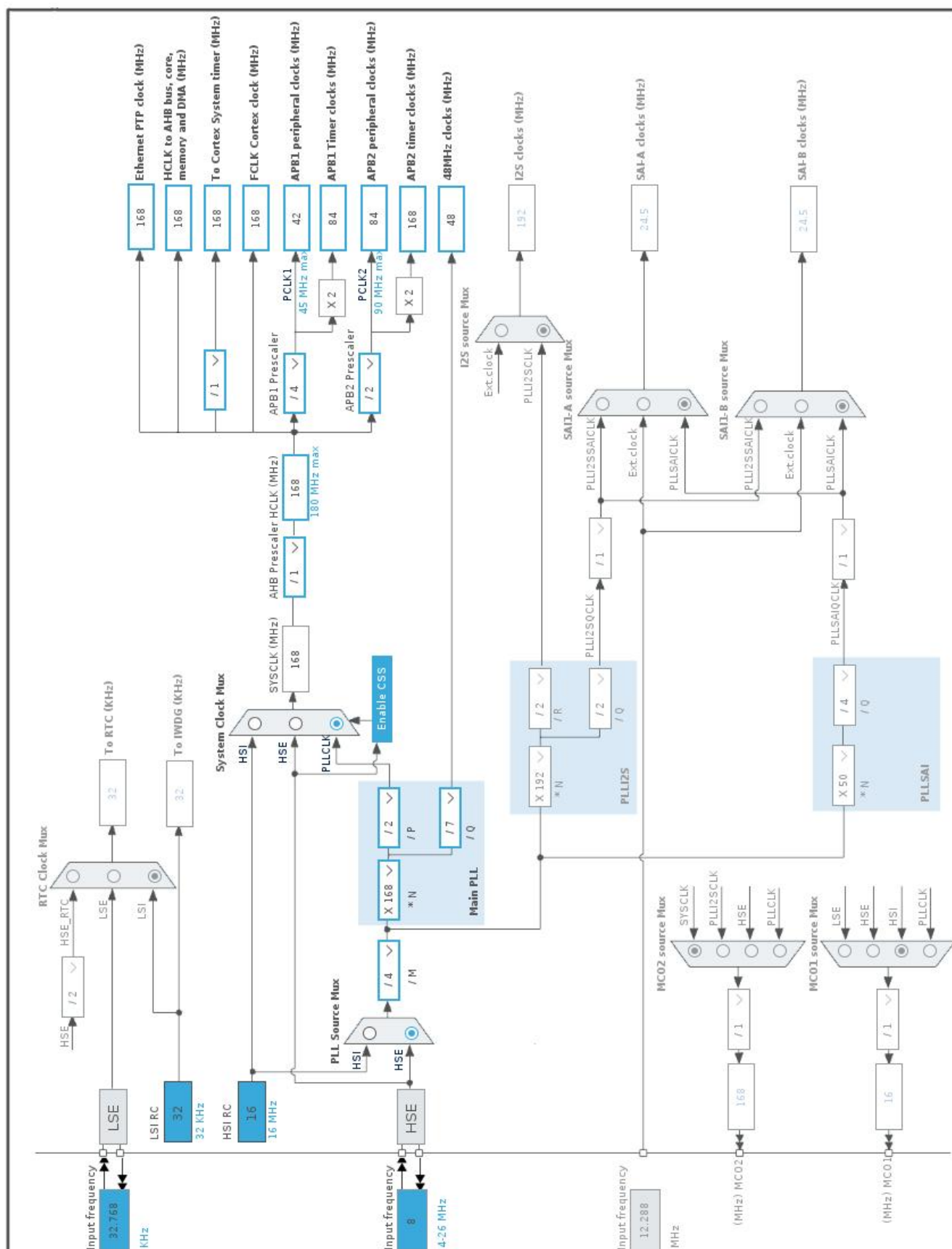
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
2	PE3 *	I/O	GPIO_Output	MOTOR_PIN1
3	PE4 *	I/O	GPIO_Output	MOTOR_PIN2
4	PE5 *	I/O	GPIO_Output	MOTOR_PIN3
6	VBAT	Power		
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF0 *	I/O	GPIO_Output	D1
11	PF1	I/O	FMC_A1	
16	VSS	Power		
17	VDD	Power		
23	PH0/OSC_IN	I/O	RCC_OSC_IN	
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	SYS_WKUP	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	SPI1_NSS	FLASH_CS
41	PA5	I/O	SPI1_SCK	FLASH_SCK
42	PA6	I/O	SPI1_MISO	FLASH_MISO
43	PA7	I/O	SPI1_MOSI	FLASH_MOSI
51	VSS	Power		
52	VDD	Power		
56	PG0 *	I/O	GPIO_Output	UV_LED
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	
66	PE13	I/O	FMC_D10	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
71	VCAP_1	Power		
72	VDD	Power		
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
81	PD12 *	I/O	GPIO_Output	TS_CS
82	PD13 *	I/O	GPIO_Output	TS_CLK_REAL
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
87	PG2 *	I/O	GPIO_Output	LCD_RST
88	PG3 *	I/O	GPIO_Output	TS_DOUT_REAL
89	PG4 *	I/O	GPIO_Input	TS_DIN_REAL
91	PG6	I/O	GPIO_EXTI6	TS_IRQ
92	PG7 *	I/O	GPIO_Output	FMC_A1_REAL
93	PG8 *	I/O	GPIO_Output	LCD_BL
94	VSS	Power		
95	VDD	Power		
103	PA11	I/O	USB_OTG_FS_DM	
104	PA12	I/O	USB_OTG_FS_DP	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
118	PD4	I/O	FMC_NOE	
119	PD5	I/O	FMC_NWE	
120	VSS	Power		
121	VDD	Power		
123	PD7	I/O	FMC_NE1	
130	VSS	Power		
131	VDD	Power		
138	BOOT0	Boot		
143	PDR_ON	Reset		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F427/437
MCU	STM32F427ZGTx
Datasheet	DS9405_Rev9

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

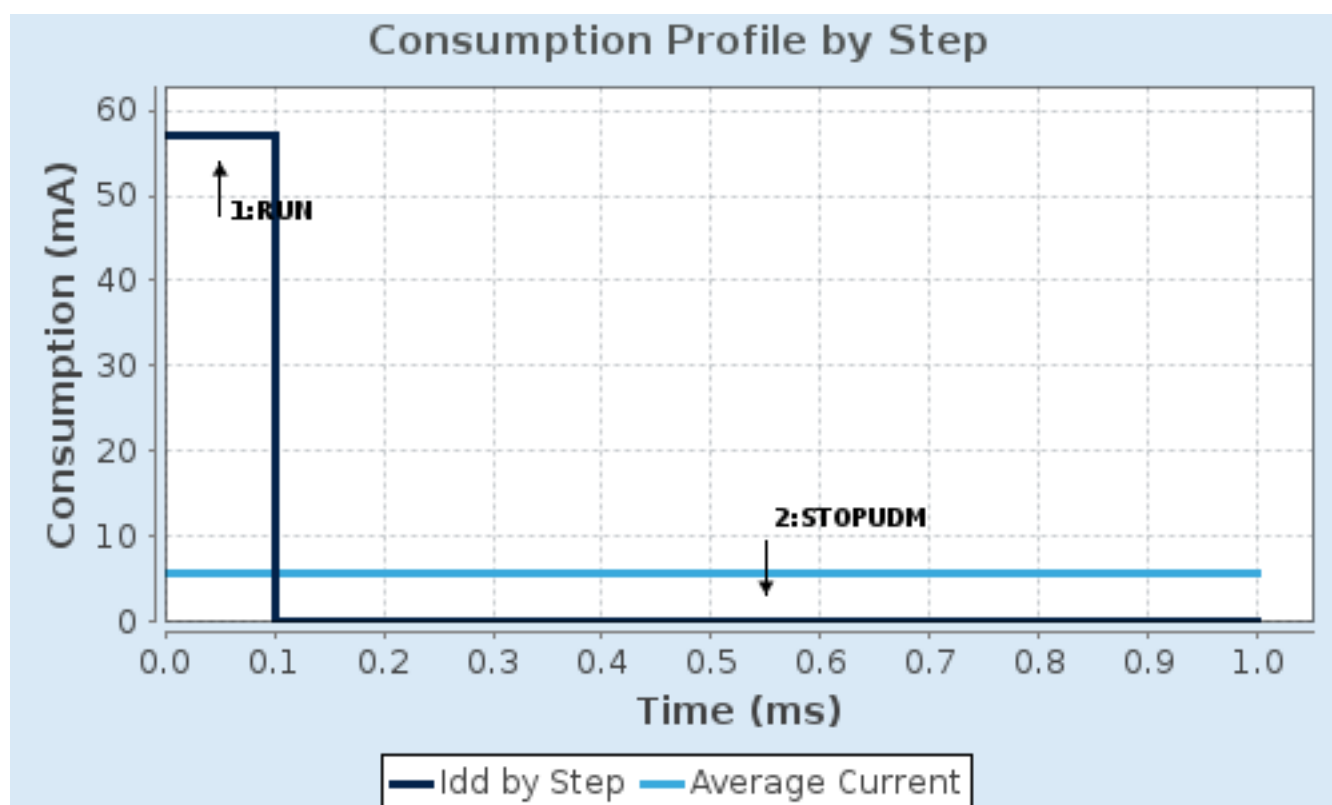
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	57 mA	100 μ A
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	97.48	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	5.79 mA
Battery Life	24 days, 10 hours	Average DMIPS	225.0 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	reverse_mono_6ks
Project Folder	/home/goran/Projects/reverse_mono_6ks
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.0
Application Structure	Basic
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x2000
Minimum Stack Size	0x2000

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_DMA_Init	DMA
4	MX_RNG_Init	RNG
5	MX_FMC_Init	FMC
6	MX_SPI1_Init	SPI1
7	MX_USB_OTG_FS_HCD_Init	USB_OTG_FS
8	MX_DMA2D_Init	DMA2D

3. Peripherals and Middlewares Configuration

3.1. DMA2D

mode: Activated

3.1.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	RGB565 *
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	RGB565
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0

3.2. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: LCD Interface

LCD Register Select: A1

Data: 16 bits

3.2.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	LCD Interface
Bank	Bank 1 NOR/PSRAM 1
Write operation	Enabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	6 *
Data setup time in HCLK clock cycles	6 *
Bus turn around time in HCLK clock cycles	0 *

3.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

3.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	8 *
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

3.4. RNG

mode: Activated

3.5. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

3.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	42.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
-----------------	----------

NSS Signal Type

Output Hardware

3.6. SYS

Debug: Serial Wire
mode: System Wake-Up
Timebase Source: SysTick

3.7. USB_OTG_FS

Mode: Host_Only

3.7.1. Parameter Settings:

Speed	Host Full Speed 12MBit/s
Signal start of frame	Disabled

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FMC	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA4	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	FLASH_CS
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	FLASH_SCK
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	FLASH_MISO
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	FLASH_MOSI

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SYS	PA0/WKUP	SYS_WKUP	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_PIN1
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_PIN2
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_PIN3
	PF0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D1
	PG0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	UV_LED
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TS_CS
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TS_CLK_REAL
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RST
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TS_DOUT_REAL
	PG4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	TS_DIN_REAL
	PG6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	TS_IRQ
	PG7	GPIO_Output	Output Push Pull	Pull-up *	Very High *	FMC_A1_REAL
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_BL

4.2. DMA configuration

DMA request	Stream	Direction	Priority
MENTOMEM	DMA2_Stream0	Memory To Memory	High *

MENTOMEM: DMA2_Stream0 DMA request Settings:

Mode: Normal
Use fifo: **Enable ***
FIFO Threshold: Full
Src Memory Increment: **Enable ***
Dst Memory Increment: **Enable ***
Src Memory Data Width: Byte
Dst Memory Data Width: Byte
Src Memory Burst Size: Single
Dst Memory Burst Size: Single

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line[9:5] interrupts	true	0	0
DMA2 stream0 global interrupt	true	0	0
HASH and RNG global interrupts	true	0	0
DMA2D global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
SPI1 global interrupt	unused		
USB On The Go FS global interrupt	unused		
FPU global interrupt	unused		

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line[9:5] interrupts	false	true	true
DMA2 stream0 global interrupt	true	true	true
HASH and RNG global interrupts	false	true	true
DMA2D global interrupt	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA ✓			FMC ✓	DMA2D ✓	RNG ✓	
GPIO ✓			SPI1 ✓			
NVIC ✓			USB_FS ✓			
RCC ✓						
SYS ✓						

6. Docs & Resources

Type	Link
------	------