CS303 Logic & Digital Systems Design
Term Project

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1 Overview

In this project, a sequential circuit for an one-sided telephone conversation is designed and this design is implemented using Verilog HDL. With this circuit the caller can initiate a conversation with the callee and send characters to the callee. The design reveals the sent characters and the cost of the conversation as the output. The circuit contains sequential and combinational parts.

The sequential circuit is used to:

- define the state transitions
- control the registers
- control the 4 counters that are used to observe the clock cycles
- display the outputs

The combinational part is used to define the next state definitions. In this project, 6 states are used, each of these states are represented with 3 bits. These states are:

- IDLE: IDLE state is assigned 000 (0). This is the starting state. Whenever reset is 1, the current state transitions into IDLE state. When the circuit is in REJECTED state, after 10 clock cycles, current state transitions into IDLE state. When the circuit is in COST state, after 5 clock cycles, current state transitions into IDLE state. In the IDLE state, when the caller starts a call by assigning startCall 1, the state transitions into RINGING state.
- RINGING: RINGING state is assigned 001 (1). When the circuit is in IDLE state, and startCall becomes 1, the current state transitions into RINGING state. The circuit can stay in this state for 10 clock cycles,

after that current state becomes BUSY. If callee rejects the call by making endCall 1, the circuit transitions into REJECTED state. If the callee accepts the call by making answerCall 1, it transitions into CALL state.

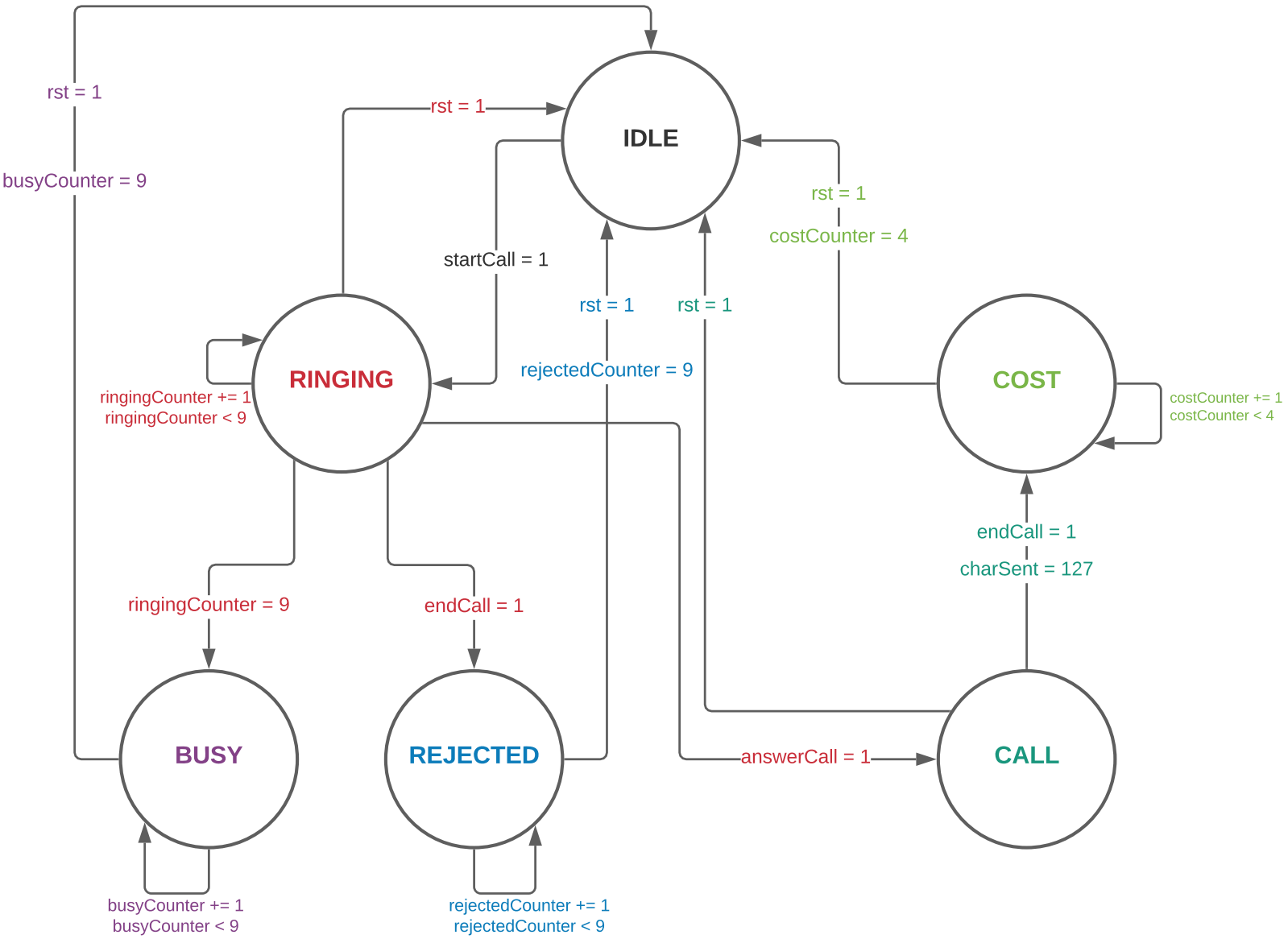
- REJECTED: REJECTED state is assigned 010 (2). When the circuit is in RINGING state and callee rejects the call by assigning endCall 1, the state becomes REJECTED. The circuit can stay in this state for 10 clock cyles, after that current state becomes IDLE.

- BUSY: BUSY state is assigned 011 (3). When the circuit is in RINGING state and callee does not respond for 10 clock cycles, the state becomes BUSY. The circuit can stay in this state for 10 clock cyles, after that current state becomes IDLE.

- CALL: CALL state is assinged 100 (4). When the circuit is in RINGING state and the callee accepts the call within the first 10 clock cycles by making answerCall 1, the state transitions into CALL state. The caller can send characters to callee with charSent and by assigning sendChar 1. The circuit stays in this state as long as the caller ends the call by sending 127 with the charSent or callee ends the call by assigning endCall 1. After that, state transitions into COST state to display the total cost of the conversation.

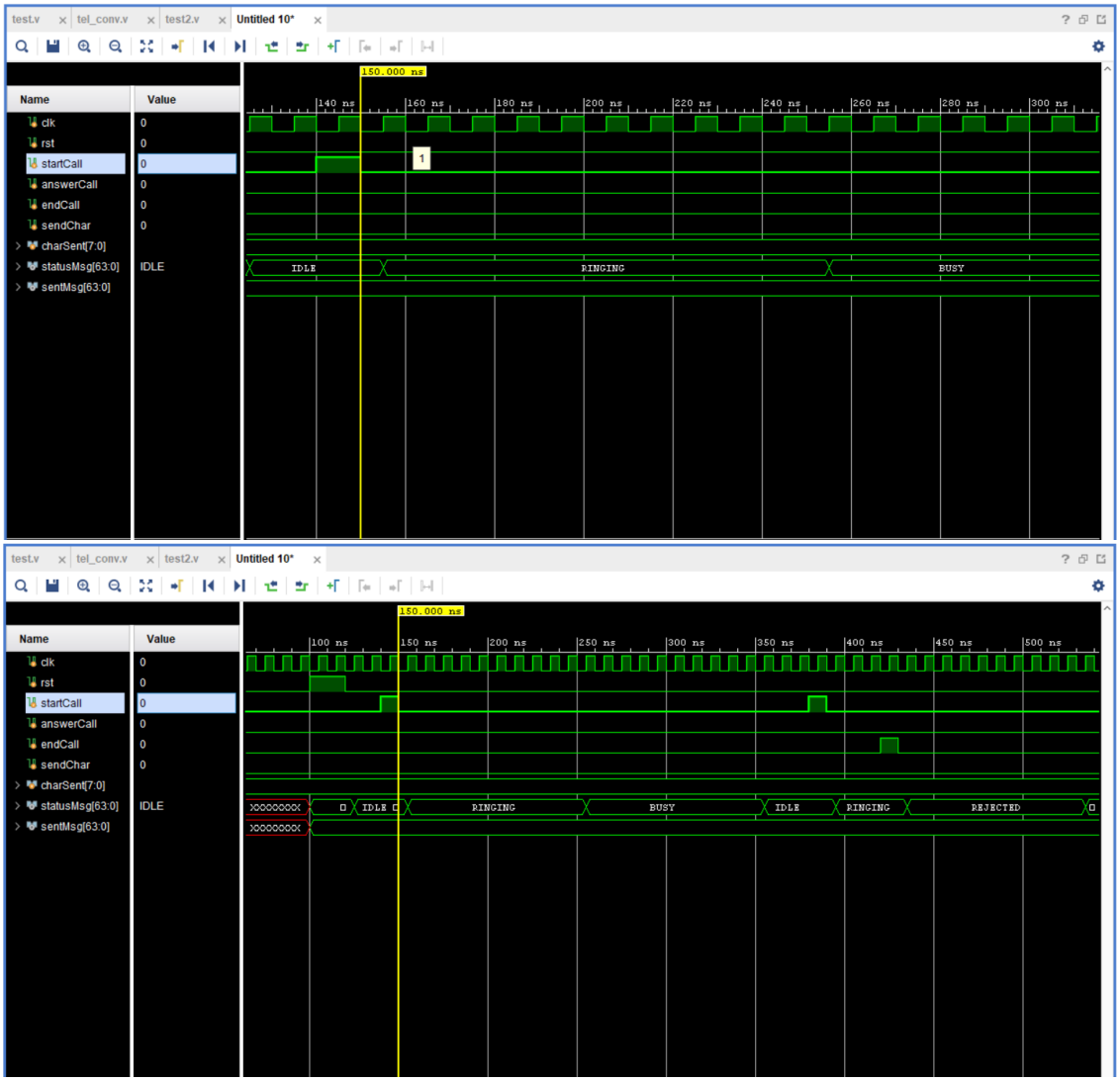
- COST: COST state is assigned 101 (5). When the conversation ends, current state transitions into the COST state. COST state displays the total cost of the conversation for 5 clock cycles and then transitions into the IDLE state.

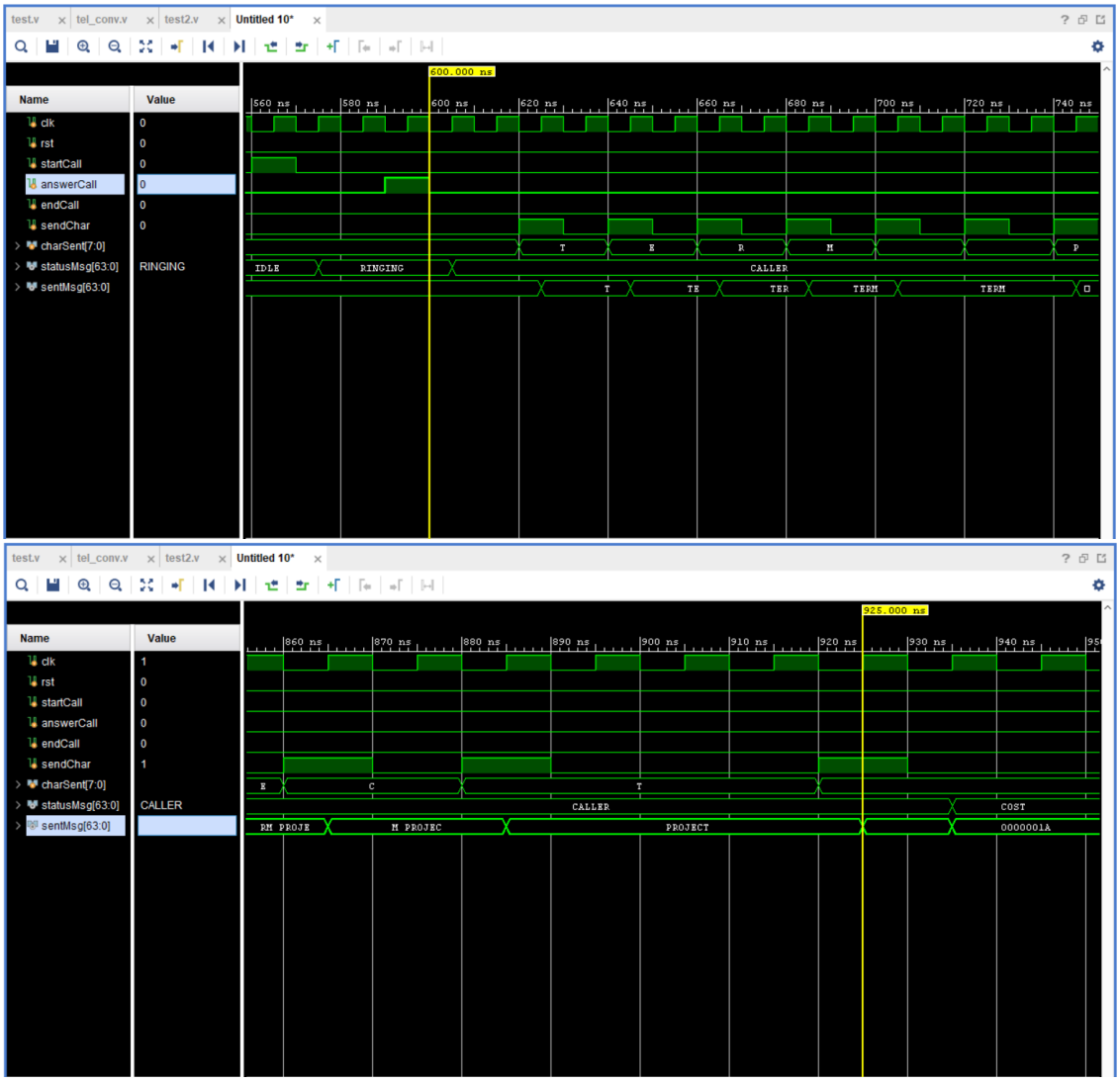
In the next page, the state diagram can be seen:

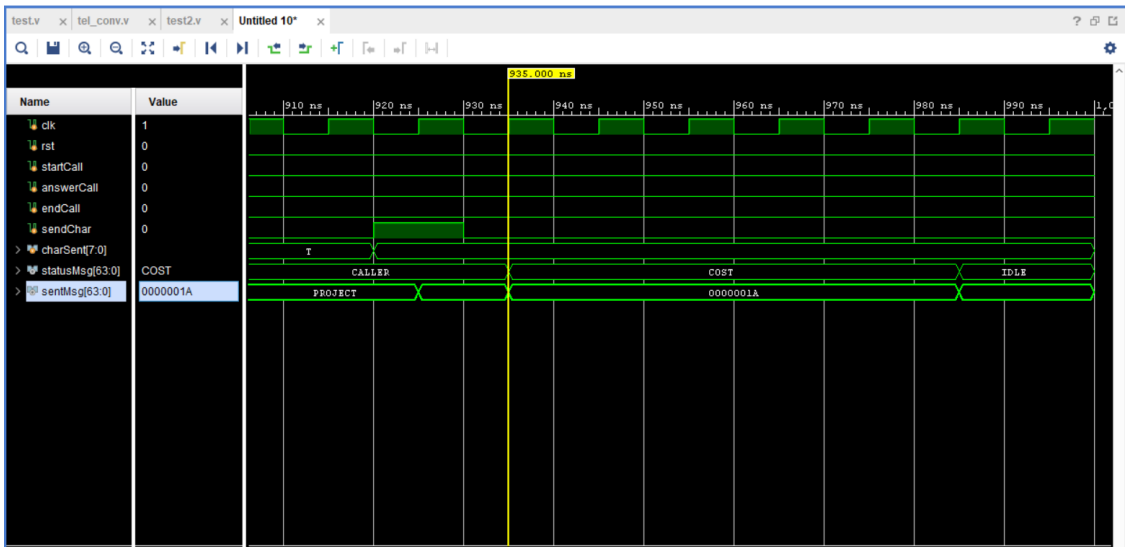

IDLE
RINGING
COST
BUSY
REJECTED
CALL
rst = 1
busyCounter = 9
rst = 1
startCall = 1
rst = 1
costCounter = 4
rst = 1
rst = 1
rejectedCounter = 9
ringingCounter += 1
ringingCounter < 9
costCounter += 1
costCounter < 4
endCall = 1
charSent = 127
ringingCounter = 9
endCall = 1
answerCall = 1
busyCounter += 1
busyCounter < 9
rejectedCounter += 1
rejectedCounter < 9

2 Simulation Results

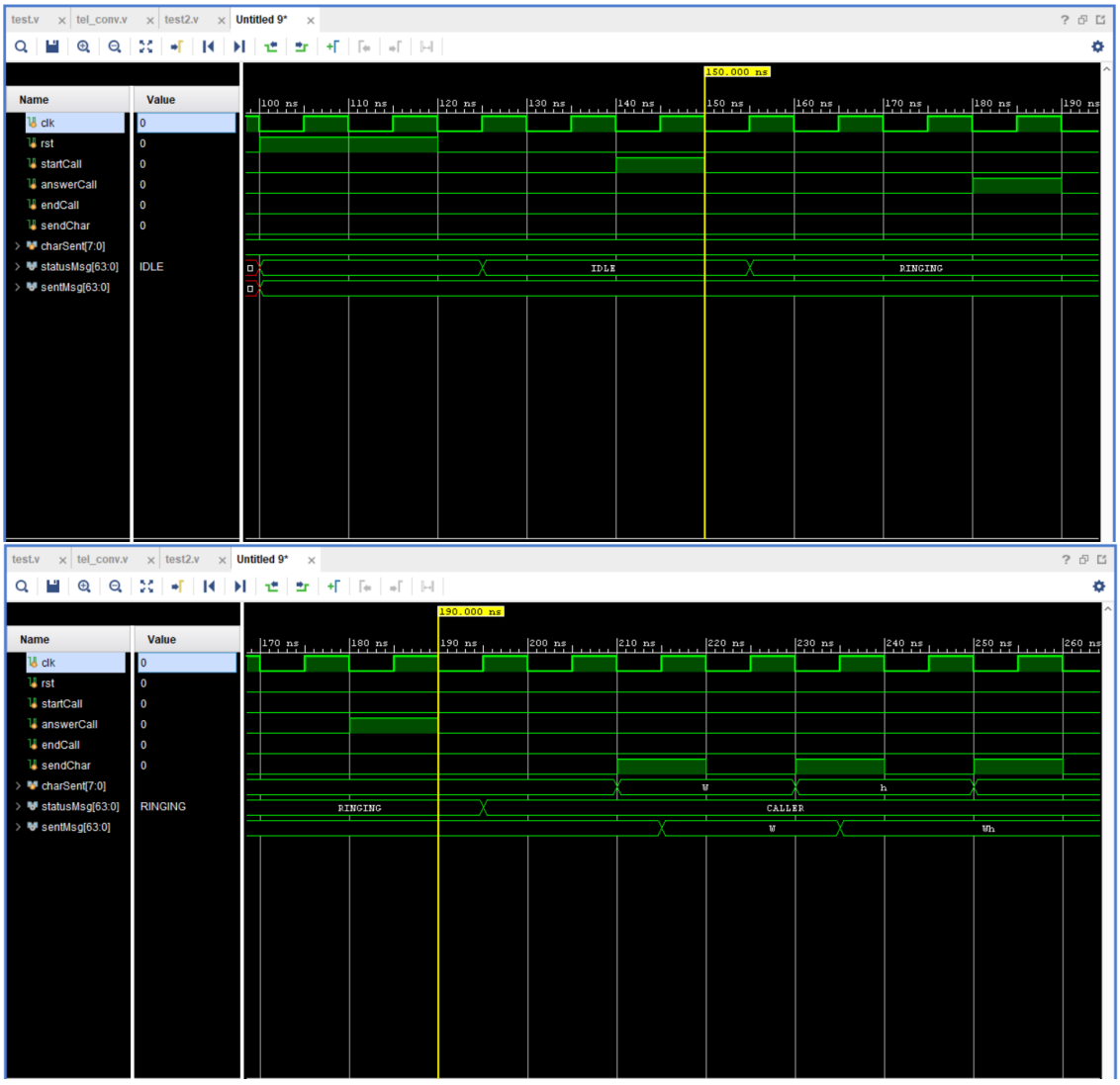
2.1 First Test

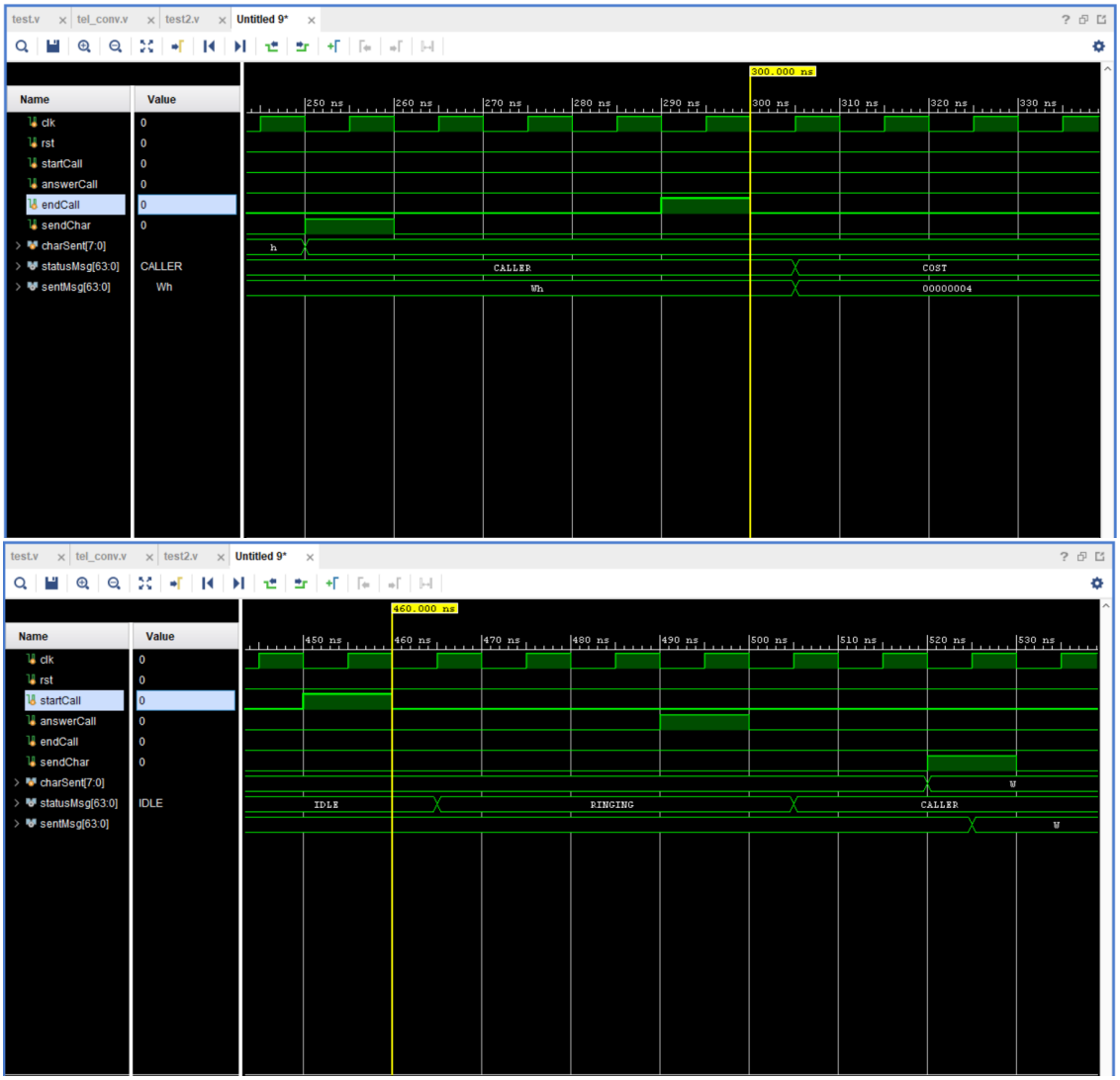


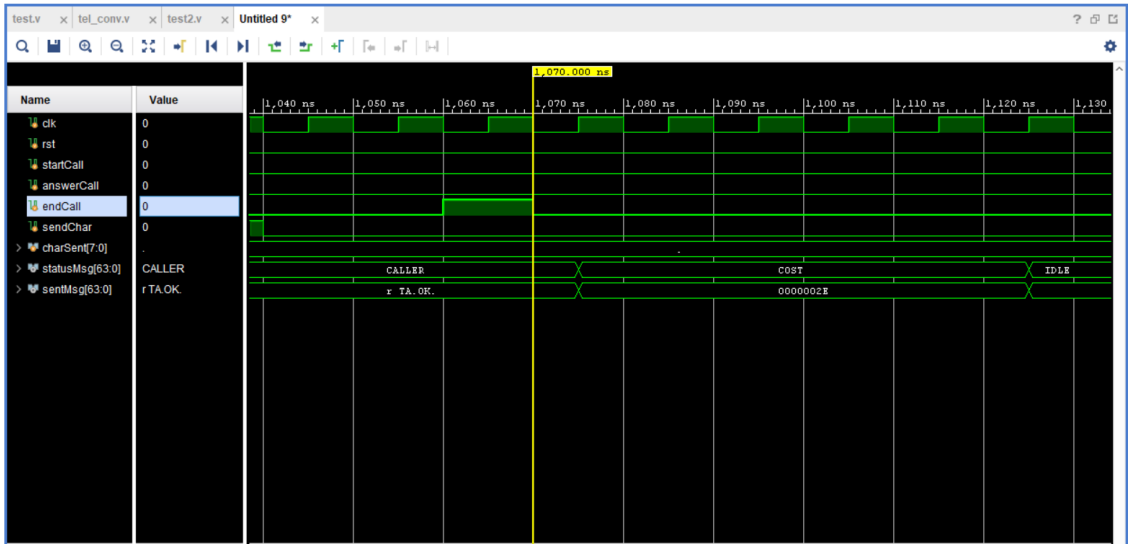

test.v
tel_conv.v
test2.v
Untitled 10*
Name
Value
clk
rst
startCall
answerCall
endCall
sendChar
charSent[7:0]
statusMsg[63:0]
sentMsg[63:0]
RINGING
600.000 ns
560 ns
580 ns
600 ns
620 ns
640 ns
660 ns
680 ns
700 ns
720 ns
740 ns
IDLE
RINGING
CALLER
TERM
925.000 ns
860 ns
870 ns
880 ns
890 ns
900 ns
910 ns
920 ns
930 ns
940 ns
CALLER
COST
PROJECT
0000001A


test.v
tel_conv.v
test2.v
Untitled 10*
935.000 ns
Name
Value
clk
1
rst
0
startCall
0
answerCall
0
endCall
0
sendChar
0
charSent[7:0]
T
statusMsg[63:0]
COST
CALLER
COST
IDLE
sentMsg[63:0]
0000001A
PROJECT
0000001A
910 ns
920 ns
930 ns
940 ns
950 ns
960 ns
970 ns
980 ns
990 ns

2.2 Second Test



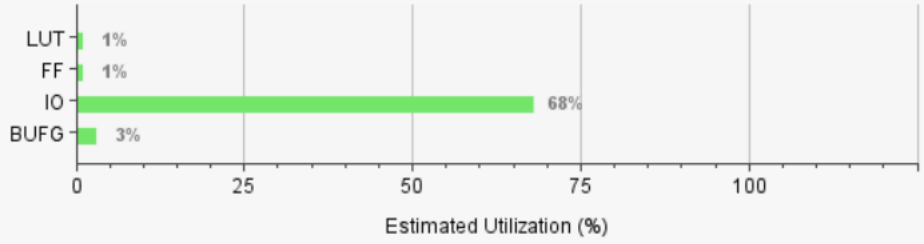

test.v
tel_conv.v
test2.v
Untitled 9*
Name
Value
clk
rst
startCall
answerCall
endCall
sendChar
charSent[7:0]
statusMsg[63:0]
sentMsg[63:0]
0
CALLER
Wh
300.000 ns
250 ns
260 ns
270 ns
280 ns
290 ns
300 ns
310 ns
320 ns
330 ns
h
CALLER
COST
Wh
00000004
460.000 ns
450 ns
460 ns
470 ns
480 ns
490 ns
500 ns
510 ns
520 ns
530 ns
IDLE
RINGING
CALLER
W



3 Synthesis Results

Utilization — **Post-Synthesis** | Post-Implementation

Graph | Table



Utilization — **Post-Synthesis** | Post-Implementation

Graph | **Table**

Resource	Estimation	Available	Utilization %
LUT	172	63400	0.27
FF	143	126800	0.11
IO	142	210	67.62
BUFG	1	32	3.13

```
Hierarchical RTL Component report
Module tel_conv
Detailed RTL Component Info :
+---Adders :
       2 Input     32 Bit       Adders := 2
       2 Input      7 Bit       Adders := 8
       2 Input      4 Bit       Adders := 3
       2 Input      3 Bit       Adders := 1
+---Registers :
                   64 Bit    Registers := 2
                   32 Bit    Registers := 1
                    4 Bit    Registers := 3
                    3 Bit    Registers := 1
+---Muxes :
       2 Input     64 Bit        Muxes := 1
       6 Input     64 Bit        Muxes := 2
       2 Input     32 Bit        Muxes := 2
       6 Input     32 Bit        Muxes := 1
       2 Input      7 Bit        Muxes := 8
       6 Input      6 Bit        Muxes := 1
       2 Input      6 Bit        Muxes := 8
       2 Input      4 Bit        Muxes := 3
       6 Input      4 Bit        Muxes := 3
       2 Input      3 Bit        Muxes := 1
       6 Input      3 Bit        Muxes := 2
       3 Input      1 Bit        Muxes := 1
       4 Input      1 Bit        Muxes := 1
       6 Input      1 Bit        Muxes := 9
       2 Input      1 Bit        Muxes := 2
```

```
Detailed RTL Component Info :
+---Adders :
       2 Input     32 Bit       Adders := 2
       2 Input      7 Bit       Adders := 8
       2 Input      4 Bit       Adders := 3
       2 Input      3 Bit       Adders := 1
+---Registers :
                   64 Bit    Registers := 2
                   32 Bit    Registers := 1
                    4 Bit    Registers := 3
                    3 Bit    Registers := 1
+---Muxes :
       2 Input     64 Bit        Muxes := 1
       6 Input     64 Bit        Muxes := 2
       2 Input     32 Bit        Muxes := 2
       6 Input     32 Bit        Muxes := 1
       2 Input      7 Bit        Muxes := 8
       6 Input      6 Bit        Muxes := 1
       2 Input      6 Bit        Muxes := 8
       2 Input      4 Bit        Muxes := 3
       6 Input      4 Bit        Muxes := 3
       2 Input      3 Bit        Muxes := 1
       6 Input      3 Bit        Muxes := 2
       3 Input      1 Bit        Muxes := 1
       4 Input      1 Bit        Muxes := 1
       6 Input      1 Bit        Muxes := 9
       2 Input      1 Bit        Muxes := 2
-----------------------------------------------
Finished RTL Component Statistics
-----------------------------------------------------------------------------------
Start Part Resource Summary
-----------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
-----------------------------------------------------------------------------------
Finished Part Resource Summary
-----------------------------------------------------------------------------------
```

Report Cell Usage:

	Cell	Count
1	BUFG	1
2	CARRY4	16
3	LUT1	1
4	LUT2	33
5	LUT3	22
6	LUT4	46
7	LUT5	49
8	LUT6	36
9	FDCE	130
10	FDPE	13
11	LD	6
12	IBUF	14
13	OBUF	128

Report Instance Areas:

	Instance	Module	Cells
1	top		495

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	172	0	63400	0.27
LUT as Logic	172	0	63400	0.27
LUT as Memory	0	0	19000	0.00
Slice Registers	149	0	126800	0.12
Register as Flip Flop	143	0	126800	0.11
Register as Latch	6	0	126800	<0.01
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

* Warning! The Final LUT count, after physical optimizations and ful

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
13	Yes	-	Set
136	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	135	0.00
RAMB36/FIFO*	0	0	135	0.00
RAMB18	0	0	270	0.00

* Note: Each Block RAM Tile only has one FIFO logic availa

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	240	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	142	0	210	67.62
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

5. Clocking

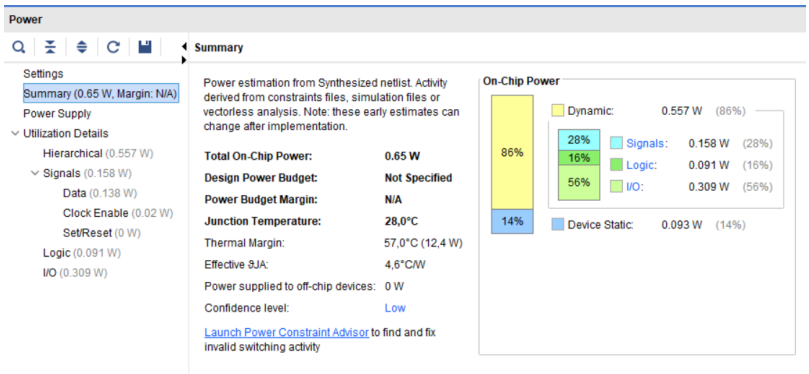
Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	24	0.00
MMCME2_ADV	0	0	6	0.00
PLLE2_ADV	0	0	6	0.00
BUFMRCE	0	0	12	0.00
BUFHCE	0	0	96	0.00
BUFR	0	0	24	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
PCIE_2_1	0	0	1	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
FDCE	130	Flop & Latch
OBUF	128	IO
LUT5	49	LUT
LUT4	46	LUT
LUT6	36	LUT
LUT2	33	LUT
LUT3	22	LUT
CARRY4	16	CarryLogic
IBUF	14	IO
FDPE	13	Flop & Latch
LDCE	6	Flop & Latch
LUT1	1	LUT
BUFG	1	Clock


Power
Summary
Settings
Summary (0.65 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.557 W)
Signals (0.158 W)
Data (0.138 W)
Clock Enable (0.02 W)
Set/Reset (0 W)
Logic (0.091 W)
I/O (0.309 W)
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.
Total On-Chip Power: 0.65 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 28,0°C
Thermal Margin: 57,0°C (12,4 W)
Effective ϑJA: 4,6°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
86%
14%
Dynamic: 0.557 W (86%)
28%
16%
56%
Signals: 0.158 W (28%)
Logic: 0.091 W (16%)
I/O: 0.309 W (56%)
Device Static: 0.093 W (14%)