In our second experiment, we will start using the Nexys A7 Artix-7 FPGA Trainer Board by Digilent. We will use a set of software tools for performing our experiments. These include:

1. The Xilinx Vivado Design Suite for synthesis.
2. Digilent Adept to communicate with the FPGA Board
3. *Digital* for designing logic circuits.

Software Setup for Vivado
You will need to set-up a free Xilinx account to access design tools. After doing so, navigate to

```
https://www.xilinx.com/support/download.html
```

and click "Vivado Archieve" from the menu on the left side of the page. The latest version that has the WebPACK is 2019.1. Download and install "Vivado HLx 2019.1: WebPACK and Editions". When installing, make the following choices:

```
Select Edition to Install : Vivado HL WebPACK
Devices : 7 Series -> Artix-7 (deselect all remaining devices to save disk space)
```

Software Setup for Digilent Adept
Go to

```
https://digilent.com/reference/software/adept/start
```

and, download and install Adept.

Pre-lab assignment
The file *lab2_test.dig* is a simplified test bench for just one seven-segment display and two switches of the Nexys A7 board. This test bench contains a sub-circuit which is defined in *lab2.dig*, as shown in in Fig. 1.

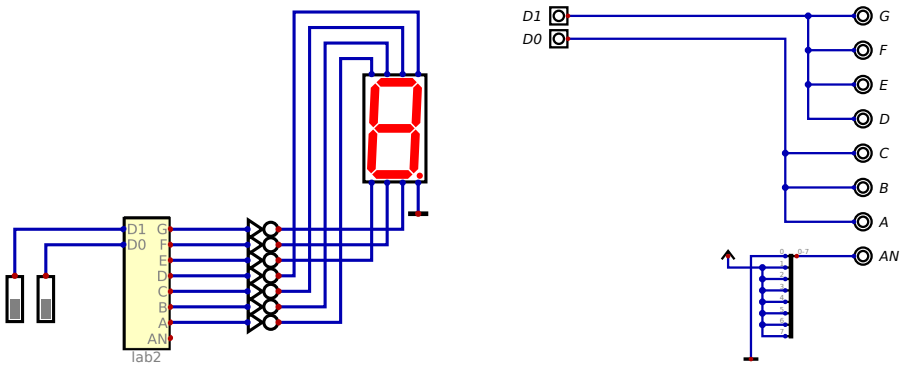

Fig. 1: Test bench for the lab assignment (left), template for the circuit to be deigned (right).

You are expected to modify *lab2.dig* so that it acts as a 2-bit input digital to seven-segment decoder, as done in Homework #2. Note that the test bench has additional inverters to drive the display to mimic the behavior of the Nexys A7 board, so you may need to modify the circuit you designed for the homework. Keep the circuit producing the 8-bit AN output intact. This is necessary for the FPGA board to function properly.

Once you show that your circuit functions correctly, export *lab2.dig* as a Verilog file, which should create a file named *lab2.v*. This will be used in Vivado to map your design into an FPGA bit file.

Optional (but strongly suggested) pre-lab work
Create a Vivado project with *xc7a100tcsg324-1* as the target device. Define *lab2.v* as the Verilog source, and *lab2.xdc* (provided on SUcourse) as the design constraints file. Synthesize the design to generate a .bit file. This file will be uploaded to the Nexys A7 board using Adept tools.

In-lab
During the laboratory session, you will test your circuit on the Nexys A7 board. You will be then asked to make a modification to the circuit to implement a different function. You may work in groups of two. Bring along your computer with all the software tools installed.

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