



# Chapter 1

## Boolean Logic

### Boolean Algebra

$$\begin{aligned}
 x \text{ or } y &= \bar{x}y + x\bar{y} + xy \\
 &= \bar{x}y + x(y + \bar{y}) \\
 &= x + \bar{x}y \\
 &= x + \overline{x + \bar{y}} \\
 &= \overline{\overline{x + \bar{y}}} \\
 &= \overline{\bar{x}(x + \bar{y})} \quad \text{where } \overline{x + \bar{y}} = \bar{x}\bar{y} \\
 &= \overline{x\bar{x} + \bar{x}\bar{y}} \\
 &= \overline{\bar{x}\bar{y}} \\
 &= \overline{\overline{x + y}} \\
 &= x + y
 \end{aligned}$$

$$\begin{aligned}
 \text{if } y \text{ then } x &= \bar{x}\bar{y} + x\bar{y} + xy \\
 &= \bar{x}\bar{y} + x(y + \bar{y}) \\
 &= x + \bar{x}\bar{y} \\
 &= x + \overline{x + y} \\
 &= \overline{\overline{x + y}} \\
 &= \overline{\bar{x}(x + y)} \\
 &= \overline{x\bar{x} + \bar{x}y} \\
 &= \overline{\bar{x}y} \\
 &= x + \bar{y}
 \end{aligned}$$

$$\begin{aligned}
 \text{if } x \text{ then } y &= \bar{x}\bar{y} + \bar{x}y + xy \\
 &= \bar{x}\bar{y} + (x + \bar{x})y \\
 &= \bar{x}\bar{y} + y \\
 &= \overline{x + y} + y \\
 &= \overline{\overline{x + y} + y} \\
 &= \overline{(x + y)\bar{y}} \\
 &= \overline{x\bar{y} + y\bar{y}} \\
 &= \overline{\bar{x}\bar{y}} \\
 &= \bar{x} + y
 \end{aligned}$$

$$\begin{aligned}
 x \text{ nand } y &= \bar{x}\bar{y} + \bar{x}y + x\bar{y} \\
 &= \bar{y}(x + \bar{x}) + \bar{x}y \\
 &= \bar{y} + \bar{x}y \\
 &= \bar{x} + \bar{y} \quad \text{where } x + y = x + \bar{x}y \\
 &= \overline{\overline{\bar{x} + \bar{y}}} \\
 &= \overline{\bar{x}\bar{y}}
 \end{aligned}$$

## Chapter 5

# Computer Architecture

### 5.1 Memory

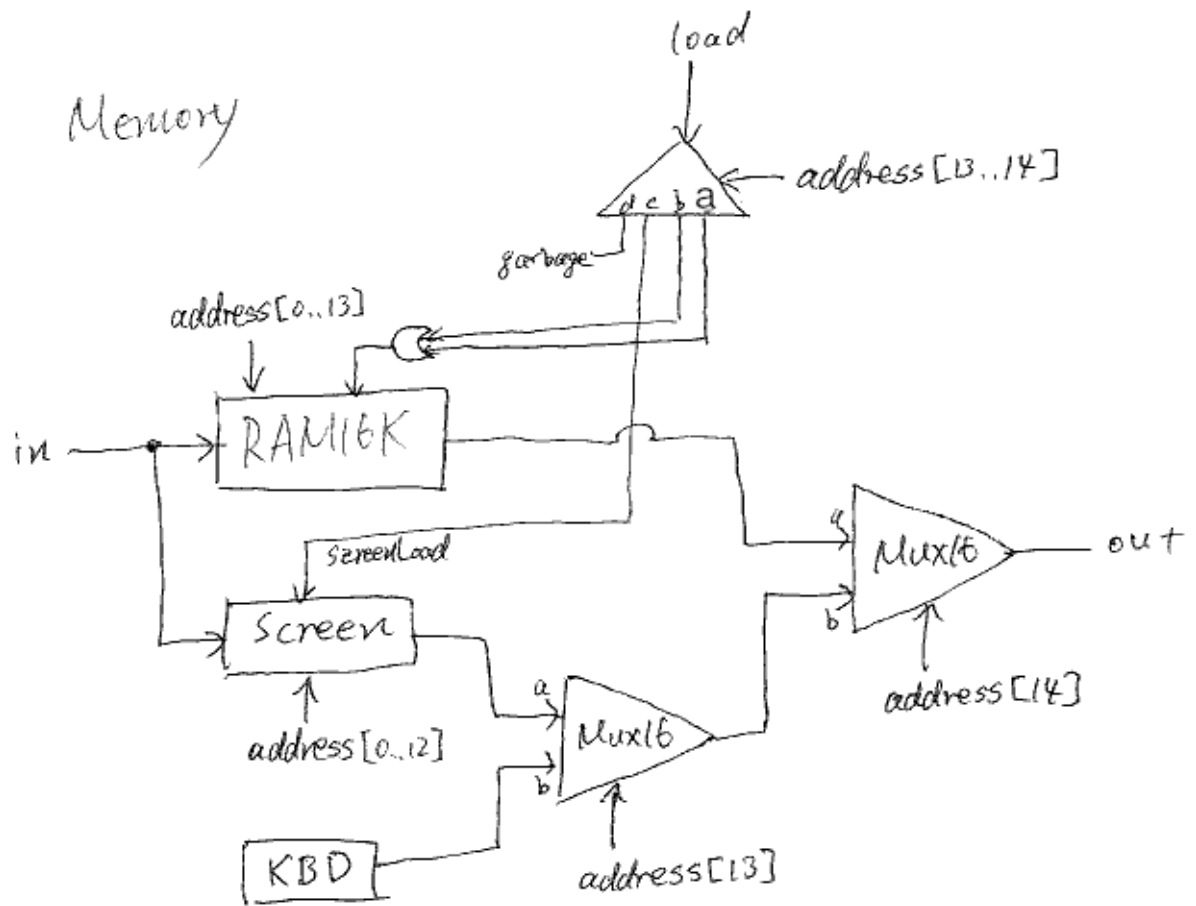


Figure 5.1: memory

### 5.2 CPU

C-instruction =  $111ac_1c_2c_3c_4c_5c_6d_1d_2d_3j_1j_2j_3$

- $d_1$ : destination A
- $d_2$ : destination D
- $d_3$ : destination M

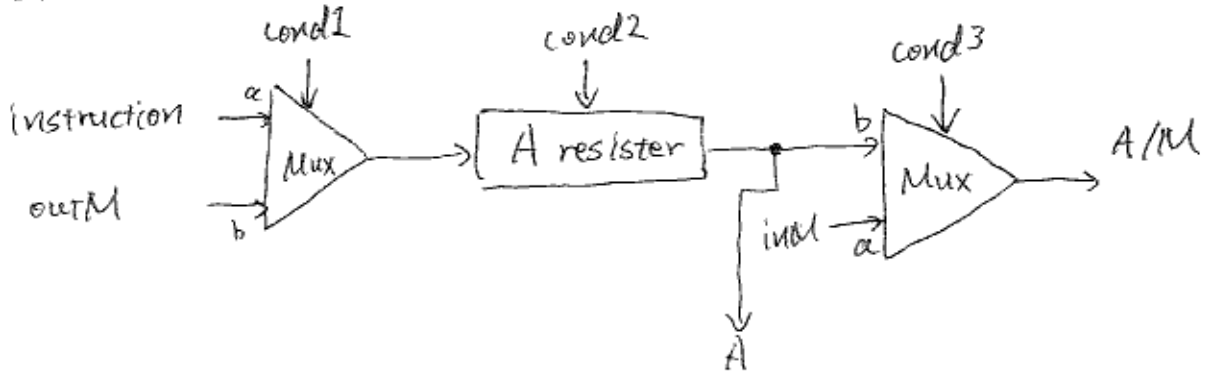


Figure 5.2: memory

$\text{cond1} = \text{instruction}[15]$   
 $\text{cond2} = (\text{not } \text{instruction}[15]) \text{ or } (\text{instruction}[15] \text{ and } \text{instruction}[5])$   
 $\text{cond3} = \text{instruction}[15] \text{ and } \text{not } \text{instruction}[12]$

- $\text{instruction}[15]$ : opcode
- $\text{instruction}[12]$ : C-instruction's  $a$ . If  $a$  is 1, comp includes A, otherwise, comp includes M.
- $\text{instruction}[5]$ : destination A.

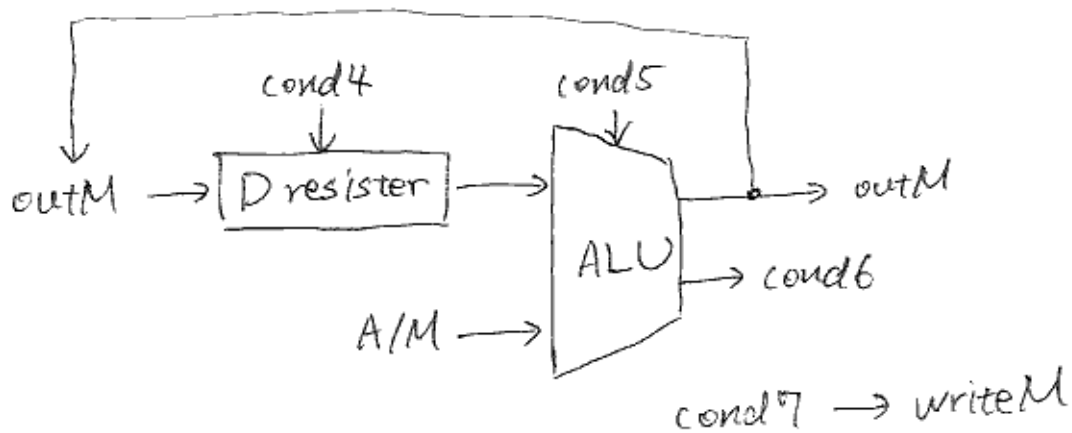


Figure 5.3: memory

$\text{cond4} = \text{instruction}[15] \text{ and } \text{instruction}[4]$

$\text{cond5} = \begin{cases} \text{zx} = \text{instruction}[11] = c_1 \\ \text{nx} = \text{instruction}[10] = c_2 \\ \text{zy} = \text{instruction}[9] = c_3 \\ \text{ny} = \text{instruction}[8] = c_4 \\ \text{f} = \text{instruction}[7] = c_5 \\ \text{no} = \text{instruction}[6] = c_6 \end{cases}$

$\text{cond6} = (\text{zr}, \text{ng})$

$\text{cond7} = \text{instruction}[15] \text{ and } \text{instruction}[3]$

- $\text{instruction}[3]$ :  $d_3$ , destination M

- instruction[4]:  $d_2$ , destination D

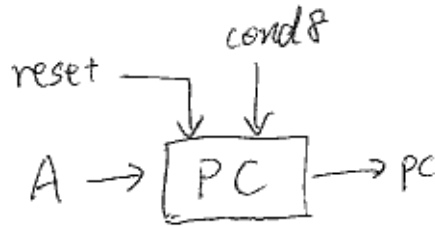


Figure 5.4: memory

$$\begin{aligned}
 \text{cond8} = & \overline{\text{zr}} \cdot \overline{\text{ng}} \cdot \overline{j_1} \cdot \overline{j_2} \cdot \overline{j_3} & (\text{JGT}) \\
 & + \overline{\text{zr}} \cdot \overline{j_1} \cdot j_2 \cdot j_3 & (\text{JEQ}) \\
 & + \overline{\text{ng}} \cdot \overline{j_1} \cdot j_2 \cdot j_3 & (\text{JGE}) \\
 & + \text{ng} \cdot j_1 \cdot \overline{j_2} \cdot \overline{j_3} & (\text{JLT}) \\
 & + \overline{\text{zr}} \cdot j_1 \cdot \overline{j_2} \cdot j_3 & (\text{JNE}) \\
 & + (\text{zr} + \text{ng}) \cdot j_1 \cdot j_2 \cdot \overline{j_3} & (\text{JLE}) \\
 & + j_1 \cdot j_2 \cdot j_3 & (\text{JMP})
 \end{aligned}$$