# APH001 APPLICATION NOTE

# DW1000 HARDWARE DESIGN GUIDE

**Version 1.0**

**This document is subject to change without notice**

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# 1 Introduction

## 1.1 Overview

Guidelines for successful hardware design of systems using the DW1000 UWB transceiver IC are presented in this application note.

## 1.2 Document Structure

The document begins with a diagrammatic overview of a typical DW1000 hardware system and a recommended application circuit schematic of the DW1000. Guidance on the number of PCB layers and board floorplan to use is then presented. Then specific advice is given on areas such as power architecture, RF transmission lines and connector interfaces, antennas and electromagnetic interference (EMI).

The Decawave EVB1000 evaluation board serves as a layout reference design which can be copied by customers. Included in the appendices of this application note is a section showing the layout graphics. Layout files in .dxf format are included in the package accompanying this application note.

The following table summarises the content of the main sections.

**Table 1. Summary of Main Sections**

| Section | Description |
|---|---|
| 1. Introduction | Objective of document and structural overview. |
| 2. DW1000 Hardware System Overview | Presents a diagram of a typical hardware system, with all major blocks, including DW1000.<br>Focuses on DW1000 application circuit with required external components. |
| 3. PCB Technology | Discusses the optimum number of PCB layers. |
| 4. Layout Floorplan | Suggests the best positioning of circuit blocks, antenna, etc. on the board. |
| 5. Power Management | General layout advice for switched-mode power supply circuits. |
| 6. DW1000 Transceiver | Guidelines for successful layout of DW1000, including power decoupling, RF tracks, etc. |
| 7. RF Connectors | PCB design guidelines for RF connectors. |
| 8. Antennas | Overview of IR-UWB antenna specifications and Decawave reference designs. |
| 9. Electromagnetic Interference | Managing sources of EMI from the PCB and product assembly. |
| 14. Advantages of Using Microvias and More PCB Layers | Demonstration of how physically smaller boards can be realised by using more layers and microvia technology. |
| 15. EVB1000 PCB Layout .dxf Files | Layout graphics from Decawave EVB1000 PCB. |

# 2 DW1000 Hardware System Overview

## 2.1 Overview

A logical first step in the hardware design of an electronic system is to review the system block diagram and schematic details, before considering PCB design matters such as the number of copper layers to use and the board floorplan.

## 2.2 System Block Diagram

A hardware system involving the DW1000 UWB transceiver includes several other main components. A simplified system block diagram of an example system is shown in Figure 1. An antenna and balun connect to the DW1000's RF port to provide the radio air interface, while a host microcontroller (MCU) processes data and controls the DW1000 via serial peripheral interface (SPI) and GPIO interfaces.

The battery is regulated to provide a 3.3 V rail for MCU and DW1000 circuits. An additional DCDC converter is recommended for generating the DW1000 1.8 V supply rail.

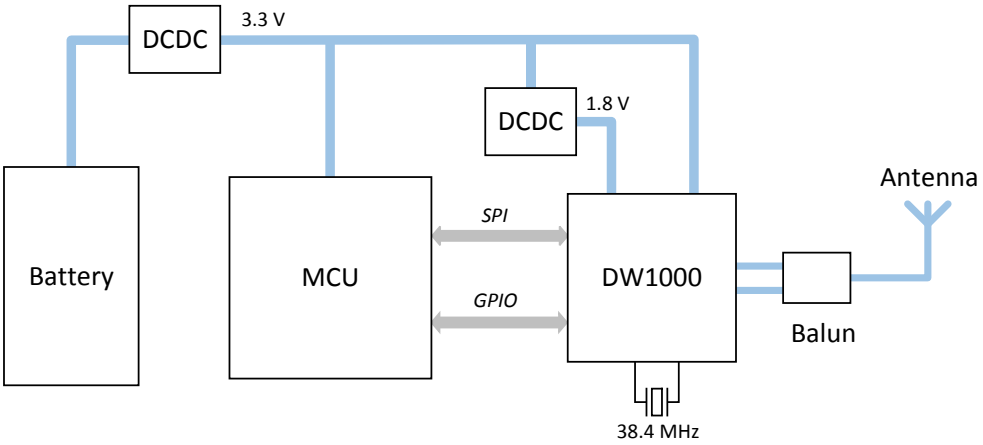



**Figure 1. Overview of DW1000 Hardware System**

## 2.3 DW1000 Application Circuit

It's useful to consider the external components required in the DW1000 application circuit, shown in Figure 2. These can be categorised as follows.

- ***RF Front-End:***
  An antenna is needed for the radio air interface. An antenna with a single-ended feed is usually used, which requires a balun (T1) to convert a single-ended transmission line to the DW1000's balanced RF port.

- ***Frequency Reference:***
  A 38.4 MHz crystal (X1) with two loading capacitors is connected to the DW1000. Alternatively, a TCXO reference (X2) may be used, though this requires an additional LDO regulator (U3) to provide a low-noise power supply.

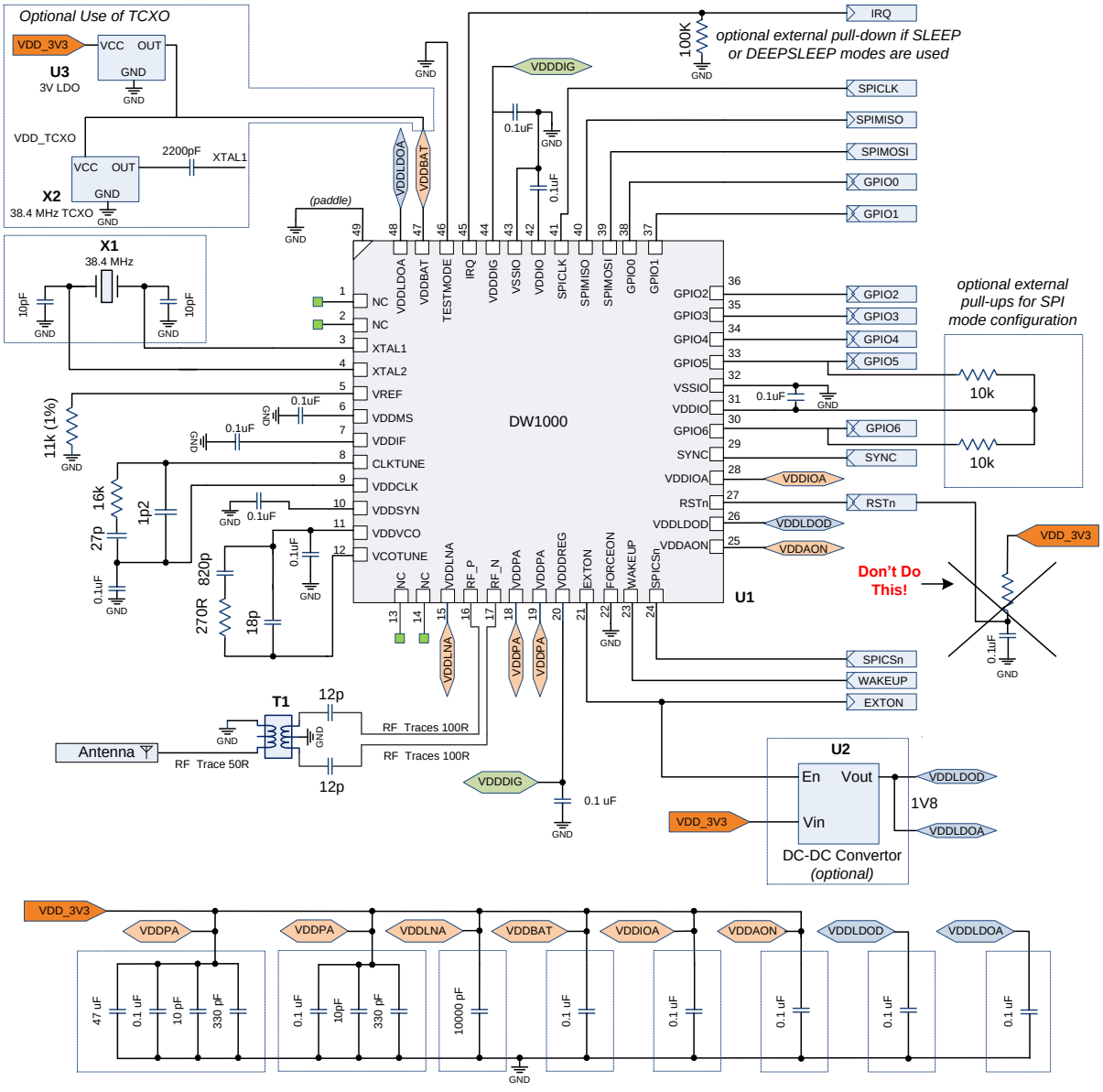
- ***PLL Loop Filters:***
  The DW1000 has two internal phase-locked loop (PLL) circuits, generating baseband processing clock and RF local oscillator signals. Each PLL requires external loop filter components.

- ***3.3 V Power Supply:***
  The DW1000 has eight power supply pins, six of which are supplied with a 3.3 V nominal voltage and two of which can optionally be supplied with a lower voltage of 1.8 V. The 3.3 V supplies each require at least one decoupling capacitor, with the VDDPA pins needing three decoupling capacitors each.

- ***1.8 V Power Supply:***
  Two power supply pins can be supplied with a lower voltage of 1.8 V. This requires the use of an external DCDC converter (U2). Additional bulk capacitors are needed for the DCDC converter aswell as decoupling capacitors for the 1.8 V DW1000 supply pins.

- ***Internal Regulator Decoupling:***
  External decoupling capacitors are required for various internal DW1000 LDO regulators.

- ***Current Reference Resistor:***
  An external, low-tolerance (1%) resistor connects to the DW1000 VREF pin.




*Decoupling: Place capacitors close to pins*

**Figure 2. DW1000 Application Circuit**

# 3 PCB Technology

## 3.1 Overview

Having looked at the hardware system and schematics, decisions about the PCB solution can be considered.

## 3.2 Number of Layers

A PCB design needs to follow certain fundamental design guidelines. Using a PCB with too few copper layers can make it very difficult or impossible to satisfy these guidelines.

- ***RF Track Widths:***
  The RF transmission line dimensions need to be accurately controlled. Differences in widths between PCB tracks and component pads should be minimised.
  Figure 3 shows 50 ohm tracks on 2-layer and 4-layer boards. Much wider tracks are needed with 2 layers, which causes impedance discontinuities with narrow component pads, conductors of RF connectors, etc.

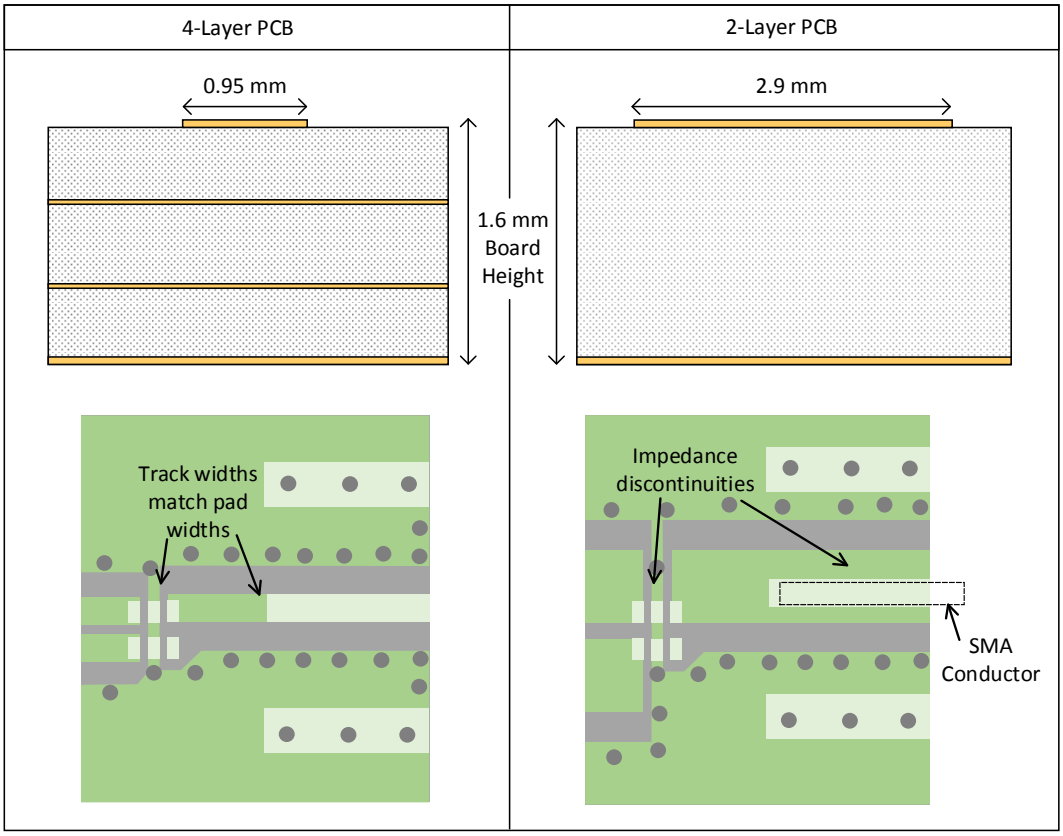



**Figure 3. RF Track Widths on 2 and 4-layer PCBs**

- ***RF Transmission Line Return Current Path:***
  Tracks carrying high frequency signals (e.g. RF signal transmission lines) must have a short return current path without obstructions in the ground plane beneath the track.
  Figure 4 compares examples of 2-layer and 4-layer DW1000 layouts, where it can be seen that with 2 layers, power tracks below the RF differential tracks block the direct path of return current flowing towards the DW1000. This lengthens the return current path and causes impedance mismatch.

- ***Decoupling Capacitors:***
  Decoupling capacitors must be placed close to power supply pins and the return current path to the IC should be kept as short as possible.
  In the 2-layer board in Figure 4, the power tracks block the direct path of current returning to the DW1000 in the ground plane. This makes the capacitor is less effective at decoupling noise.

- ***Noise Isolation:***
  Sensitive signals must be isolated from noisy signals.
  In the 2-layer board in Figure 4, the power tracks are routed below the sensitive crystal and PLL loop filter components, exposing them to noise on the power tracks.

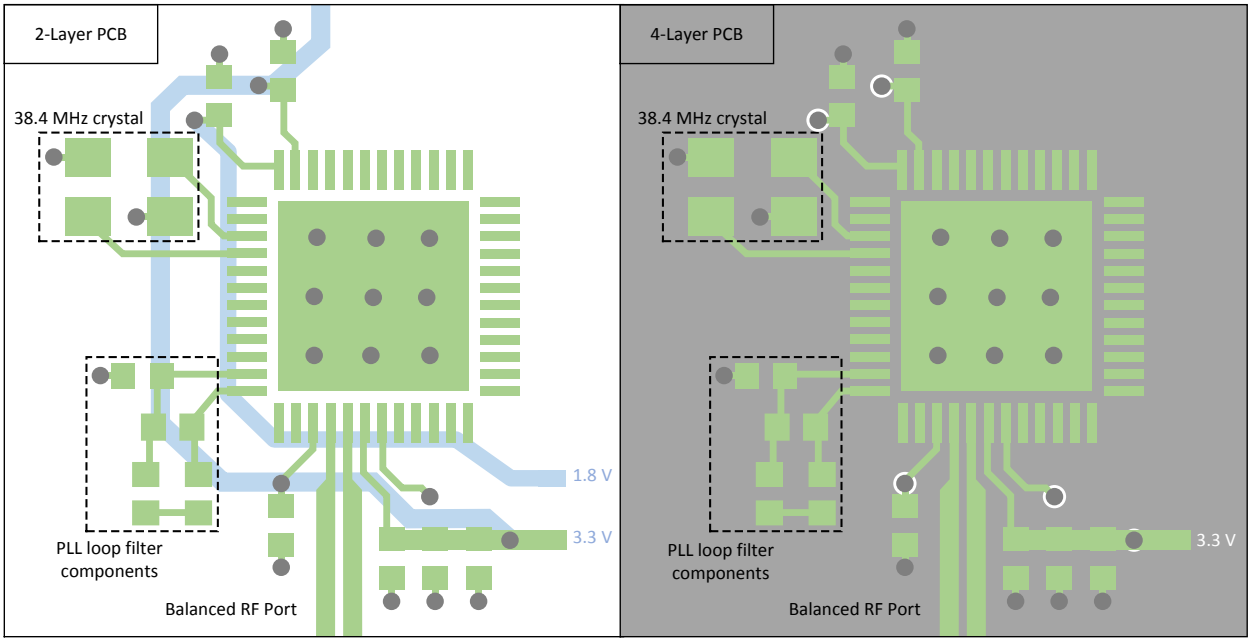



**Figure 4. DW1000 Layout on 2 and 4 Layer PCBs**

A board with 4 layers can satisfy all of the design guidelines above by using a continuous ground plane on the layer below the DW1000 component layer. It is therefore recommended that **at least 4 copper layers are used in the PCB**.

Having six or more layers offers further advantages in terms of board space, ease of routing, etc. More detail can be found in Appendix A.

In general, PCB layers should be flooded with ground copper, i.e. the entire area of the copper layer not occupied with traces or components should be filled with copper connected to ground. This reduces the impedance of the ground plane, helping to keep ground at different places on the board at the same potential. It is also important for shielding noise from sensitive traces. Copper should not be flooded, however, near antennas on the PCB. See section 4.3 for more information.

## 3.3 Recommended 4-Layer PCB Stack-up Solution

For 4-layer PCB designs, it is recommended to copy the stack-up shown in Figure 5. This stack-up is used in the Decawave EVB1000 evaluation board. The stack-up consists of layers of copper foil between layers of core and pre-preg (pre-impregnated) glass-reinforced epoxy laminate, known as 'FR4'. Dielectric constants for core and pre-preg materials is 4.2.

For the layout of RF traces, the PCB manufacturer must be consulted to ensure that trace impedances are controlled.

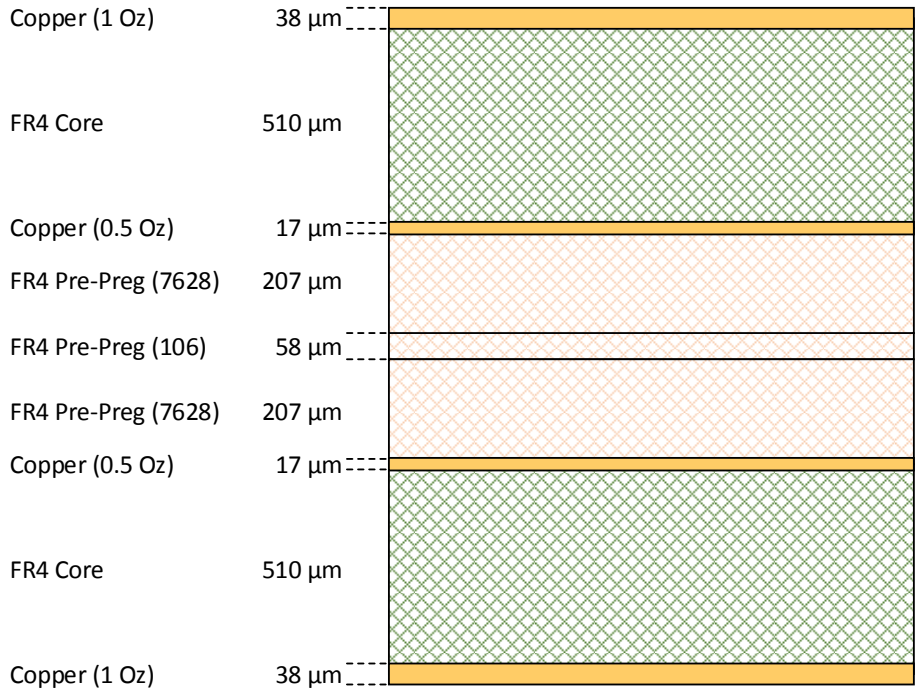



**Figure 5. Recommended PCB Stack-up**

# 4 Layout Floorplan

## 4.1 Overview

The floorplan concerns choosing where on the board to best place the different circuit sections. The main considerations are minimising noise coupling through power routing and avoiding interference with the antenna's radiation pattern.

## 4.2 Power Architecture

A system involving the DW1000 usually includes a microcontroller, power management circuits for regulating power and peripheral circuitry such as sensors. A high-level block diagram showing the flow of current in the power network of a typical system is shown in Figure 6, where a battery provides the power source.

There are a couple of fundamental factors to consider when placing the circuit sections from the point of view of power routing.

- ***Power Management:***
  The total power consumed by the board is supplied through the regulators and chargers in the power management section. As high currents and switching regulators are usually involved, this circuitry should be placed close to the battery or power source and away from RF circuits, which are sensitive to noise.

- ***Isolating Digital and RF Power Routing:***
  Digital circuit sections such as the microcontroller create clock harmonics and transients when circuits change state at high speed. To isolate the RF power supply from noise on the digital supply, ideally each section should be fed using separate paths from the regulator in the power management section. If separate paths can't be made, then it's acceptable to share paths but the RF circuitry must be furthest from the power management circuitry to prevent noise from the digital section entering the RF section.

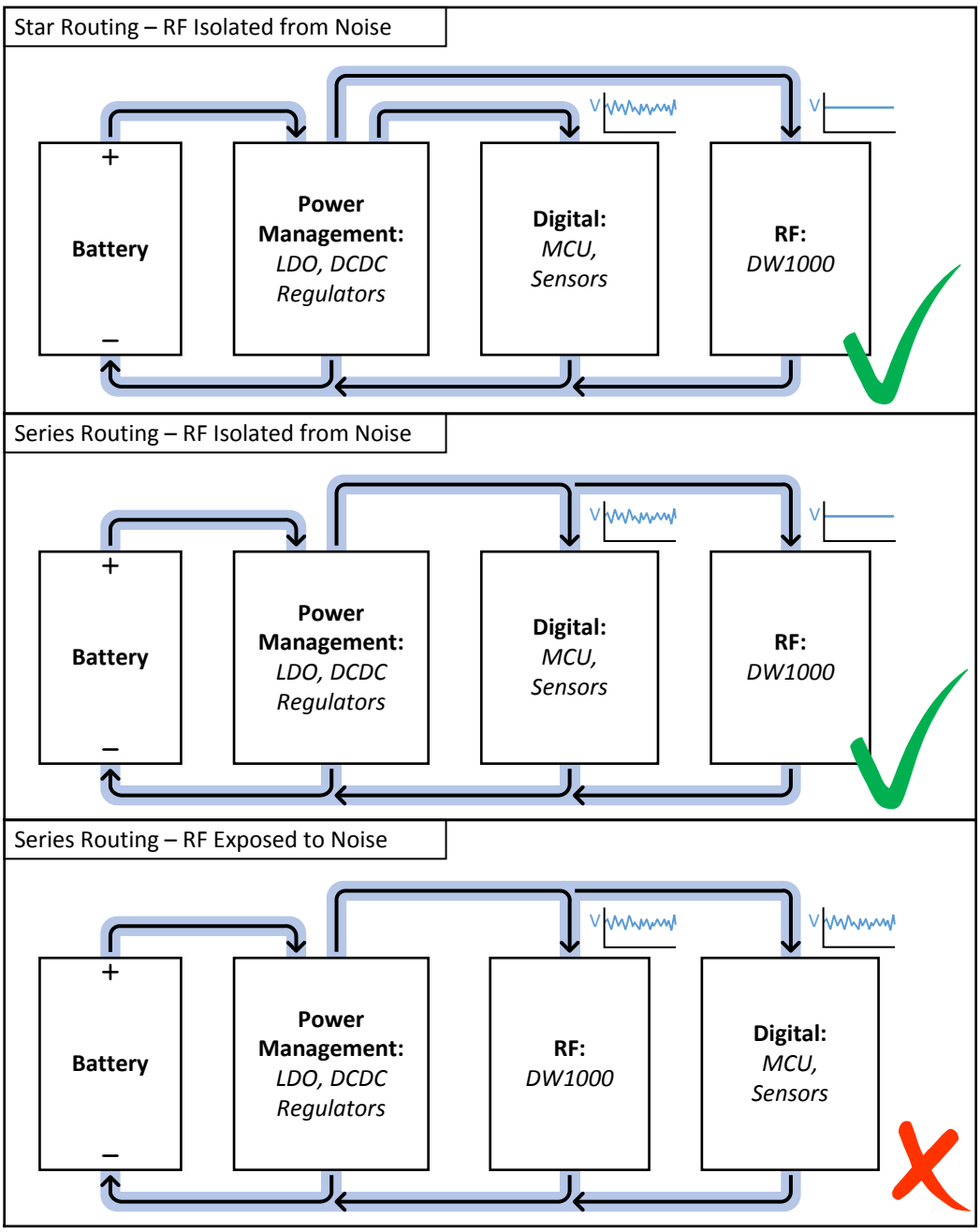



**Figure 6. Conceptual Power Routing of Circuit Sections**

## 4.3 Antenna Considerations

When placing a chip antenna or printing an antenna pattern on a PCB, care must be taken to ensure that no objects, especially metallic ones, are positioned in the antenna's radiating plane.

A vertically polarised monopole has nulls through its vertical axis, as illustrated in the X-Z plane pattern in Figure 7. As the PCB ground plane lies within the antenna's null, the radiation pattern isn't affected but if obstructions such as copper or metallic components enter the X-Y plane, then the gain in this direction is reduced (Figure 8).

Having an omnidirectional antenna (i.e. one having the same gain in all directions in a certain plane) is important because it allows the location of other DW1000 devices to be determined more accurately.

For specific layout and placement advice for your chosen antenna, follow the guidelines given by the antenna manufacturer.

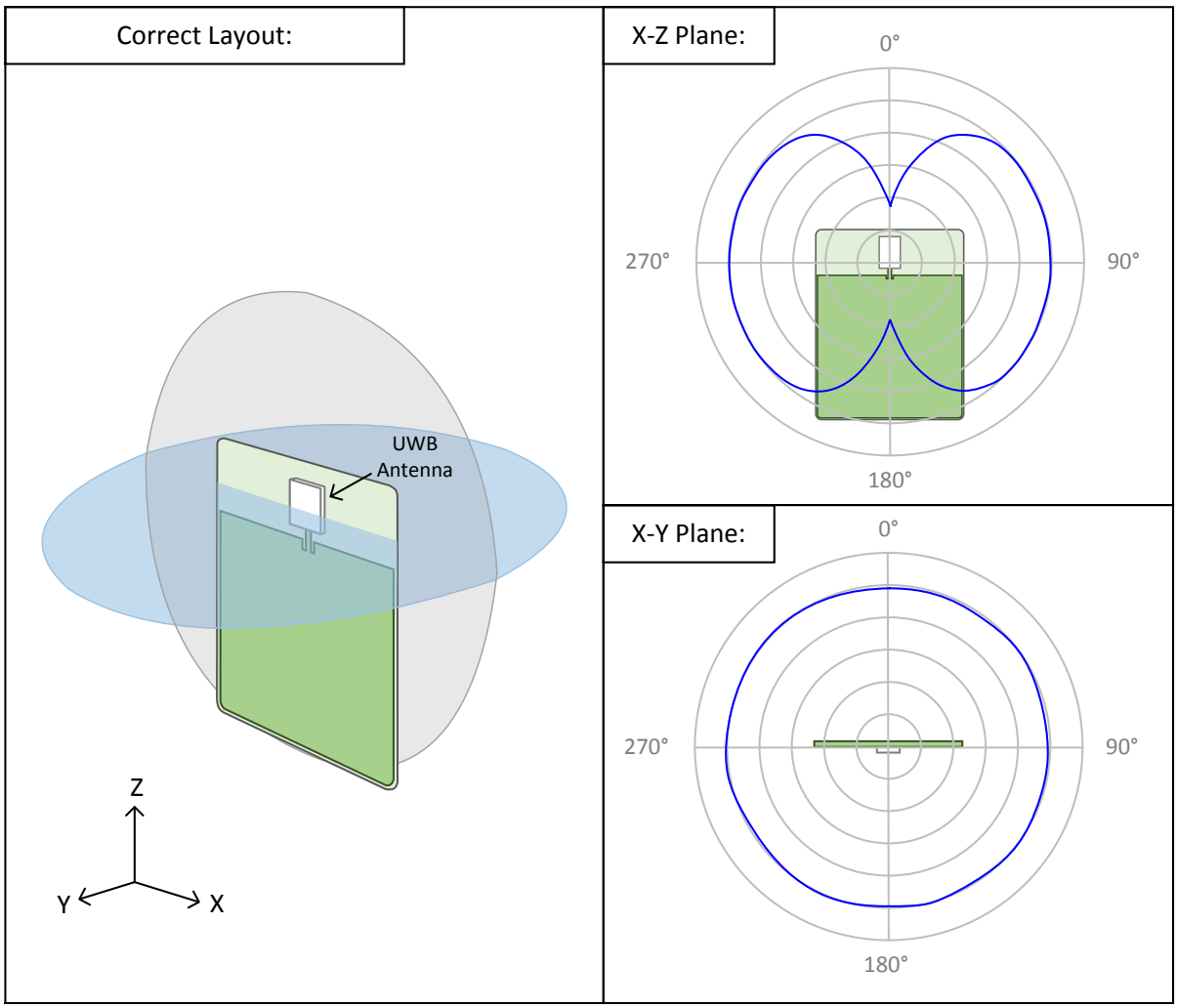



**Figure 7. Radiation Patterns with Correct Layout**

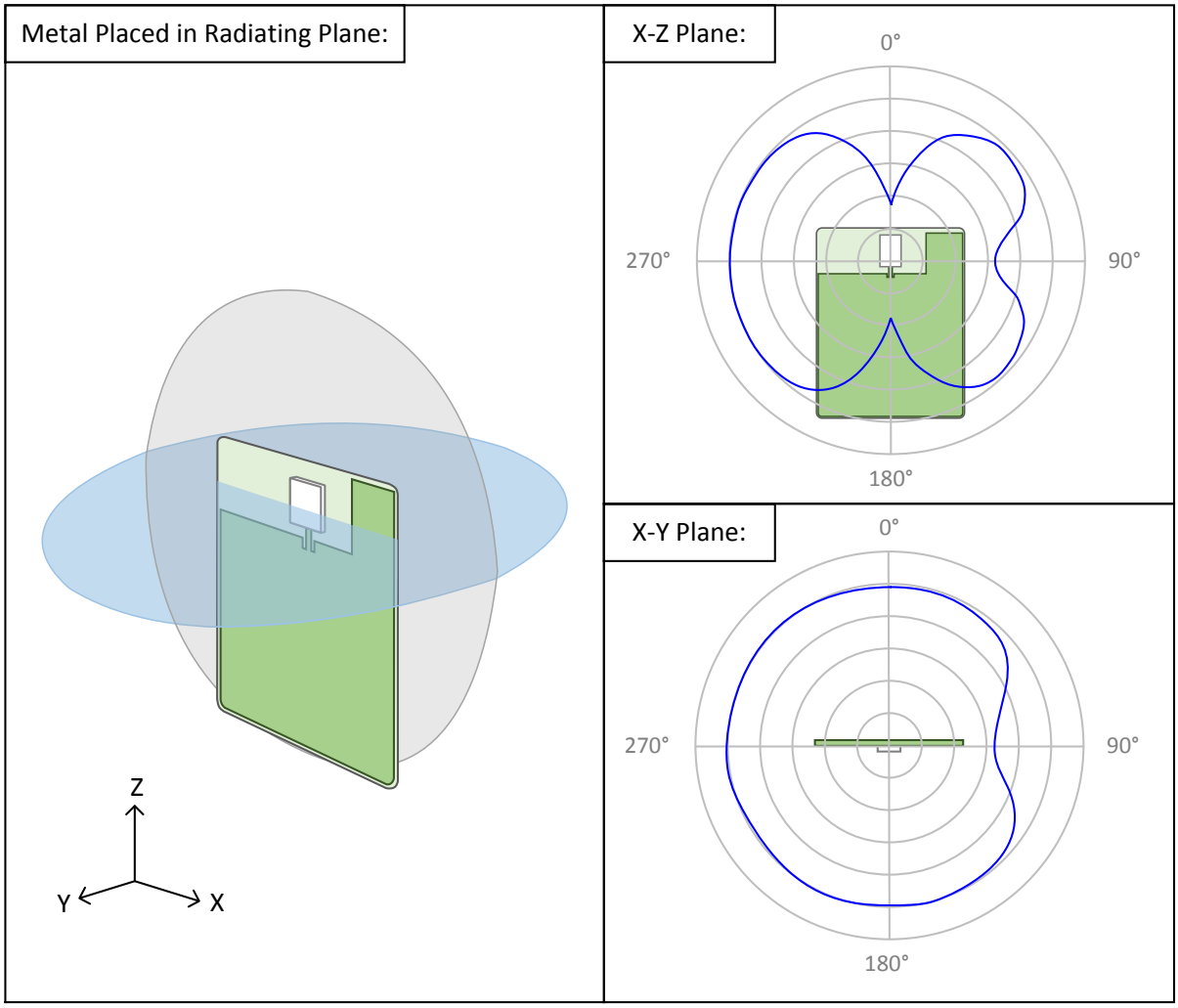



**Figure 8. Radiation Patterns with Metal Obstruction in Radiating Plane**

## 4.4 Example Floorplan

The requirement for the UWB antenna to be placed away from components and copper on the PCB usually mandates that the UWB antenna and RF circuitry are placed towards one end of a PCB. Power is often supplied through leads and, since these leads can act as antennas themselves, it is advisable to place power terminals as far away as possible from the antenna. Placing power management circuitry close to the power terminals and microcontroller, and sensors between power management and RF sections leads to a floorplan that meets the fundamental requirements in terms of noise isolation and UWB antenna performance.

Antennas for other radio technologies shouldn't share the UWB antenna area, but should be spatially isolated from the UWB antenna as much as possible.

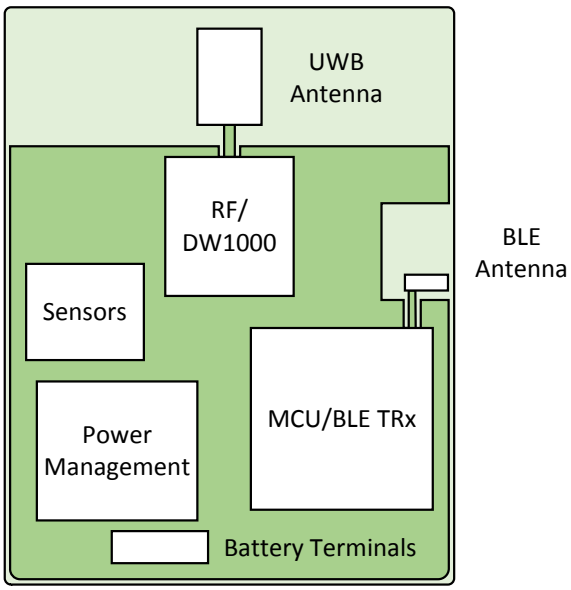



**Figure 9. Example PCB Floorplan for UWB Product (with BLE)**

# 5 Power Management

## *5.1 Switched-Mode Power Supplies*

It's beneficial to use switched-mode power supplies, also known as DCDC converters, as opposed to LDOs (Low Drop-Out regulators) for power regulation as they offer increased power efficiency and therefore longer battery life. Greater consideration must be given to the layout of DCDC converters, however, in order to ensure they operate correctly.

A step-down, or BUCK DCDC converter IC typically requires bulk capacitors at the input and output aswell as an output power inductor. Current loops are formed at the input and output stages and the area of these loops must be minimised in order to limit parasitic inductance. Excessive inductance can compromise the stability of the regulator and generate electromagnetic interference (EMI) due to the regulator's switching process, which can propagate to other sensitive circuits on the PCB.

Figure 10 shows a generic DCDC converter circuit. Current loop areas can be minimised by placing components as close as possible to the regulator IC, with short, wide tracks connecting component terminals to the IC pins.

Always follow the specific layout guidelines in the regulator vendor's datasheet.

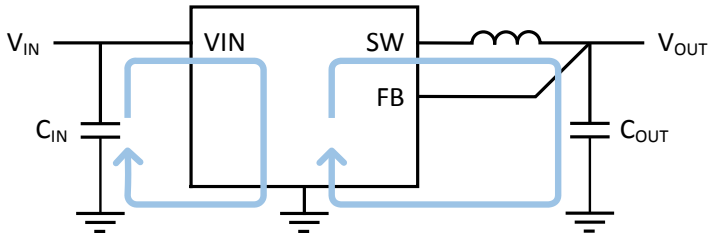



**Figure 10. Generic Switched-Mode Power Supply Circuit**

# 6 DW1000 Transceiver

## 6.1 Local Power Supply Routing and Decoupling

The DW1000 has eight power supply pins, each requiring decoupling capacitors which should be placed as close as possible to the pin. A nominal 3.3 V supply level is required, though the on-chip LDOs can be supplied with 1.8 V. An external DCDC converter can supply the 1.8 V voltage for greater power efficiency.

In a PCB layout, the 3.3 V supply can be routed to the DW1000 using either a power plane or power tracks, with narrower tracks used to route to decoupling caps and pins. The 47 µF bulk cap should be placed close to the VDDPA pins, though lower-valued capacitors should be placed closest.

The 1.8 V DCDC converter can be supplied with the local 3.3 V supply for the DW1000.

External capacitors are also needed for decoupling the DW1000's internal LDO regulator outputs. These are shown on the right hand side of the DW1000 block in Figure 11. VDDDIG and VDDDREG are outputs of the same internal LDO regulator and they should be connected together on the PCB in order to minimize impedance between the decoupling capacitors and the internal circuits.

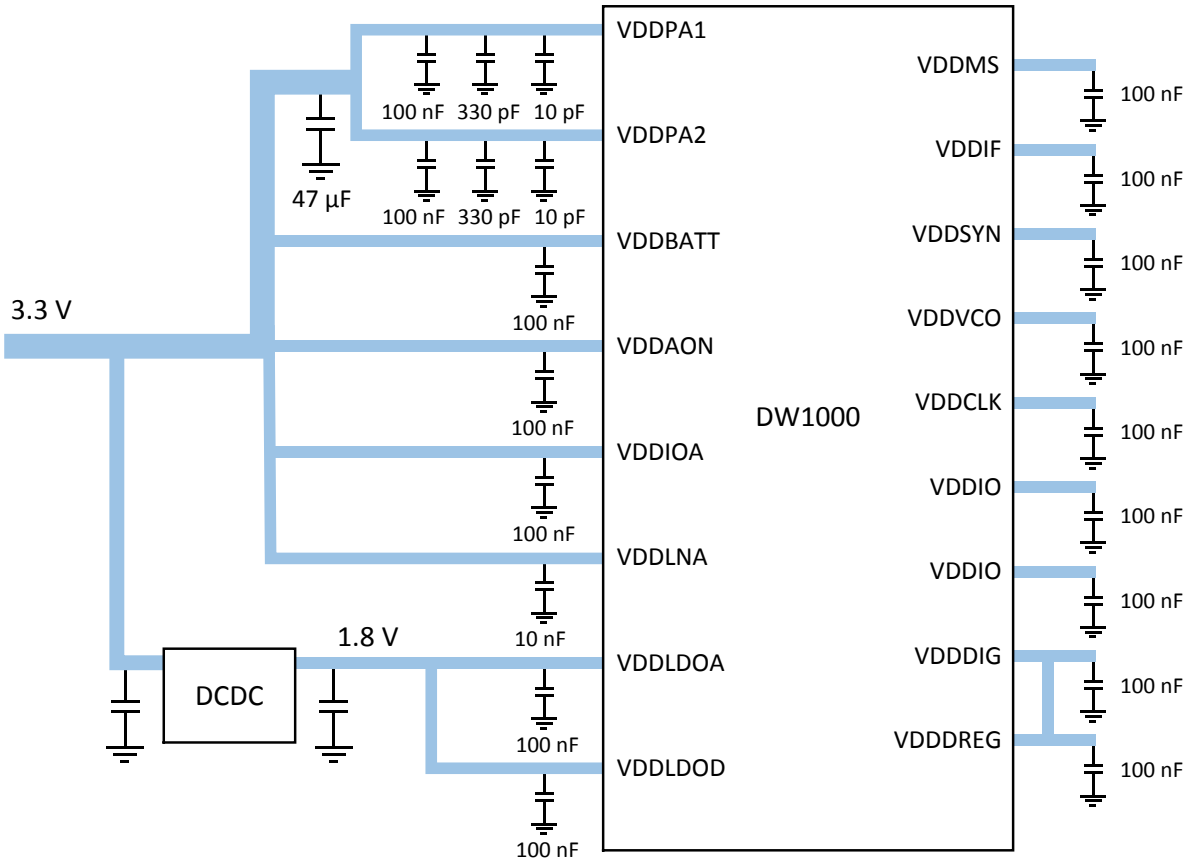



**Figure 11. Local Power Supply Routing and Decoupling**

## 6.2 Effective Capacitive Decoupling

Decoupling capacitors should be placed as close as possible to DW1000 power supply pins. When routing power through a via, the decoupling capacitor should be placed on the power track between the via and the pad of the IC. This ensures that noise on the supply line is decoupled through the capacitor, rather than bypassing it.

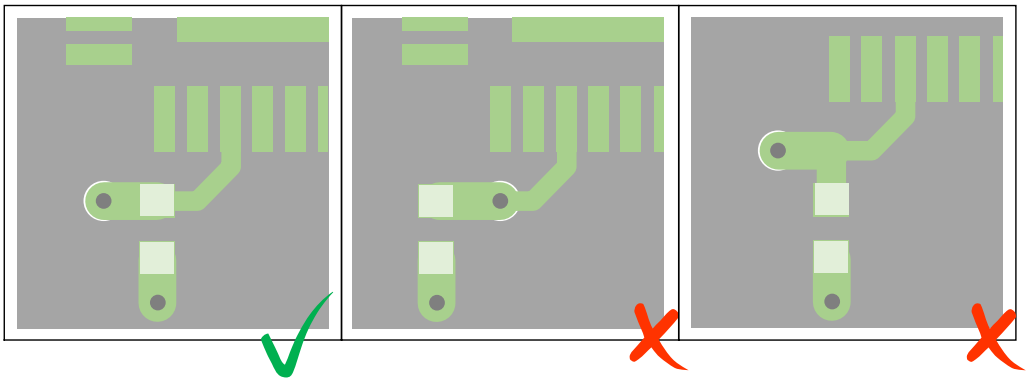


**Figure 12. Correct Positioning of Decoupling Capacitor on Power Track**

## 6.3 Decoupling Noise with Multiple Capacitors

The DW1000's internal power amplifier stages can generate noise with more power and higher in frequency than other internal circuits. Several capacitors are therefore used on the VDDPA1 and VDDPA2 power tracks, in order to decouple noise through the frequency spectrum.

Lower capacitor values should be placed closer to the VDDPA pin, so that the return path to the IC is minimised for higher frequency noise. Since board parasitics create larger impedances at higher frequencies, minimising the return current path limits noise propagation to other parts of the board.

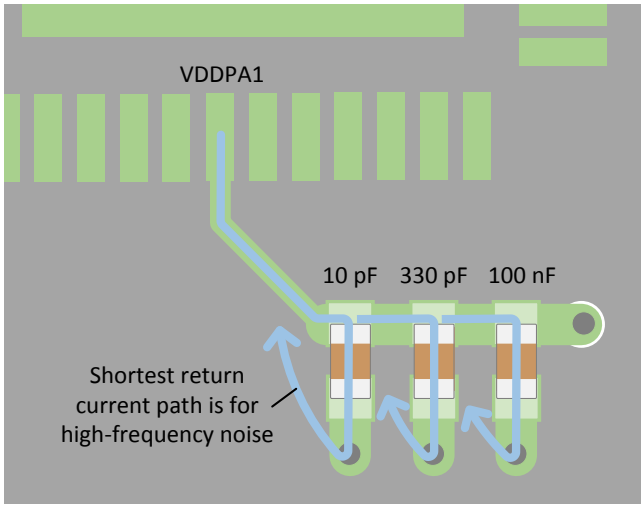



**Figure 13. Placing Lowest Value Caps Closest to Pins**

### 6.3.1 VDDPA1 and VDDPA2 Routing

Although VDDPA1 and VDDPA2 pins are located beside each other, each pin should be decoupled separately. Avoid joining the pads together but rather route the tracks to their decoupling capacitors so that noise from the pins can be isolated.

## 6.4 RF Layout

### 6.4.1 Transmission Lines

The DW1000 has a balanced 100 Ω RF port, to which an external balun can be connected to transform to a single-ended 50 Ω port for connection to an antenna or RF connector. Therefore, the PCB layout usually requires 100 Ω differential and 50 Ω single-ended transmission lines.

Follow these guidelines for the layout of DW1000 RF transmission lines.

- Route RF transmission lines on the same layer as the DW1000. Vias in the RF signal path should be avoided as they create impedance discontinuity and reduce isolation.
- Ensure transmission line impedances are controlled accurately from source to load. The PCB manufacturer can advise how to implement differential and single-ended transmission lines for the PCB specification used.
- Ensure there is an unbroken ground path beneath transmission lines so that current paths in the RF track and ground plane beneath it are of matching lengths. Figure 14 shows an example of how the return current path could be lengthened by the presence of another track in the ground layer beneath the RF track.
- Use ample vias at source and load ends of the transmission line to minimise impedance in the return current path.
- Place vias joining ground planes on adjacent layers around the border of transmission lines to shield the RF signal. This technique is sometimes called ‘stitching’ or ‘picket fencing’. The distance between adjacent vias should be small relative to the wavelength (λ) of the highest frequency signal on the RF trace. The recommended distance is λ/20.
- Remove soldermask above transmission lines. It is difficult to control the uniformity of the soldermask thickness which can result in impedance variation. Use thin strips of soldermask at the ends of the transmission line where they connect to component pads to prevent solder from the pads from spreading over the tracks.
- Keep tracks short to minimise insertion loss, which is increased at UWB frequencies.
- Keep the RF track as straight as possible as bends can introduce impedance discontinuities. If a bend must be used, make the bend radius as large as possible, as shown in Figure 15.

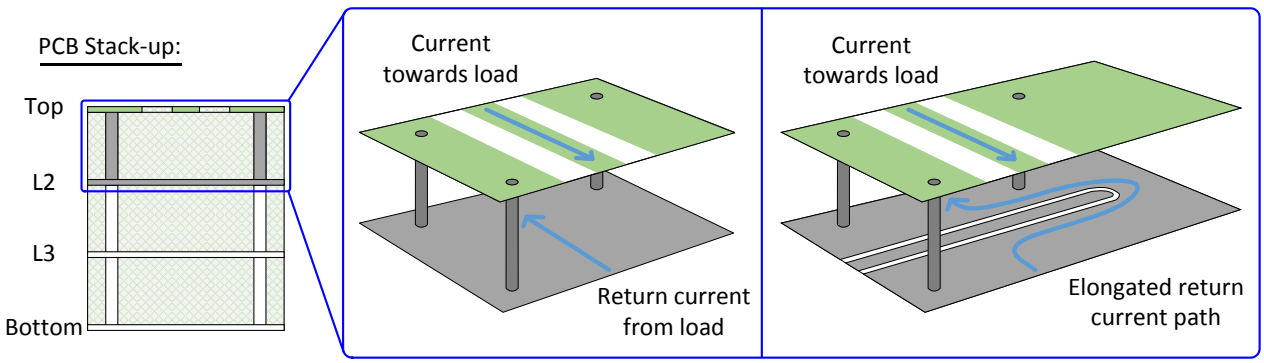



**Figure 14. RF Transmission Line Return Current Paths**

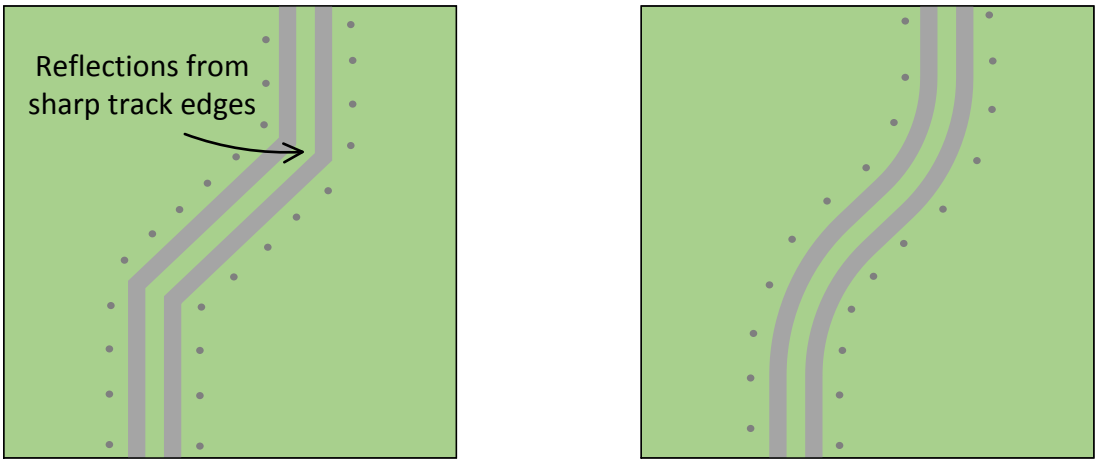



**Figure 15. Smooth Bends in RF track**

The EVB1000 layout is shown in Figure 16 as an example of an optimum layout of the RF path from DW1000 to antenna. DW1000 RF port pins connect to the DC blocking capacitors through narrow differential traces. The differential traces between the capacitors and the balun's balanced port are implemented as 50 ohm single-ended traces. The trace leading from the balun's single-ended port is also 50 ohms. All traces are referenced to ground on the layer immediately beneath the traces.

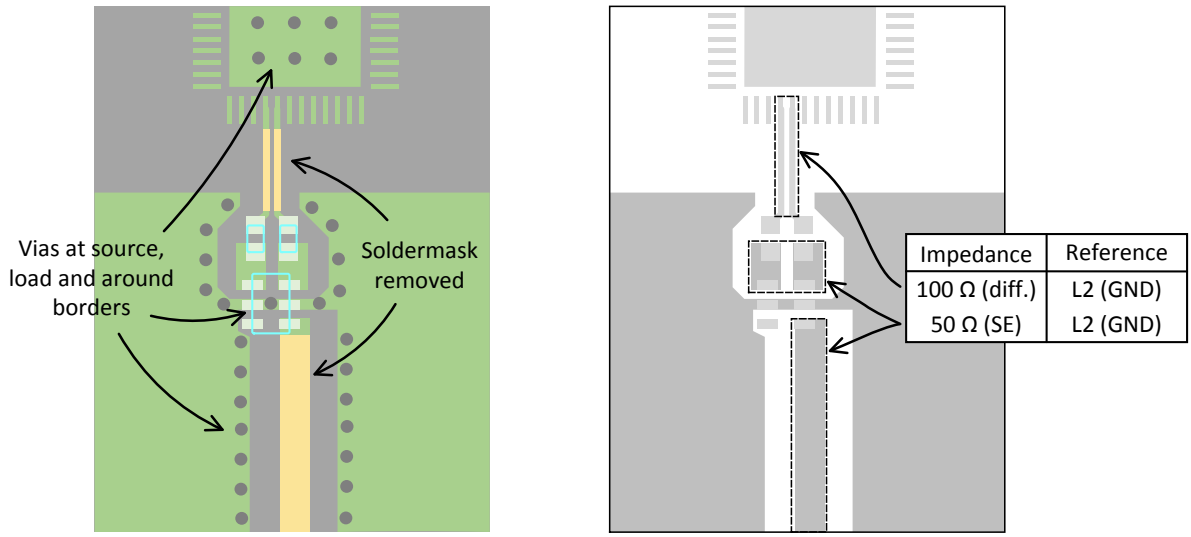



**Figure 16. RF Transmission Line Layout**

### 6.4.2 Placement of Sensitive RF Components

#### 6.4.2.1 Crystal and Loop Filter Components

An external 38.4MHz crystal provides the frequency reference for internal digital and RF phase-locked loops (PLL). Both PLLs require external loop filter components. Crystal and loop filter tracks must be isolated from noise so components should be placed close to the relevant DW1000 pins, with continuous ground on the PCB layer beneath the components.

#### 6.4.2.2 1.8 V DCDC Converter

If placed close to the DW1000, the DCDC converter should be on the opposite side of the IC to the crystal and PLL loop filter components to avoid switching noise coupling to the sensitive RF circuits, as illustrated in Figure 17.

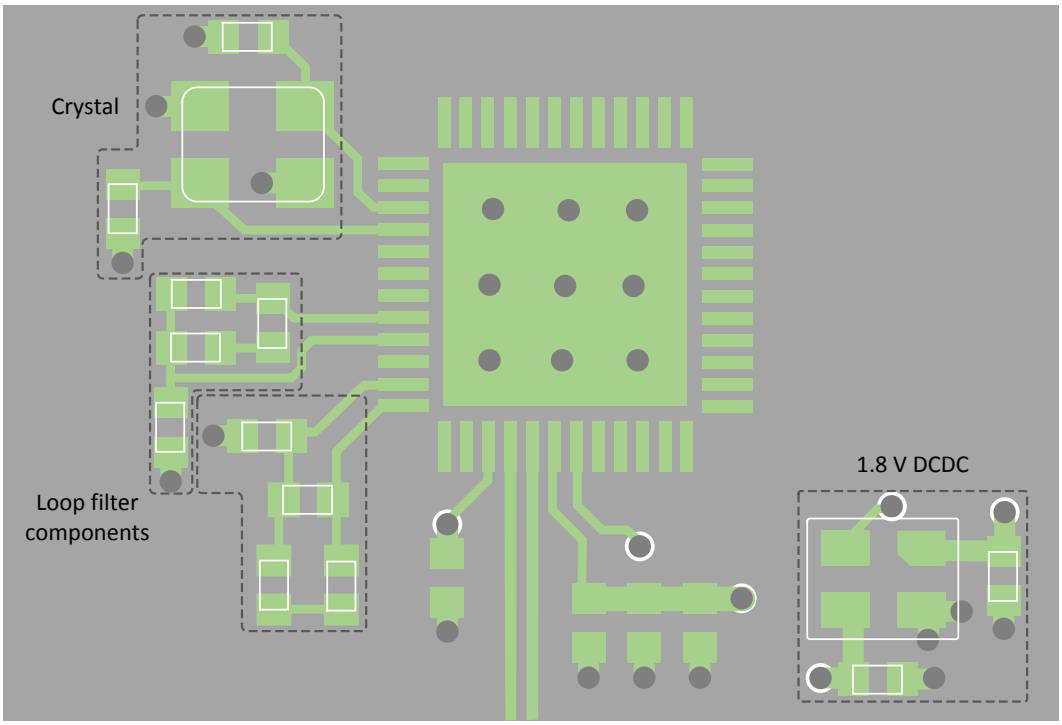



**Figure 17. Placement of Sensitive RF Components**

## 6.5 TCXO Guidelines

A temperature-controlled crystal oscillator (TCXO) can be used as a frequency reference for the DW1000. To maximise the spectral purity of the reference signal, the TCXO power supply pin and DW1000 VDDBATT pin must be isolated from noise. It is therefore recommended that an LDO regulator is used to supply both TCXO and VDDBATT power supply pins.

Figure 18 shows how noise can be coupled to the 3.3 V rail from the PAs during frame transmission. Due to its power supply ripple rejection capability, the LDO can filter this noise to provide a clean voltage supply to the TCXO and VDDBATT pin.

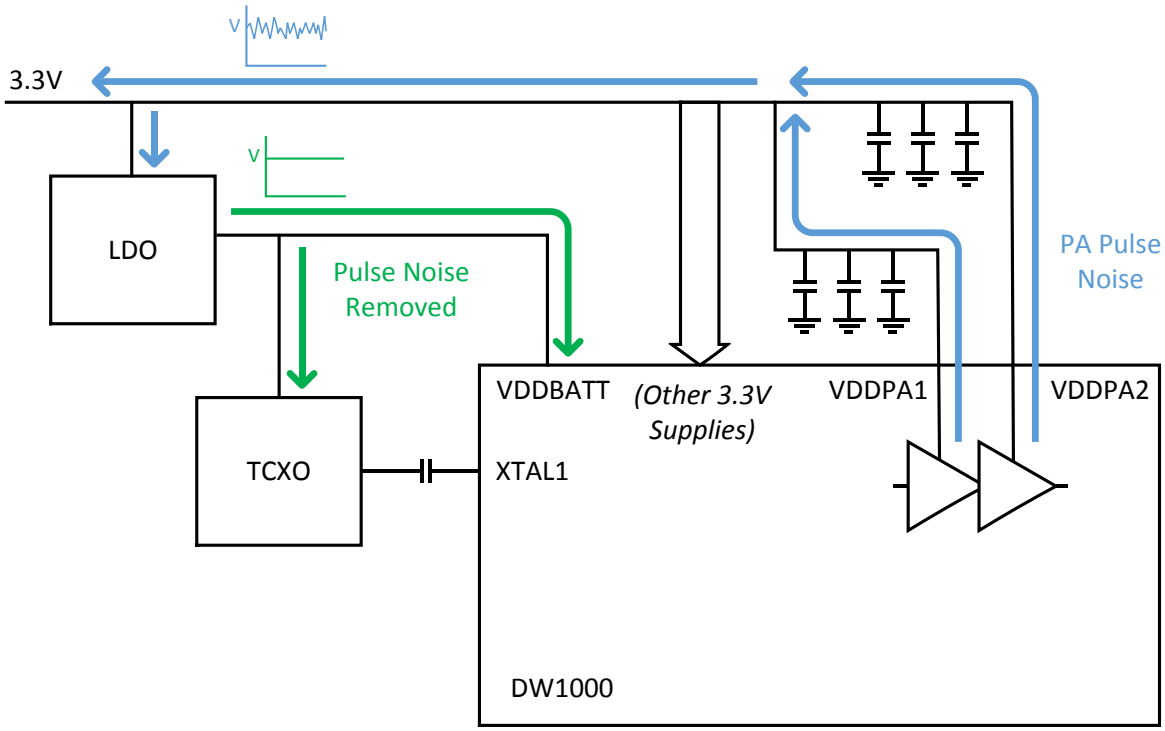



**Figure 18. Isolating Noise when using a TCXO**

## 6.6 Microcontroller Interface

The DW1000 has various digital I/O ports which relate to its interaction with the host microcontroller. Specific hardware guidelines which apply to some of these ports are presented here.

### 6.6.1 SPI Mode Selection

The DW1000 supports four different SPI modes for compatibility with the host microcontroller's SPI polarity and phase specification. GPIO5 and GPIO6, which are set as inputs during device power up, are used to select the appropriate SPI mode. These GPIOs have internal pull-down resistors and so the default is SPI mode 0. Pull-up resistors can be used to select SPI modes 1 – 3, as shown in Figure 19.

Further information can be found in the DW1000 datasheet [1].

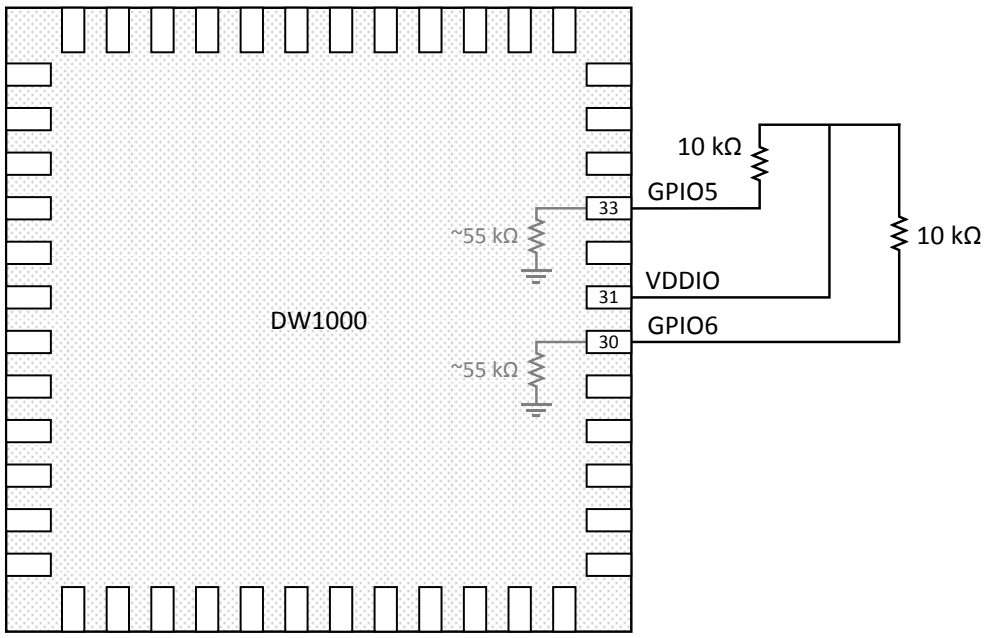



**Figure 19. SPI Mode Pull-up Resistors**

### 6.6.2 Interrupt Request Output

The interrupt request (IRQ/GPIO8) pin can be used to signal specific events to the host microcontroller to trigger interrupts. When the DW1000 is in SLEEP or DEEPSLEEP states, the IRQ pin will be floating. An external pull-down resistor is therefore required to ensure that spurious interrupts aren't signalled to the microcontroller.

More information on interrupt events and IRQ/GPIO8 pin configuration can be found in the DW1000 datasheet [1] and DW1000 user manual [2].

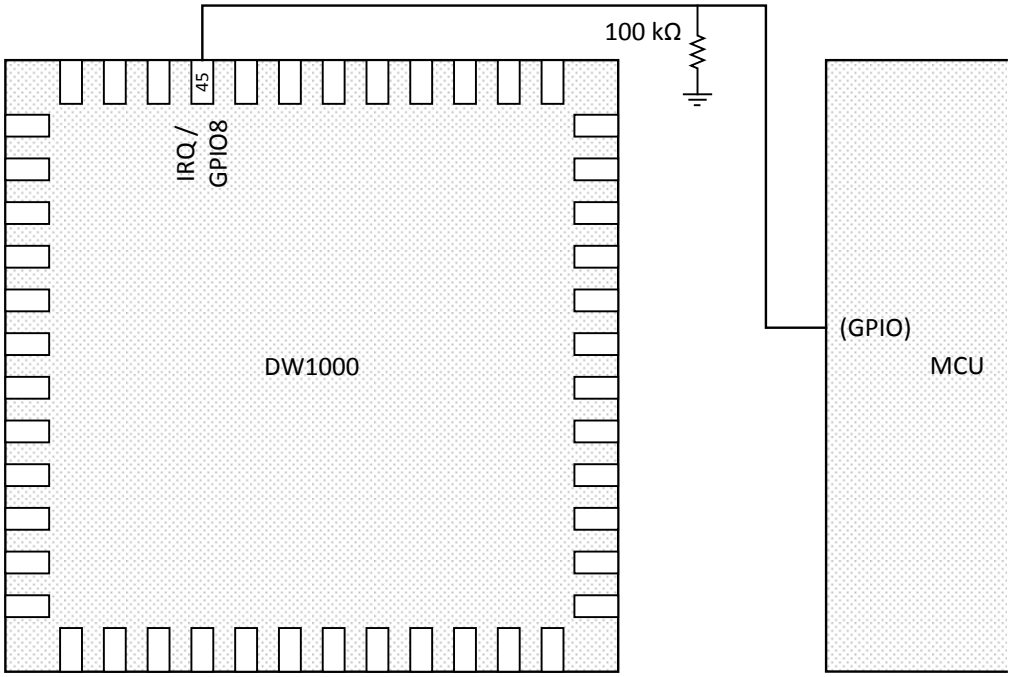



**Figure 20. External Pull-Down on IRQ Pin**

### 6.6.3 Reset Pin

The active-low, DW1000 reset (RSTn) pin is held low internally during power-up but can also be used to reset the DW1000 by pulling the pin low. The pin must not be driven high externally. Figure 21 shows a suitable solution where the microcontroller's GPIO pin is configured as open-drain, so that RSTn can be pulled low but not driven high.

Further details can be found in the DW1000 datasheet [1].

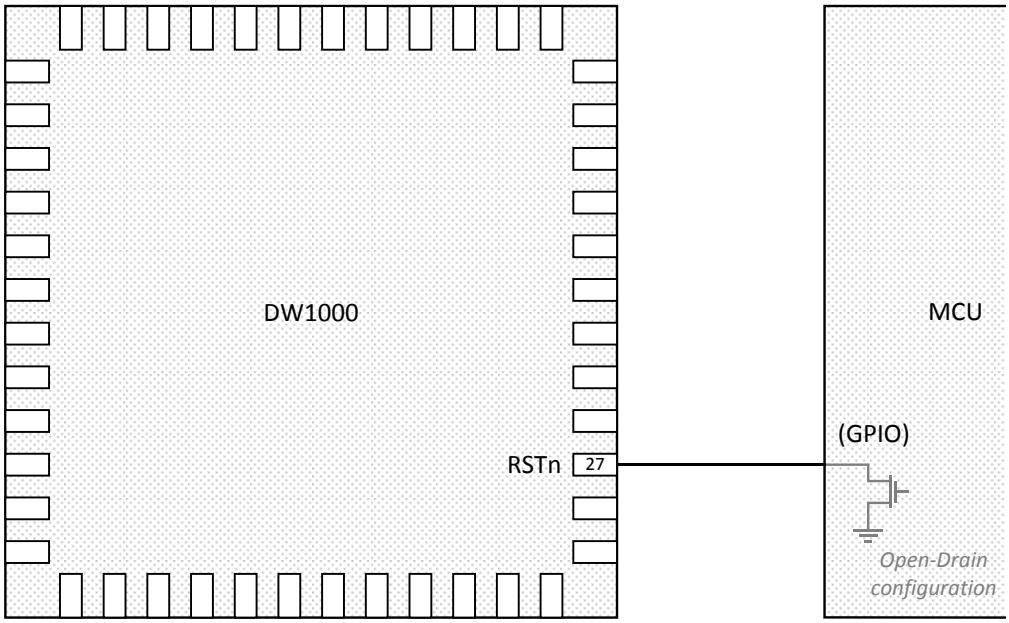



**Figure 21. Control of DW1000 RSTn Pin**

# 7 RF Connectors

## 7.1 Surface-Mount Connectors

An RF connector of some kind may be needed in the RF path in order to connect the device to test equipment for production testing.

Surface-mount connectors with the ability to switch the RF signal path from the antenna trace to the plug adapter are recommended as it is important that the stub formed from the antenna and feed trace are removed from the measurement. To ensure an accurate impedance match between the board and the adapter, there must be a low-impedance path between the board's ground plane and the adapter cable's ground shield. Place many vias in, or as close as possible to, the connector ground pads, as shown in Figure 22.

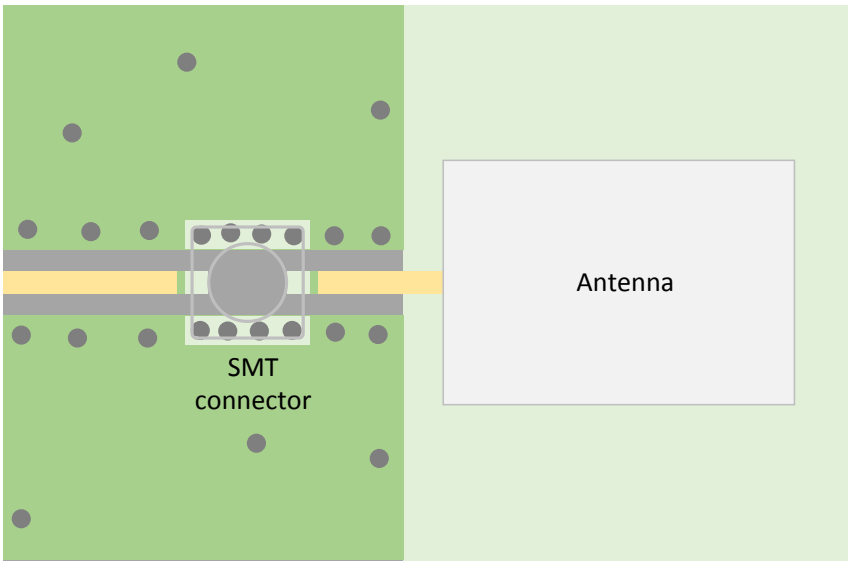



**Figure 22. SMT Antenna Connector Layout**

Some suggested coaxial switch connectors are listed in the following table.

**Table 2. Suggested Coaxial Switch Connectors**

| Vendor | Part Number | Frequency Range | Description |
|---|---|---|---|
| Hirose | MS-156C | DC to 11 GHz | Miniature coaxial switch |
| Murata | MM8030-2610 | DC to 11 GHz | Miniature coaxial switch |

## 7.2 SMA Connectors

PCB designs using SMA connectors should use edge-mount rather than through-hole connectors in order to avoid impedance discontinuities. A through-hole interconnect introduces a stub, aswell as a sharp right-angled bend in the transmission line which will result in distortion and power loss in the RF signal.

Many vias should be used within or close to the SMA connector ground pads. Since an edge-mounted SMA connector attaches to top and bottom PCB layers, through-hole vias should be used to reduce the impedance to current flowing from the connector's ground connection on the bottom layer.

Match track and connector pad widths in order to avoid impedance discontinuity, as discussed in section 3.2.

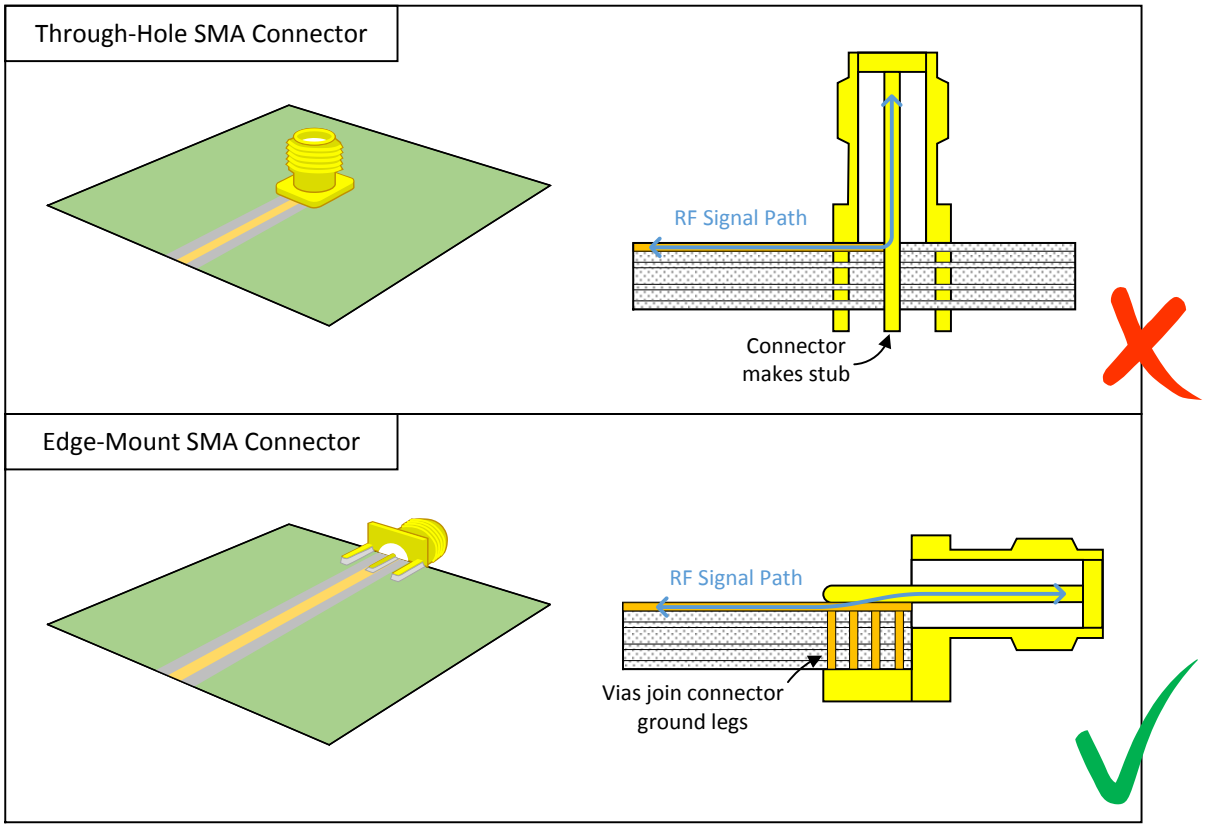



**Figure 23. Types of SMA Connector**

## 7.3 Semi-Rigid Adapters

Semi-rigid adapters (sometimes called ‘pig-tails’) are thin, copper-clad coaxial cables, with the inner conductor exposed at one end and an SMA connector attached at the other end. These adapters typically have 50 ohm characteristic impedance are useful during product development for making conducted RF measurements such as observing the transmit signal spectrum and receiver sensitivity.

The RF track may need to be cut in order to attach the inner conductor of the adapter. The length of exposed inner conductor should be minimised. Soldermask on the top layer of the PCB should be removed so that the copper shield of the adapter can be soldered to the board. The shield of the adapter should be soldered to the board as close as possible to the point where the inner conductor of the adapter is soldered to the RF track. Connections should be made to ground on either side of the RF track. By following these guidelines, the transmission line impedance from PCB to adapter can be kept as consistent as possible.

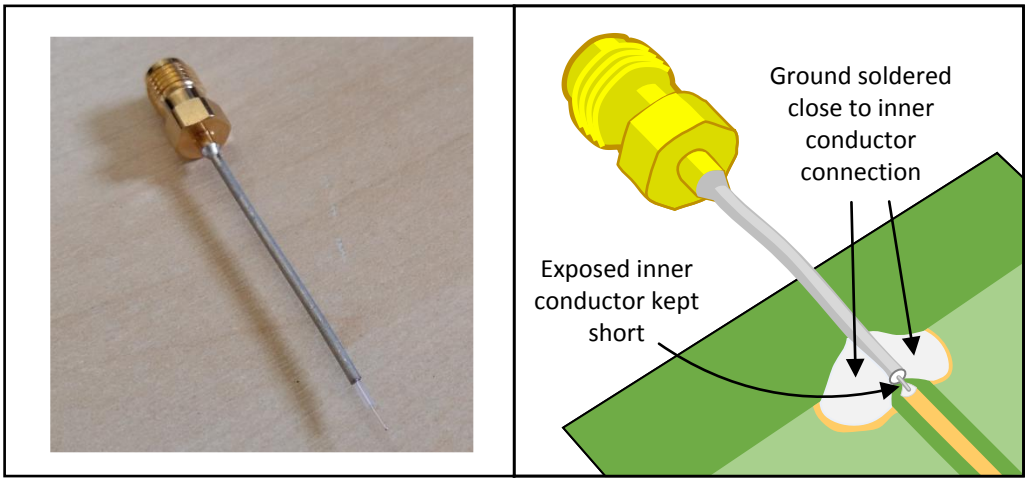



**Figure 24. Semi-Rigid Adapter and Connection to PCB**

# 8 Antennas

## 8.1 Overview

In contrast with narrowband radio systems, antennas for UWB RTLS applications need to meet additional performance specifications, such as fidelity factor and group delay.

An overview of requirements for antennas for use in DW1000-based products is presented in application note APH007 [3]. This document also addresses practical considerations such as the effect of various polymer housing enclosure materials on antenna performance.

## 8.2 Antenna Reference Designs from Decawave

### 8.2.1 WB001

Close proximity to objects with low RF-transparency can degrade antenna performance, reducing efficiency and altering radiation patterns. WB001 is designed for use in products such as body-worn tags. It is a linearly-polarised monopole antenna with a ground shorting via feature designed to have good gain across UWB channels in the 3.5 to 7 GHz frequency range. It is a planar antenna which can be implemented in copper as part of the PCB layout.

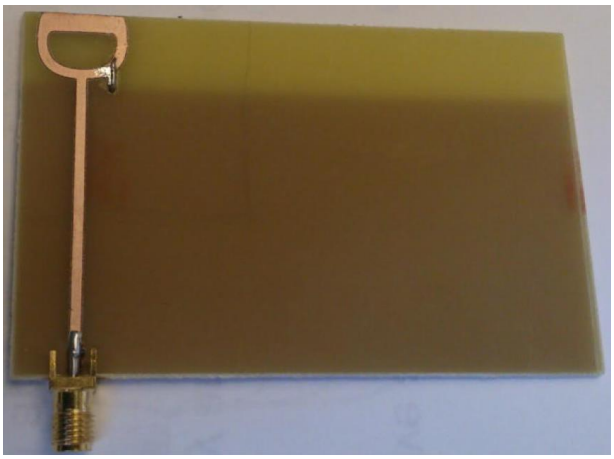


**Figure 25. WB001 Antenna**

A design document, including gerber files, can be found in the downloadable WB001 package at www.decawave.com.

### 8.2.2 WB002

WB002 is the antenna provided in Decawave EVK1000 and TREK1000 development kits and is a good antenna for use in free-space scenarios. It is a linearly-polarised monopole antenna designed to have good gain across UWB channels in the 3 to 8 GHz frequency range. It is a planar antenna which can be implemented in copper as part of the PCB layout.

**Figure 26. WB002 Antenna**

A design document, including gerber files, can be found in the downloadable WB002 package at www.decawave.com.

# 9 Electromagnetic Interference

## 9.1 Overview

It is intended that any electromagnetic radiation from a product with a radio should be from the product's antenna. In reality, however, it is found that unintentional radiation commonly occurs from structures within the product other than the radio system's antenna. Electromagnetic interference (EMI) is the name given to this kind of unintentional radiation as it can interfere with the radio signal transmitted from the antenna.

There are techniques which can be used to limit EMI originating from both the PCB and the other structures within an assembled product.

## 9.2 PCB Ground Stitching Vias

The high radio frequencies generated in a UWB transmitter can cause noise to radiate from the PCB due to a number of different mechanisms. A technique of using through-hole vias to join ground copper on all layers around the perimeter of the PCB limits the propagation of EMI from the board.

- ***EMI from Signal Traces:***
  Noise generated from RF circuits, switched-mode power regulators and digital circuitry can propagate between the copper PCB layers and emerge from the board as EMI. Ground stitching vias act as a Faraday cage, containing EMI within the board.

- ***Varying Ground Plane Potential:***
  As UWB signal wavelengths are shorter than the physical PCB dimensions, the current density profiles along the ground plane borders on different PCB layers can vary significantly, causing the edges of the board to act like dipole antennas, radiating noise from the board. Ground stitching vias reduce the potential difference between ground copper around the edges of the board.

An illustration of the positioning of ground stitching vias on a PCB is shown in Figure 27. The distance between adjacent vias should be small relative to the wavelength (λ) of the highest frequency signal on the PCB. The recommended distance is λ/20 or less.

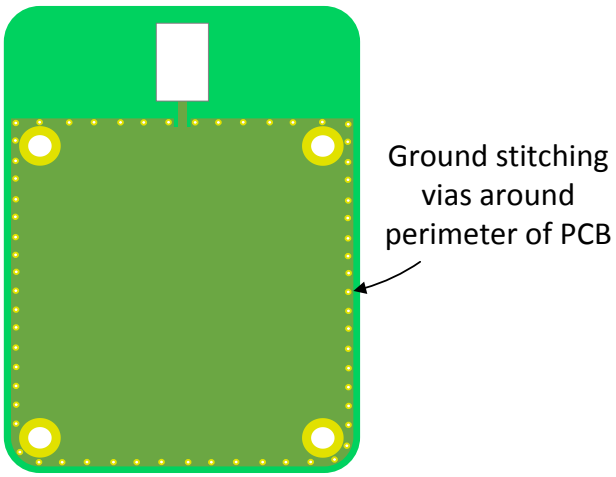



**Figure 27. Ground Stitching Vias around PCB Perimeter**

## 9.3 EMI Shield Cans

Shields cans are often used on PCB assemblies for preventing noise from being coupled between different circuit blocks on the PCB. The DW1000 has external components which are sensitive to noise, such as the crystal and PLL components, but provided they aren't placed close to noise sources, an EMI shield can may not be needed.

There are, however, some circumstances in which placing a shield can over the DW1000 circuit block may be necessary. Here are some examples.

- If the product uses another radio technology (e.g. BLE, WiFi, cellular, etc.) which can transmit when the UWB receiver is active, then UWB desensitisation due to blocking may occur.
- If noisy power supplies and digital signals are placed near the DW1000's sensitive RF circuits.
- If the PCB assembly requires protection from physical damage.
- If there are other sensitive circuit blocks on the PCB that could suffer from noise generated in the DW1000's digital circuits.

The fence of the shield can should have a section removed to form a "mousehole" where the RF track emerges, so that the impedance of the RF track isn't altered by the close proximity of the grounded shield can fence. Guideline dimensions of the mousehole would be a width equal to three times the RF track width and height equal to four times the substrate height between the track and its reference ground layer in the PCB.

Through-hole vias should be used to stitch ground copper in the layers of the PCB around the perimeter of the shield can. This improves shielding of noise which could propagate through the PCB. It also minimises impedance between shield can and ground plane, preventing shield can itself from radiating noise.

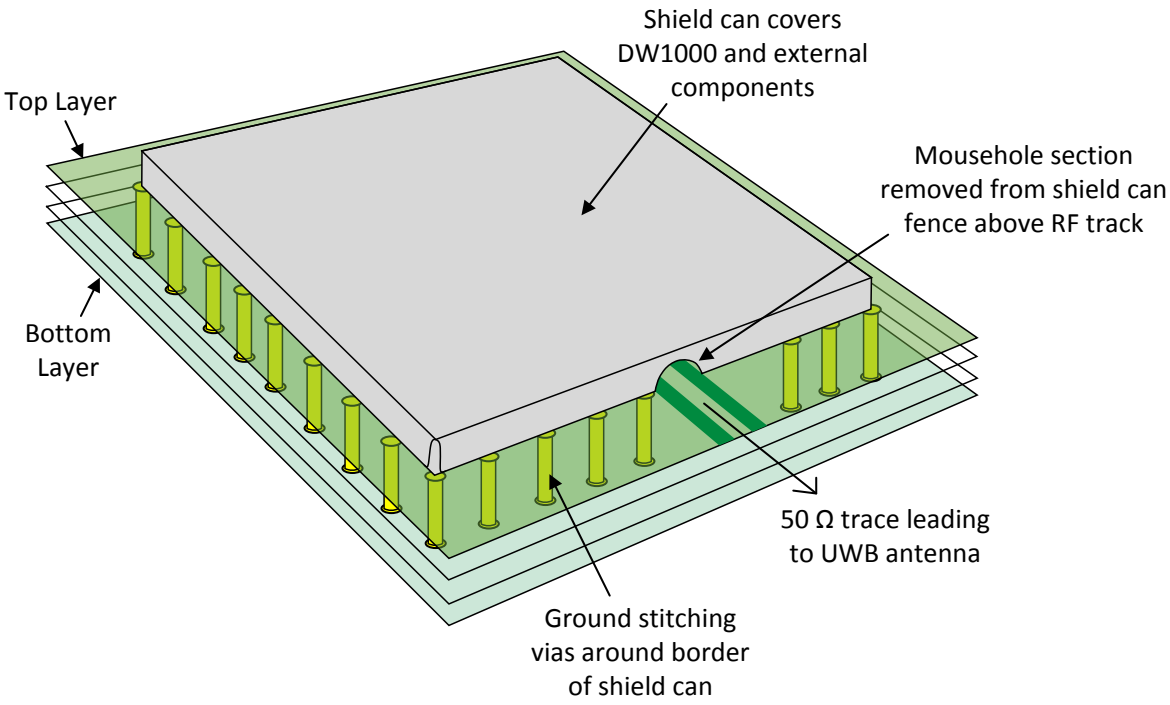



**Figure 28. EMI Shield Can**

## 9.4 EMI from PCB Interfaces

Most of the electronic components in a typical product reside on the PCB but there are usually other circuits which connect to the main PCB assembly. Often wires or flexible printed circuits (FPCs) are used to interface between the PCB and components mounted elsewhere, such as an LED display or a power button on the product's housing. Power leads are often used to connect the battery to the PCB. Consideration should be given to how both the PCB and metallic objects connected to the PCB behave when high radio frequencies are involved.

RF currents on signals and ground planes in the PCB can couple to signals routed on wires and battery leads. These conductors are often unshielded and so they can act as antennas, radiating EMI unintentionally from the product, as illustrated in Figure 29.

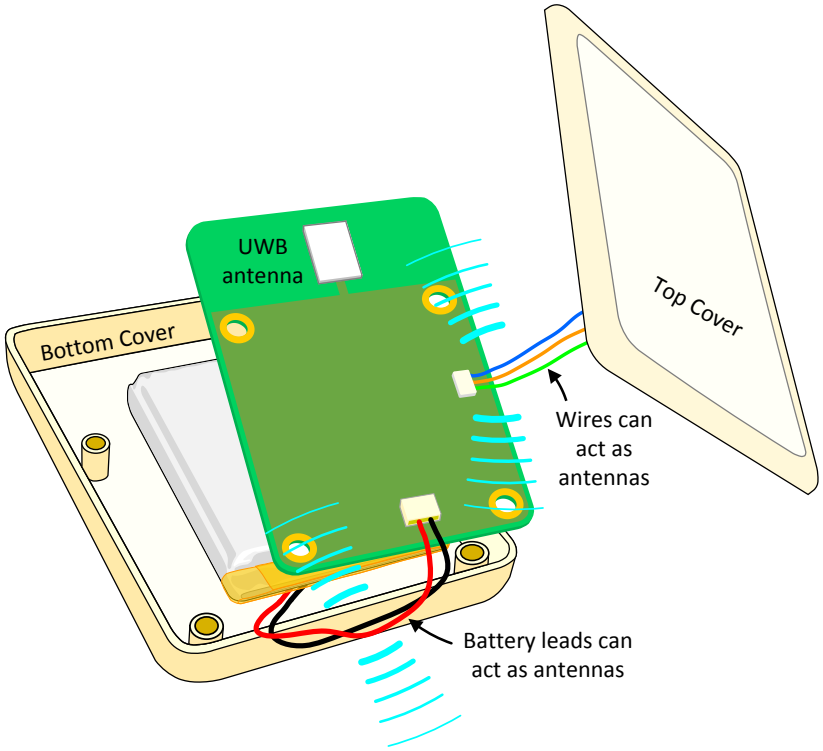



**Figure 29. Unintentional Radiation in UWB Product**

EMI can combine constructively or destructively with the energy transmitted from the UWB antenna to create a distorted UWB transmit spectrum. Figure 30 illustrates a scenario where the transmit spectrum of a UWB product is being measured. With the EMI source facing the measuring antenna, the spectrum is distorted, with a peak in power where the EMI constructively interferes with the signal from the product's antenna. When the product is in a position where the EMI source is facing away from the measuring antenna, the EMI is much weaker and the measured power is well below the regulatory limit. The product's power must be set lower to allow for the peak seen due to the EMI source. This demonstrates how EMI can lead to reduced communication range aswell as ranging inaccuracies associated with varying power being transmitted in a 360° plane around the product.

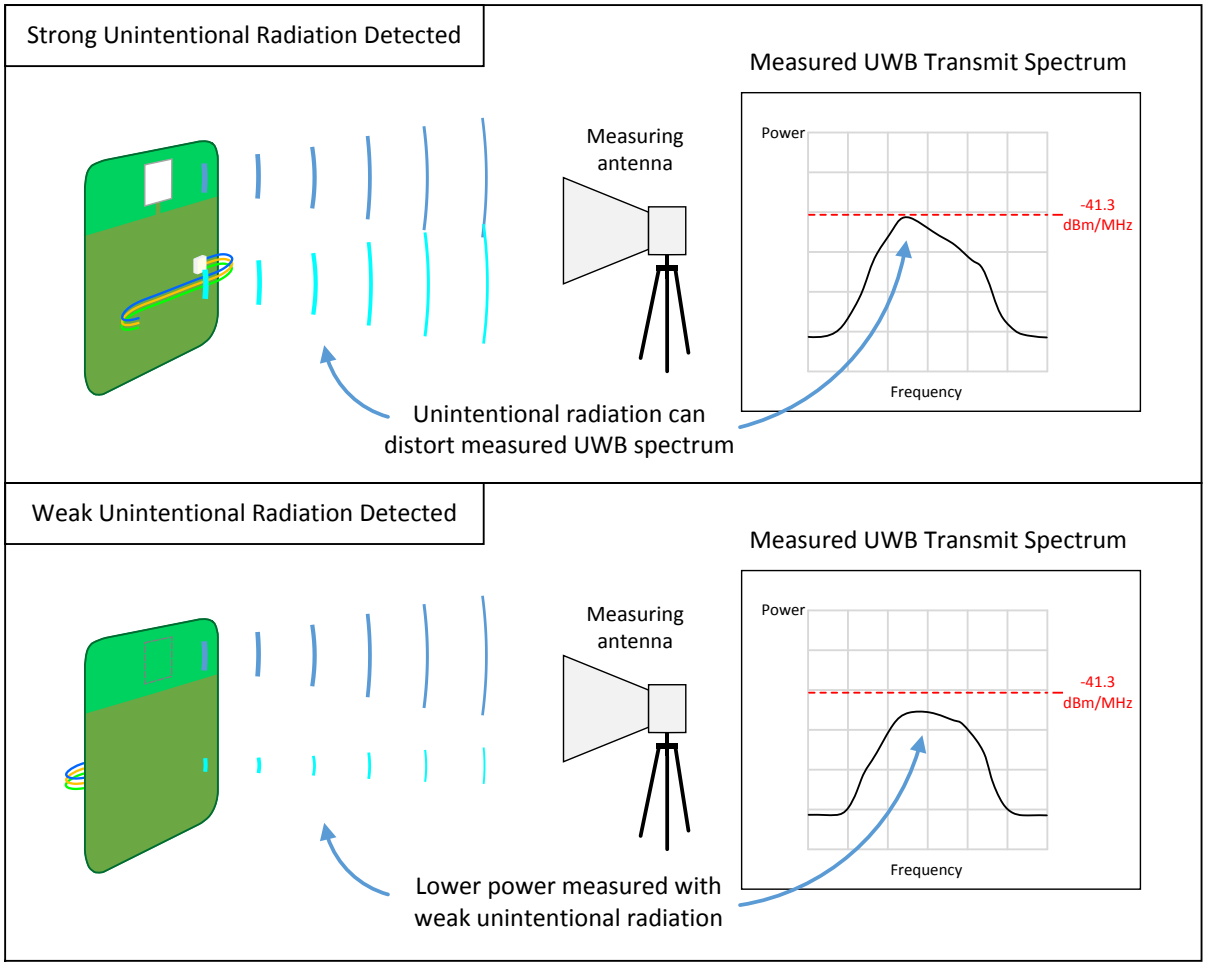



**Figure 30. Effect of Unintentional Radiation on Transmit Spectrum Measurements**

Follow these guidelines for limiting EMI from wire and battery PCB interfaces.

- Keep wires as short as possible. This will limit their ability to radiate EMI.
- Try to position wires so that they run close to the surface of the PCB ground plane. EMI radiating from the wires can be reduced through coupling to the ground plane.
- Try placing ferrites or decoupling capacitors to decouple noise on the PCB at the wire interface connection. This will filter noise before reaching the wires.
- Electromagnetic absorber sheet material or EMI cloth can be positioned on wires so that noise can be absorbed rather than radiated.
- Use battery terminals rather than leads if possible.

# 10 References

## *10.1 Listing*

Reference is made to the following documents in the course of this Application Note: -

**Table 3. Table of References**

| Ref | Author | Version | Title |
|---|---|---|---|
| [1] | Decawave | Current | DW1000 Datasheet |
| [2] | Decawave | Current | DW1000 User Manual |
| [3] | Decawave | Current | APH007 Antenna Selection / Design Guide for DW1000 |

# 11 Document History

**Table 4. Document History**

| Revision | Date | Description |
|---|---|---|
| 1.0 | 30th September 2016 | Initial release. |

# 12 Major Changes

**Revision 1.0**

| Page | Change Description |
|---|---|
| All | Initial release. |

# 13 About Decawave

Decawave is a pioneering fabless semiconductor company whose flagship product, the DW1000, is a complete, single chip CMOS Ultra-Wideband IC based on the IEEE 802.15.4-2011 UWB standard. This device is the first in a family of parts that will operate at data rates of 110 kbps, 850 kbps and 6.8 Mbps.

The resulting silicon has a wide range of standards-based applications for both Real Time Location Systems (RTLS) and Ultra Low Power Wireless Transceivers in areas as diverse as manufacturing, healthcare, lighting, security, transport, inventory & supply chain management.

**Further Information**

For further information on this or any other Decawave product contact a sales representative as follows: -

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Adelaide Chambers
Peter Street
Dublin 8
t: +353 1 697 5030
e: sales@decawave.com
w: www.decawave.com

# 14 Appendix A: Advantages of Using Microvias and More PCB Layers

For designs requiring more functionality in very small form factors, it may be worth having an increased number of PCB layers. With more layers, there is more vertical space for escape routing and it is easier to keep space adjacent to the DW1000 free of routing, so that a physically smaller board can be produced. The drawback of having more layers is that production time and cost are also higher.

Figure 31 illustrates an example 6-layer PCB stack-up where a high component density is possible for several reasons.

- With 6 layers in the stack-up, there is enough routing space for ICs to be placed opposite each other on top and bottom sides of the PCB.
- In addition to plated through-hole vias which are drilled through all 6 layers, the use of blind microvias between the top and bottom two layers greatly eases escape routing.
- Using via-in-pad technology, where the via can be placed within component pads as opposed to adjacent to the pad, offers board space savings. As no soldermask is applied over component pads, vias need to be filled with epoxy or copper to avoid air entrapment and outgassing during assembly, adding additional cost.

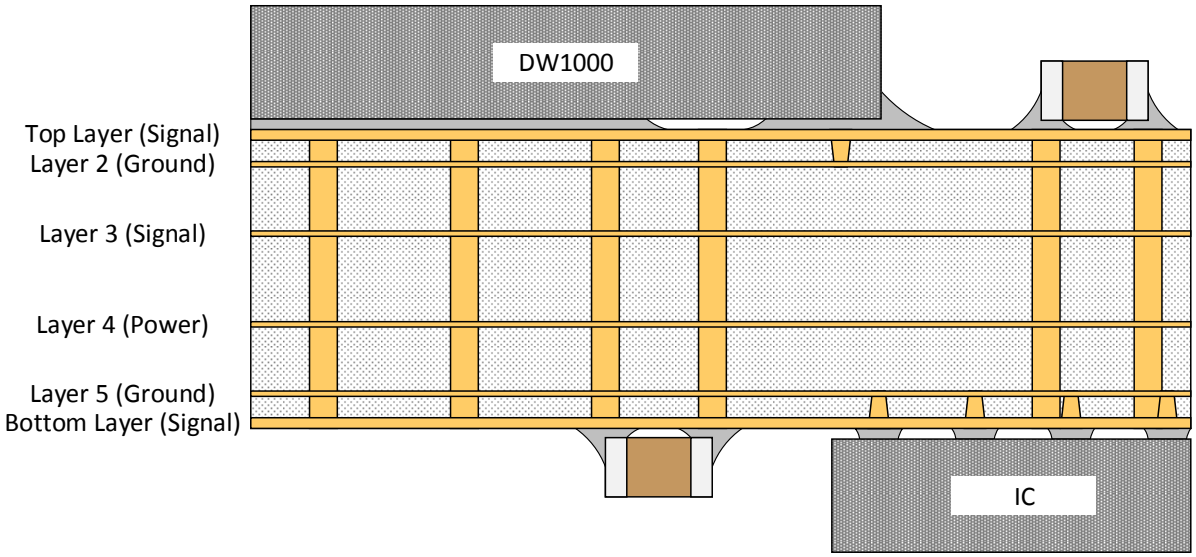


**Figure 31. High Component Density with 6 PCB Layers and Microvias**

# 15 Appendix B: EVB1000 PCB Layout .dxf Files

## *15.1 Introduction*

To assist customers with PCB layout of a DW1000 based product, three files in DXF format are available from Decawave. These DXF files can be imported in most PCB layout EDA tools and used as an overlay to replicate the DW1000 section of Decawave's EVB1000 evaluation boards.

Note: In order to maintain the correct impedances of the RF tracks, the PCB stack up shown in section 3.3 should be used. However, customers should consult their PCB manufacturer to fine tune impedances. During PCB manufacture, impedance control techniques should be employed to ensure that the RF tracks have the correct impedance. This is required because of the variability of laminate parameters with standard FR4 material.

## *15.2 Files Supplied*

In total 4 files are supplied. One is an image file for reference and the other three are DXF files.

### 15.2.1 DW1000 section of EVB1000 layout

**File name:** EVB1000_DW1000_section.png

**Description**: This file is an image of the DW1000 section of Decawave's EVB1000 board for reference.

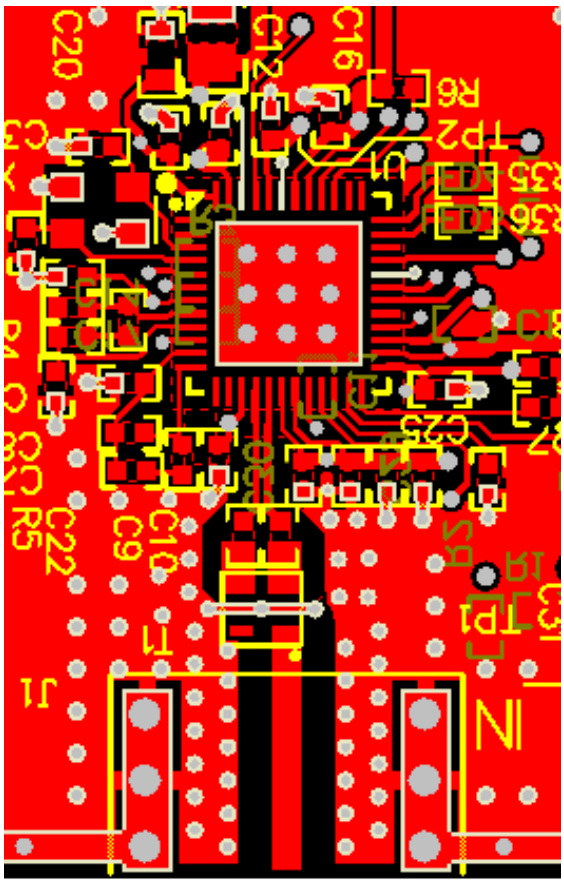


**Figure 32. Image of DW1000 Section of EVB1000 for Reference**

### 15.2.2 Top Side Copper

**Filename:** DW1000_IC_PCB_TopCopperOnly.dxf

**Description**: This file shows how the topside tracks and ground plane are constructed on the DW1000 section of the EVB1000 PCB. This is the main file of interest.

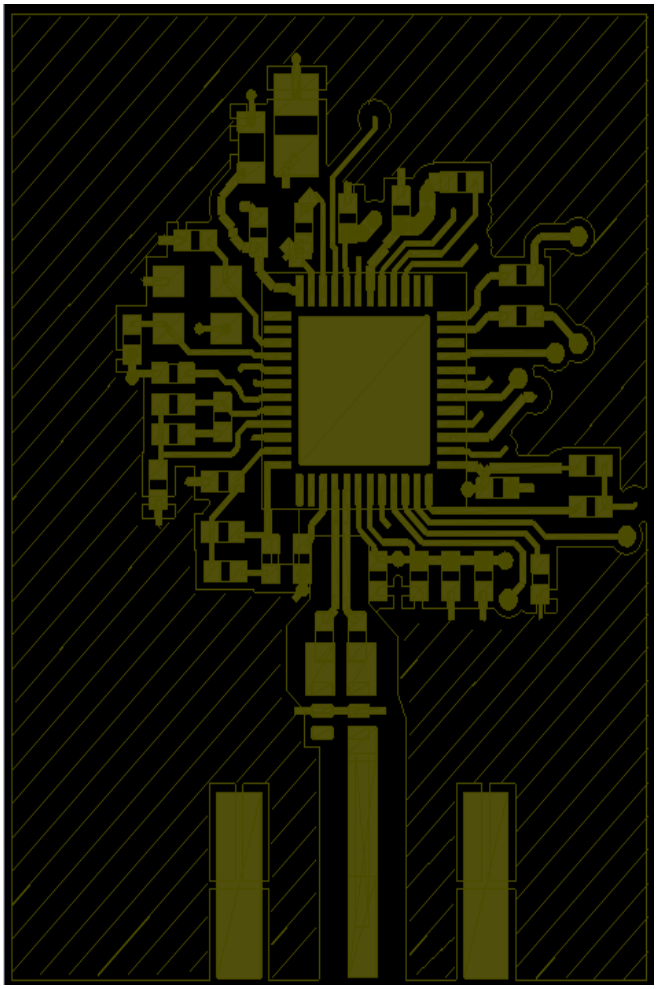

**Figure 33: Top Side Copper of DW1000 Section of EVB1000**

### 15.2.3 Top Side Resist

**Filename:** DW1000_IC_PCB_TopResistOnly.dxf

**Description**: This file shows how the top side solder resist (mask) is applied to the DW1000 section of the EVB1000 PCB. Note: We do not recommend applying solder resist on the RF traces. This helps ensure that the correct RF impedance is maintained. In order to stop solder flowing onto these tracks during the solder reflow process, slivers of resist as shown are used.

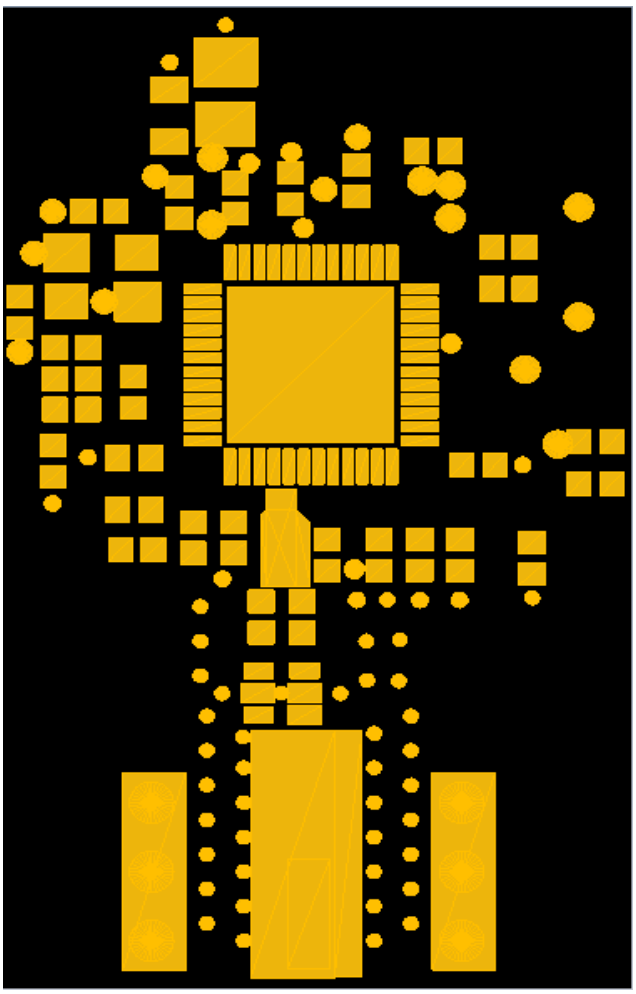

**Figure 34: Top side Resist of DW1000 Section of EVB1000**

### 15.2.4 Top Side Silk Screen

**Filename:** DW1000_IC_PCB_TopSilkscreenOnly.dxf

**Description**: This file shows the top side silk screen of the DW1000 section of EVB1000 for reference.

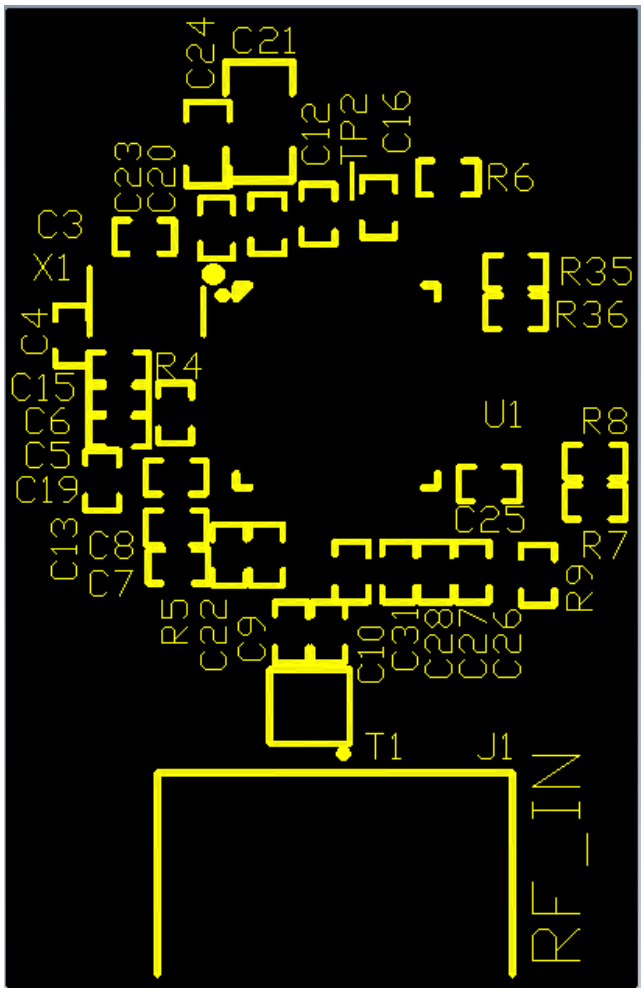


**Figure 35. Top Side Silk Screen of DW1000 Section of EVB1000**