```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                    2 ************************************************************************
                                                    3 *
                                                    4 *        EXPERIMENTAL pending further PoP definition
                                                    5 *
                                                    6 *        Zvector E6 instruction tests for VRR-a encoded:
                                                    7 *
                                                    8 *        E655 VCNF     - VECTOR FP CONVERT TO NNP
                                                    9 *        E656 VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                   10 *        E65D VCFN     - VECTOR FP CONVERT FROM NNP
                                                   11 *        E65E VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                   12 *
                                                   13 *        and partial testing of
                                                   14 *
                                                   15 *        E675  VCRNF   - VECTOR FP CONVERT AND ROUND TO NNP
                                                   16 *
                                                   17 *        during cross check tests for VCLFNH and VCLFNL
                                                   18 *
                                                   19 *        James Wekel August 2024
                                                   20 ************************************************************************


                                                   22 ************************************************************************
                                                   23 *
                                                   24 *        basic instruction tests
                                                   25 *
                                                   26 ************************************************************************
                                                   27 *  This program tests EXPERIMENTAL functioning of the z/arch E6 VRR-a
                                                   28 *  Neural-network-processing-assist facility vector instructions.
                                                   29 *  These test are EXPERIMENTAL pending further PoP definition of
                                                   30 *  NNP-data-type-1.
                                                   31 *
                                                   32 *  If requested and if VXC == 0 after test instruction execution,
                                                   33 *  a cross check test is performed. A cross check uses the result
                                                   34 *  of the instruction test to recreate the test source.
                                                   35 *
                                                   36 *  Exceptions (including trapable IEEE exceptions) are not tested.
                                                   37 *
                                                   38 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                   39 *  obvious coding errors.  None of the tests are thorough.  They are
                                                   40 *  NOT designed to test all aspects of any of the instructions.
                                                   41 *
                                                   42 ************************************************************************
                                                   43 *
                                                   44 *    *Testcase zvector-e6-20-NNPconvert
                                                   45 *    *
                                                   46 *    *   EXPERIMENTAL pending further PoP definition
                                                   47 *    *
                                                   48 *    *   Zvector E6 instruction tests for VRR-a encoded:
                                                   49 *    *
                                                   50 *    *   E655 VCNF     - VECTOR FP CONVERT TO NNP
                                                   51 *    *   E656 VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                   52 *    *   E65D VCFN     - VECTOR FP CONVERT FROM NNP
                                                   53 *    *   E65E VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                   54 *    *
                                                   55 *    *   # ------------------------------------------------------
                                                   56 *    *   #  This tests only the basic function of the instruction.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                    57 *    *   #  Exceptions are NOT tested.
                                                    58 *    *   # ------------------------------------------------------------
                                                    59 *    *
                                                    60 *    mainsize    2
                                                    61 *    numcpu      1
                                                    62 *    sysclear
                                                    63 *    archlvl     z/Arch
                                                    64 *
                                                    65 *    loadcore    "$(testpath)/zvector-e6-20-NNPconvert.core" 0x0
                                                    66 *
                                                    67 *    diag8cmd    enable    # (needed for messages to Hercules console)
                                                    68 *    runtest 2
                                                    69 *    diag8cmd    disable   # (reset back to default)
                                                    70 *
                                                    71 *    *Done
                                                    72 *
                                                    73 ***********************************************************************
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   75 ************************************************************************
                                                   76 *        FCHECK Macro - Is a Facility Bit set?
                                                   77 *
                                                   78 *        If the facility bit is NOT set, an message is issued and
                                                   79 *        the test is skipped.
                                                   80 *
                                                   81 *        Fcheck uses R0, R1 and R2
                                                   82 *
                                                   83 * eg.    FCHECK 134,'vector-packed-decimal'
                                                   84 ************************************************************************
                                                   85          MACRO
                                                   86          FCHECK &BITNO,&NOTSETMSG
                                                   87 .*                       &BITNO : facility bit number to check
                                                   88 .*                       &NOTSETMSG : 'facility name'
                                                   89          LCLA  &FBBYTE           Facility bit in Byte
                                                   90          LCLA  &FBBIT            Facility bit within Byte
                                                   91
                                                   92          LCLA  &L(8)
                                                   93 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                   94
                                                   95 &FBBYTE  SETA  &BITNO/8
                                                   96 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                   97 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                   98
                                                   99          B     X&SYSNDX
                                                  100 *                                       Fcheck data area
                                                  101 *                                       skip messgae
                                                  102 SKT&SYSNDX DC  C'          Skipping tests: '
                                                  103          DC    C&NOTSETMSG
                                                  104          DC    C' facility (bit &BITNO) is not installed.'
                                                  105 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                  106 *                                       facility bits
                                                  107          DS    FD                      gap
                                                  108 FB&SYSNDX DS   4FD
                                                  109          DS    FD                      gap
                                                  110 *
                                                  111 X&SYSNDX EQU *
                                                  112          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                  113          STFLE FB&SYSNDX               get facility bits
                                                  114
                                                  115          XGR   R0,R0
                                                  116          IC    R0,FB&SYSNDX+&FBBYTE    get fbit byte
                                                  117          N     R0,=F'&FBBIT'           is bit set?
                                                  118          BNZ   XC&SYSNDX
                                                  119 *
                                                  120 * facility bit not set, issue message and exit
                                                  121 *
                                                  122          LA    R0,SKL&SYSNDX           message length
                                                  123          LA    R1,SKT&SYSNDX           message address
                                                  124          BAL   R2,MSG
                                                  125
                                                  126          B     EOJ
                                                  127 XC&SYSNDX EQU *
                                                  128          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   130 ************************************************************************
                                                   131 *        Low core PSWs
                                                   132 ************************************************************************


                             00000000  000055D7   134 ZVE6TST  START 0
00000000                     00000000              135          USING ZVE6TST,R0            Low core addressability
                                                   136
                             00000140  00000000   137 SVOLDPSW EQU   ZVE6TST+X'140'        z/Arch Supervisor call old PSW


00000000                     00000000  000001A0   139          ORG   ZVE6TST+X'1A0'        z/Architecture RESTART PSW
000001A0  00000001 80000000                        140          DC    X'0000000180000000'
000001A8  00000000 00000200                        141          DC    AD(BEGIN)


000001B0                     000001B0  000001D0   143          ORG   ZVE6TST+X'1D0'        z/Architecture PROGRAM CHECK PSW
000001D0  00020001 80000000                        144          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                        145          DC    AD(X'DEAD')


000001E0                     000001E0  00000200   147          ORG   ZVE6TST+X'200'        Start of actual test program...
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    149
                                                    150 ************************************************************************
                                                    151 *                The actual "ZVE6TST" program itself...
                                                    152 ************************************************************************
                                                    153 *
                                                    154 *  Architecture Mode: z/Arch
                                                    155 *  Register Usage:
                                                    156 *
                                                    157 *   R0       (work)
                                                    158 *   R1-4     (work)
                                                    159 *   R5       Testing control table - current test base
                                                    160 *   R6       (work)
                                                    161 *   R7       msg return
                                                    162 *   R8       First base register
                                                    163 *   R9       Second base register
                                                    164 *   R10      Third base register
                                                    165 *   R11      E6TEST call return
                                                    166 *   R12      E6TESTS register
                                                    167 *   R13      (work)
                                                    168 *   R14      Subroutine call
                                                    169 *   R15      Secondary Subroutine call or work
                                                    170 *
                                                    171 ************************************************************************

00000200                       00000200             173          USING  BEGIN,R8               FIRST Base Register
00000200                       00001200             174          USING  BEGIN+4096,R9          SECOND Base Register
00000200                       00002200             175          USING  BEGIN+8192,R10         THIRD Base Register
                                                    176
00000200  0580                                      177 BEGIN    BALR   R8,0                   Initialize FIRST base register
00000202  0680                                      178          BCTR   R8,0                   Initialize FIRST base register
00000204  0680                                      179          BCTR   R8,0                   Initialize FIRST base register
                                                    180
00000206  4190 8800                     00000800    181          LA     R9,2048(,R8)           Initialize SECOND base register
0000020A  4190 9800                     00000800    182          LA     R9,2048(,R9)           Initialize SECOND base register
                                                    183
0000020E  41A0 9800                     00000800    184          LA     R10,2048(,R9)          Initialize THIRD base register
00000212  41A0 A800                     00000800    185          LA     R10,2048(,R10)         Initialize THIRD base register
                                                    186
00000216  B600 859C                     0000079C    187          STCTL  R0,R0,CTLR0            Store CR0 to enable AFP
0000021A  9604 859D                     0000079D    188          OI     CTLR0+1,X'04'          Turn on AFP bit
0000021E  9602 859D                     0000079D    189          OI     CTLR0+1,X'02'          Turn on Vector bit
00000222  B700 859C                     0000079C    190          LCTL   R0,R0,CTLR0            Reload updated CR0
                                                    191
                                                    192 ************************************************************************
                                                    193 * Is Neural-network-processing-assist facility 2 installed  (bit 165)
                                                    194 ************************************************************************
                                                    195
                                                    196          FCHECK 165,'Neural-network-processing-assist'
00000226  47F0 80C0                     000002C0    197+         B      X0001
                                                    198+*                                        Fcheck data area
                                                    199+*                                        skip messgae
0000022A  40404040 40404040                         200+SKT0001  DC     C'          Skipping tests: '
00000244  D585A499 81936095                         201+         DC     C'Neural-network-processing-assist'
00000264  40868183 899389A3                         202+         DC     C' facility (bit 165) is not installed.'
                               0000005F  00000001   203+SKL0001  EQU    *-SKT0001
                                                    204+*                                        facility bits
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00000290  00000000 00000000                        205+         DS    FD                      gap
00000298  00000000 00000000                        206+FB0001   DS    4FD
000002B8  00000000 00000000                        207+         DS    FD                      gap
                                                   208+*
                             000002C0  00000001    209+X0001    EQU   *
000002C0  4100 0004                    00000004    210+         LA    R0,((X0001-FB0001)/8)-1
000002C4  B2B0 8098                    00000298    211+         STFLE FB0001                  get facility bits
000002C8  B982 0000                                212+         XGR   R0,R0
000002CC  4300 80AC                    000002AC    213+         IC    R0,FB0001+20            get fbit byte
000002D0  5400 85D8                    000007D8    214+         N     R0,=F'4'                is bit set?
000002D4  4770 80E8                    000002E8    215+         BNZ   XC0001
                                                   216+*
                                                   217+* facility bit not set, issue message and exit
                                                   218+*
000002D8  4100 005F                    0000005F    219+         LA    R0,SKL0001              message length
000002DC  4110 802A                    0000022A    220+         LA    R1,SKT0001              message address
000002E0  4520 84B0                    000006B0    221+         BAL   R2,MSG
000002E4  47F0 8580                    00000780    222+         B     EOJ
                             000002E8  00000001    223+XC0001   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   225 ***********************************************************************
                                                   226 *               Do tests in the E6TESTS table
                                                   227 ***********************************************************************
                                                   228
000002E8  58C0 85DC                      000007DC  229          L     R12,=A(E6TESTS)        get table of test addresses
                                                   230
                                 000002EC  00000001 231 NEXTE6   EQU   *
000002EC  5850 C000                      00000000  232          L     R5,0(0,R12)            get test address
000002F0  1255                                     233          LTR   R5,R5                     have a test?
000002F2  4780 846C                      0000066C  234          BZ    ENDTEST                      done?
                                                   235
000002F6                         00000000          236          USING E6TEST,R5
                                                   237
000002F6  4800 5004                      00000004  238          LH    R0,TNUM                save current test number
000002FA  5000 8E04                      00001004  239          ST    R0,TESTING             for easy reference
                                                   240
000002FE  58B0 5000                      00000000  241          L     R11,TSUB               get address of test routine
00000302  05BB                                     242          BALR  R11,R11                do test
                                                   243
00000304  45F0 813C                      0000033C  244          BAL   R15,XCHECK
                                                   245 *
                                                   246 * validate FPC first
                                                   247 *
00000308  D500 500A 5041                 00000041  248          CLC   FLG(1),FPC_R+1          expected FPC flags?
0000030E  4780 8116                      00000316  249          BE    CHECKVXC
00000312  4570 8310                      00000510  250          BAL   R7,FPCMSG               no, issue failed message
                                                   251
                                 00000316  00000001 252 CHECKVXC EQU   *
00000316  D500 500B 5042                 00000042  253          CLC   VXC(1),FPC_R+2          expected VXC?
0000031C  4780 8124                      00000324  254          BE    CHECKRES
00000320  4570 8382                      00000582  255          BAL   R7,VXCMSG               no, issue failed message
                                                   256
                                 00000324  00000001 257 CHECKRES EQU   *
                                                   258
                                                   259 * then validate results, if not inexact
                                                   260
                                                   261 *         XGR   R1,R1
                                                   262 *         IC    R1,FPC_R+1             FPC flags
                                                   263 *         N     R1,=XL4'00000008'      check inexact flag
                                                   264 *         LTR   R1,R1
                                                   265 *         BNZ   DONEXT
                                                   266
00000324  E310 501C 0014                 0000001C  267          LGF   R1,READDR              expected result address
0000032A  D50F 5028 1000         00000028  00000000 268          CLC   V1OUTPUT,0(R1)
00000330  4770 83F4                      000005F4  269          BNE   FAILMSG                no, issue failed message
                                                   270
                                 00000334  00000001 271 DONEXT   EQU   *
00000334  41C0 C004                      00000004  272          LA    R12,4(0,R12)           next test address
00000338  47F0 80EC                      000002EC  273          B     NEXTE6
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   275 *-----------------------------------------------------------------------
                                                   276 * cross check that the result can be converted back to the source
                                                   277 * where there were NO exceptions (DXC/VXC = 0)
                                                   278 *-----------------------------------------------------------------------
                                0000033C  00000001 279 XCHECK   EQU   *
0000033C  D207 5050 85A8        00000050  000007A8 280          MVC   SKIPXC,=CL8'SKIP XC '
00000342  D500 5007 85E8        00000007  000007E8 281          CLC   XCSKIP,=CL1'S'          skip xcheck requested
00000348  478F 0000                       00000000 282          BE    0(R15)                  skip = S, so exit
0000034C  9500 5042                       00000042 283          CLI   FPC_R+2,0               Only Xcheck no VXC error
00000350  477F 0000                       00000000 284          BNZ   0(R15)                  some VXC error , so exit
                                                   285 *
                                                   286 *        cross check depends on the instruction
                                                   287 *
00000354  D207 5050 85B0        00000050  000007B0 288          MVC   SKIPXC,=CL8'        '
0000035A  D507 5010 85B8        00000010  000007B8 289          CLC   OPNAME,=CL8'VCNF'
00000360  4780 818C                       0000038C 290          BE    XCVCNF
                                                   291
00000364  D507 5010 85C0        00000010  000007C0 292          CLC   OPNAME,=CL8'VCLFNH'
0000036A  4780 81C0                       000003C0 293          BE    XCVCLFNH
                                                   294
0000036E  D507 5010 85C8        00000010  000007C8 295          CLC   OPNAME,=CL8'VCFN'
00000374  4780 81F4                       000003F4 296          BE    XCVCFN
                                                   297
00000378  D507 5010 85D0        00000010  000007D0 298          CLC   OPNAME,=CL8'VCLFNL'
0000037E  4780 8228                       00000428 299          BE    XCVCLFNL
                                                   300
00000382  D207 5050 85A8        00000050  000007A8 301          MVC   SKIPXC,=CL8'SKIP XC '
00000388  07FF                                     302          BR    R15                     return from xcheck
                                                   303
                                                   304 * cross check: VCNF     - VECTOR FP CONVERT TO NNP
                                                   305 *
0000038C                                           306 XCVCNF   DS    0F
0000038C  B29D 85A4                       000007A4 307          LFPC  FPCINIT                 initialize FPC
                                                   308
00000390  E700 5028 0806                  00000028 309          VL    V16,V1OUTPUT
00000396  E6F0 0000 145D                           310          VCFN  V15,V16,1,0
0000039C  B29C 5078                       00000078 311          STFPC FPC_XC                  save FPC
000003A0  E7F0 5060 000E                  00000060 312          VST   V15,XCOUTPUT
                                                   313
000003A6  9500 507A                       0000007A 314          CLI   FPC_XC+2,0
000003AA  477F 0000                       00000000 315          BNZ   0(R15)                  some VXC error , so exit
                                                   316
000003AE  E310 500C 0014                  0000000C 317          LGF   R1,V2ADDR               expected source address
000003B4  D50F 5060 1000        00000060  00000000 318          CLC   XCOUTPUT,0(R1)
000003BA  4770 825C                       0000045C 319          BNE   XCFAILMSG
000003BE  07FF                                     320          BR    R15                     return from xcheck
                                                   321
                                                   322 * cross check: VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                   323 *
000003C0                                           324 XCVCLFNH DS    0F
000003C0  B29D 85A4                       000007A4 325          LFPC  FPCINIT                 initialize FPC
                                                   326
000003C4  E700 5028 0806                  00000028 327          VL    V16,V1OUTPUT
000003CA  E6F0 0002 0675                           328          VCRNF V15,V16,V16,0,2
000003D0  B29C 5078                       00000078 329          STFPC FPC_XC                  save FPC
000003D4  E7F0 5060 000E                  00000060 330          VST   V15,XCOUTPUT
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   331
000003DA  9500 507A                     0000007A   332          CLI   FPC_XC+2,0
000003DE  477F 0000                     00000000   333          BNZ   0(R15)                  some VXC error , so exit
                                                   334
000003E2  E310 500C 0014                0000000C   335          LGF   R1,V2ADDR              expected source address
000003E8  D507 5060 1000                00000000   336          CLC   XCOUTPUT(8),0(R1)
000003EE  4770 825C                     0000045C   337          BNE   XCFAILMSG
000003F2  07FF                                     338          BR    R15                    return from xcheck
                                                   339
                                                   340 * cross check: VCFN     - VECTOR FP CONVERT FROM NNP
                                                   341 *
000003F4                                           342 XCVCFN   DS    0F
000003F4  B29D 85A4                     000007A4   343          LFPC  FPCINIT                initialize FPC
                                                   344
000003F8  E700 5028 0806                00000028   345          VL    V16,V1OUTPUT
000003FE  E6F0 0001 0455                           346          VCNF  V15,V16,0,1
00000404  B29C 5078                     00000078   347          STFPC FPC_XC                 save FPC
00000408  E7F0 5060 000E                00000060   348          VST   V15,XCOUTPUT
                                                   349
0000040E  9500 507A                     0000007A   350          CLI   FPC_XC+2,0
00000412  477F 0000                     00000000   351          BNZ   0(R15)                  some VXC error , so exit
                                                   352
00000416  E310 500C 0014                0000000C   353          LGF   R1,V2ADDR              expected source address
0000041C  D50F 5060 1000      00000060  00000000   354          CLC   XCOUTPUT,0(R1)
00000422  4770 825C                     0000045C   355          BNE   XCFAILMSG
00000426  07FF                                     356          BR    R15                    return from xcheck
                                                   357
                                                   358 * cross check: VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                   359 *
00000428                                           360 XCVCLFNL DS    0F
00000428  B29D 85A4                     000007A4   361          LFPC  FPCINIT                initialize FPC
                                                   362
0000042C  E700 5028 0806                00000028   363          VL    V16,V1OUTPUT
00000432  E6F0 0002 0675                           364          VCRNF V15,V16,V16,0,2
00000438  B29C 5078                     00000078   365          STFPC FPC_XC                 save FPC
0000043C  E7F0 5060 000E                00000060   366          VST   V15,XCOUTPUT
                                                   367
00000442  9500 507A                     0000007A   368          CLI   FPC_XC+2,0
00000446  477F 0000                     00000000   369          BNZ   0(R15)                  some VXC error , so exit
                                                   370
0000044A  E310 500C 0014                0000000C   371          LGF   R1,V2ADDR              expected source address
00000450  D507 5060 1008                00000008   372          CLC   XCOUTPUT(8),8(R1)      low part of vector
00000456  4770 825C                     0000045C   373          BNE   XCFAILMSG
0000045A  07FF                                     374          BR    R15                    return from xcheck
                                                   375
                                                   376
                                                   377 * xcheck failed message
0000045C                                           378 XCFAILMSG DS   0H
0000045C  4820 5004                     00000004   379          LH    R2,TNUM                get test number and convert
00000460  4E20 8F90                     00001190   380          CVD   R2,DECNUM
00000464  D211 8F7A 8F64      0000117A  00001164   381          MVC   PRT3,EDIT
0000046A  DE11 8F7A 8F90      0000117A  00001190   382          ED    PRT3,DECNUM
00000470  D202 8F23 8F87      00001123  00001187   383          MVC   XCPTNUM(3),PRT3+13     fill in message with test #
                                                   384
00000476  D207 8F45 5010      00001145  00000010   385          MVC   XCPNAME,OPNAME         fill in message with instruction
                                                   386
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000047C  B982 0022                               387          XGR   R2,R2
00000480  4320 5008                     00000008  388          IC    R2,M3                  get m3 and convert
00000484  4E20 8F90                     00001190  389          CVD   R2,DECNUM
00000488  D211 8F7A 8F64      0000117A  00001164  390          MVC   PRT3,EDIT
0000048E  DE11 8F7A 8F90      0000117A  00001190  391          ED    PRT3,DECNUM
00000494  D201 8F56 8F88      00001156  00001188  392          MVC   XCPM3(2),PRT3+14       fill in message with m3 field
                                                  393 *
0000049A  B982 0022                               394          XGR   R2,R2
0000049E  4320 5009                     00000009  395          IC    R2,M4                  get m4 and convert
000004A2  4E20 8F90                     00001190  396          CVD   R2,DECNUM
000004A6  D211 8F7A 8F64      0000117A  00001164  397          MVC   PRT3,EDIT
000004AC  DE11 8F7A 8F90      0000117A  00001190  398          ED    PRT3,DECNUM
000004B2  D201 8F61 8F88      00001161  00001188  399          MVC   XCPM4(2),PRT3+14       fill in message with m4 field
                                                  400
000004B8  50F0 8308                     00000508  401          ST    R15,XCR15              save r15
000004BC  4100 004E                     0000004E  402          LA    R0,XCPLNG              message length
000004C0  4110 8F16                     00001116  403          LA    R1,XCPLINE             message address
000004C4  45F0 847A                     0000067A  404          BAL   R15,RPTERROR
000004C8  58F0 8308                     00000508  405          L     R15,XCR15
                                                  406
000004CC  5800 85E0                     000007E0  407          L     R0,=F'1'               set failed test indicator
000004D0  5000 8E00                     00001000  408          ST    R0,FAILED
000004D4  07FF                                    409          BR    R15                    return from xcheck
                                                  410
000004D8                                          411          DS    0FD
000004D8  00000000 00000000                       412 XCRESULT DS    XL16
000004E8  00000000 00000000                       413 XCV1     DS    XL16
000004F8  00000000 00000000                       414 XCV2     DS    XL16
00000508  00000000 00000000                       415 XCR15    DS    FD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   417 ***********************************************************************
                                                   418 * FPC not as expected:
                                                   419 *        issue message with test number, instruction under test,
                                                   420 *              expected FPC and received FPC
                                                   421 ***********************************************************************
                                 00000510  00000001  422 FPCMSG   EQU   *
00000510  5800 85E0                        000007E0  423          L     R0,=F'1'                set failed test indicator
00000514  5000 8E00                        00001000  424          ST    R0,FAILED
                                                   425
00000518  4820 5004                        00000004  426          LH    R2,TNUM                 get test number and convert
0000051C  4E20 8F90                        00001190  427          CVD   R2,DECNUM
00000520  D211 8F7A 8F64         0000117A  00001164  428          MVC   PRT3,EDIT
00000526  DE11 8F7A 8F90         0000117A  00001190  429          ED    PRT3,DECNUM
0000052C  D202 8E15 8F87         00001015  00001187  430          MVC   FPCPNUM(3),PRT3+13      fill in message with test #
                                                   431
00000532  D207 8E39 5010         00001039  00000010  432          MVC   FPCPNAME,OPNAME         fill in message with instruction
                                                   433 *
00000538  B982 0022                                434          XGR   R2,R2
0000053C  4320 500A                        0000000A  435          IC    R2,FLG                  get expected flags and convert
00000540  4E20 8F90                        00001190  436          CVD   R2,DECNUM
00000544  D211 8F7A 8F64         0000117A  00001164  437          MVC   PRT3,EDIT
0000054A  DE11 8F7A 8F90         0000117A  00001190  438          ED    PRT3,DECNUM
00000550  D202 8E52 8F87         00001052  00001187  439          MVC   FPCPEXP(3),PRT3+13      fill in message with m3 field
                                                   440 *
00000556  B982 0022                                441          XGR   R2,R2
0000055A  4320 5041                        00000041  442          IC    R2,FPC_R+1              get received flags and convert
0000055E  4E20 8F90                        00001190  443          CVD   R2,DECNUM
00000562  D211 8F7A 8F64         0000117A  00001164  444          MVC   PRT3,EDIT
00000568  DE11 8F7A 8F90         0000117A  00001190  445          ED    PRT3,DECNUM
0000056E  D202 8E67 8F87         00001067  00001187  446          MVC   FPCPGOT(3),PRT3+13      fill in message with FPC got
                                                   447 *
00000574  4100 0063                        00000063  448          LA    R0,FPCPLNG              message length
00000578  4110 8E08                        00001008  449          LA    R1,FPCPLINE             message address
0000057C  45F0 847A                        0000067A  450          BAL   R15,RPTERROR
00000580  07F7                                     451          BR    R7
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   453 ***********************************************************************
                                                   454 * VXC not as expected:
                                                   455 *        issue message with test number, instruction under test,
                                                   456 *               expected FPC and received FPC
                                                   457 ***********************************************************************
                                 00000582  00000001  458 VXCMSG   EQU   *
00000582  5800 85E0                        000007E0  459          L     R0,=F'1'                set failed test indicator
00000586  5000 8E00                        00001000  460          ST    R0,FAILED
                                                   461
0000058A  4820 5004                        00000004  462          LH    R2,TNUM                 get test number and convert
0000058E  4E20 8F90                        00001190  463          CVD   R2,DECNUM
00000592  D211 8F7A 8F64         0000117A  00001164  464          MVC   PRT3,EDIT
00000598  DE11 8F7A 8F90         0000117A  00001190  465          ED    PRT3,DECNUM
0000059E  D202 8E78 8F87         00001078  00001187  466          MVC   VXCPNUM(3),PRT3+13      fill in message with test #
                                                   467
000005A4  D207 8E9C 5010         0000109C  00000010  468          MVC   VXCPNAME,OPNAME         fill in message with instruction
                                                   469 *
000005AA  B982 0022                                470          XGR   R2,R2
000005AE  4320 500B                        0000000B  471          IC    R2,VXC                  get expected flags and convert
000005B2  4E20 8F90                        00001190  472          CVD   R2,DECNUM
000005B6  D211 8F7A 8F64         0000117A  00001164  473          MVC   PRT3,EDIT
000005BC  DE11 8F7A 8F90         0000117A  00001190  474          ED    PRT3,DECNUM
000005C2  D202 8EB5 8F87         000010B5  00001187  475          MVC   VXCPEXP(3),PRT3+13      fill in message with m3 field
                                                   476 *
000005C8  B982 0022                                477          XGR   R2,R2
000005CC  4320 5042                        00000042  478          IC    R2,FPC_R+2              get received flags and convert
000005D0  4E20 8F90                        00001190  479          CVD   R2,DECNUM
000005D4  D211 8F7A 8F64         0000117A  00001164  480          MVC   PRT3,EDIT
000005DA  DE11 8F7A 8F90         0000117A  00001190  481          ED    PRT3,DECNUM
000005E0  D202 8ECA 8F87         000010CA  00001187  482          MVC   VXCPGOT(3),PRT3+13      fill in message with FPC got
                                                   483 *
000005E6  4100 0063                        00000063  484          LA    R0,VXCPLNG              message length
000005EA  4110 8E6B                        0000106B  485          LA    R1,VXCPLINE             message address
000005EE  45F0 847A                        0000067A  486          BAL   R15,RPTERROR
000005F2  07F7                                     487          BR    R7
                                                   488
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   490 ***********************************************************************
                                                   491 * result not as expected:
                                                   492 *        issue message with test number, instruction under test
                                                   493 *              and instruction m4
                                                   494 ***********************************************************************
                                000005F4  00000001 495 FAILMSG  EQU   *
000005F4  4820 5004                       00000004 496          LH    R2,TNUM                 get test number and convert
000005F8  4E20 8F90                       00001190 497          CVD   R2,DECNUM
000005FC  D211 8F7A 8F64        0000117A  00001164 498          MVC   PRT3,EDIT
00000602  DE11 8F7A 8F90        0000117A  00001190 499          ED    PRT3,DECNUM
00000608  D202 8EDB 8F87        000010DB  00001187 500          MVC   PRTNUM(3),PRT3+13       fill in message with test #
                                                   501
0000060E  D207 8EF6 5010        000010F6  00000010 502          MVC   PRTNAME,OPNAME          fill in message with instruction
                                                   503 *
00000614  B982 0022                                504          XGR   R2,R2
00000618  4320 5008                       00000008 505          IC    R2,M3                   get m3 and convert
0000061C  4E20 8F90                       00001190 506          CVD   R2,DECNUM
00000620  D211 8F7A 8F64        0000117A  00001164 507          MVC   PRT3,EDIT
00000626  DE11 8F7A 8F90        0000117A  00001190 508          ED    PRT3,DECNUM
0000062C  D201 8F07 8F88        00001107  00001188 509          MVC   PRTM3(2),PRT3+14        fill in message with m3 field
                                                   510 *
00000632  B982 0022                                511          XGR   R2,R2
00000636  4320 5009                       00000009 512          IC    R2,M4                   get m4 and convert
0000063A  4E20 8F90                       00001190 513          CVD   R2,DECNUM
0000063E  D211 8F7A 8F64        0000117A  00001164 514          MVC   PRT3,EDIT
00000644  DE11 8F7A 8F90        0000117A  00001190 515          ED    PRT3,DECNUM
0000064A  D201 8F13 8F88        00001113  00001188 516          MVC   PRTM4(2),PRT3+14        fill in message with m4 field
                                                   517 *
00000650  4100 0048                       00000048 518          LA    R0,PRTLNG               message length
00000654  4110 8ECE                       000010CE 519          LA    R1,PRTLINE              message address
00000658  45F0 847A                       0000067A 520          BAL   R15,RPTERROR


                                                   522 ***********************************************************************
                                                   523 * continue after a failed test
                                                   524 ***********************************************************************
                                0000065C  00000001 525 FAILCONT EQU   *
0000065C  5800 85E0                       000007E0 526          L     R0,=F'1'                set failed test indicator
00000660  5000 8E00                       00001000 527          ST    R0,FAILED
                                                   528
00000664  41C0 C004                       00000004 529          LA    R12,4(0,R12)            next test address
00000668  47F0 80EC                       000002EC 530          B     NEXTE6


                                                   532 ***********************************************************************
                                                   533 * end of testing; set ending psw
                                                   534 ***********************************************************************
                                0000066C  00000001 535 ENDTEST  EQU   *
0000066C  5810 8E00                       00001000 536          L     R1,FAILED               did a test fail?
00000670  1211                                     537          LTR   R1,R1
00000672  4780 8580                       00000780 538          BZ    EOJ                      No, exit
00000676  47F0 8598                       00000798 539          B     FAILTEST                 Yes, exit with BAD PSW
                                                   540
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   542 ************************************************************************
                                                   543 *        RPTERROR          Report instruction test in error
                                                   544 *                              R0 = MESSGAE LENGTH
                                                   545 *                              R1 = ADDRESS OF MESSAGE
                                                   546 ************************************************************************

0000067A  50F0 8498                     00000698   548 RPTERROR ST    R15,RPTSAVE            Save return address
0000067E  5050 849C                     0000069C   549          ST    R5,RPTSVR5             Save R5
                                                   550 *
                                                   551 *        Use Hercules Diagnose for Message to console
                                                   552 *
00000682  9002 84A0                     000006A0   553          STM   R0,R2,RPTDWSAV         save regs used by MSG
00000686  4520 84B0                     000006B0   554          BAL   R2,MSG                 call Hercules console MSG display
0000068A  9802 84A0                     000006A0   555          LM    R0,R2,RPTDWSAV         restore regs


0000068E  5850 849C                     0000069C   557          L     R5,RPTSVR5             Restore R5
00000692  58F0 8498                     00000698   558          L     R15,RPTSAVE            Restore return address
00000696  07FF                                     559          BR    R15                    Return to caller

00000698  00000000                                 561 RPTSAVE  DC    F'0'                   R15 save area
0000069C  00000000                                 562 RPTSVR5  DC    F'0'                   R5 save area

000006A0  00000000 00000000                        564 RPTDWSAV DC    2D'0'                  R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   566 ************************************************************************
                                                   567 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                   568 *              R2 = return address
                                                   569 ************************************************************************

000006B0  4900 85E4                    000007E4    571 MSG      CH    R0,=H'0'                Do we even HAVE a message?
000006B4  07D2                                     572          BNHR  R2                      No, ignore

000006B6  9002 84EC                    000006EC    574          STM   R0,R2,MSGSAVE           Save registers

000006BA  4900 85E6                    000007E6    576          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
000006BE  47D0 84C6                    000006C6    577          BNH   MSGOK                   Yes, continue
000006C2  4100 0064                    00000064    578          LA    R0,L'MSGMSG             No, set to maximum

000006C6  1820                                     580 MSGOK    LR    R2,R0                   Copy length to work register
000006C8  0620                                     581          BCTR  R2,0                    Minus-1 for execute
000006CA  4420 84F8                    000006F8    582          EX    R2,MSGMVC               Copy message to O/P buffer

000006CE  4120 200A                    0000000A    584          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
000006D2  4110 84FE                    000006FE    585          LA    R1,MSGCMD               Point to true command

000006D6  83120008                                 587          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
000006DA  4780 84E6                    000006E6    588          BZ    MSGRET                  Return if successful
                                                   589
000006DE  1222                                     590          LTR   R2,R2                   Is Diag8 Ry (R2) 0?
000006E0  4780 84E6                    000006E6    591          BZ    MSGRET                    an error occurred but coninue
                                                   592
000006E4  0000                                     593          DC    H'0'                    CRASH for debugging purposes

000006E6  9802 84EC                    000006EC    595 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
000006EA  07F2                                     596          BR    R2                      Return to caller


000006EC  00000000 00000000                        598 MSGSAVE  DC    3F'0'                   Registers save area
000006F8  D200 8507 1000      00000707  00000000   599 MSGMVC   MVC   MSGMSG(0),0(R1)          Executed instruction


000006FE  D4E2C7D5 D6C8405C                        601 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
00000707  40404040 40404040                        602 MSGMSG   DC    CL100' '                The message text to be displayed
                                                   603
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   605 ************************************************************************
                                                   606 *        Normal completion or Abnormal termination PSWs
                                                   607 ************************************************************************


00000770  00020001 80000000                        609 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000780  B2B2 8570                     00000770   611 EOJ      LPSWE EOJPSW               Normal completion


00000788  00020001 80000000                        613 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

00000798  B2B2 8588                     00000788   615 FAILTEST LPSWE FAILPSW              Abnormal termination


                                                   617 ************************************************************************
                                                   618 *        Working Storage
                                                   619 ************************************************************************


0000079C  00000000                                 621 CTLR0    DS    F                      CR0
000007A0  00000000                                 622          DS    F
000007A4  00000000                                 623 FPCINIT  DC    XL4'00000000'          FPC before test


                                                   625
000007A8                                           626          LTORG ,                Literals pool
000007A8  E2D2C9D7 40E7C340                        627                =CL8'SKIP XC '
000007B0  40404040 40404040                        628                =CL8'        '
000007B8  E5C3D5C6 40404040                        629                =CL8'VCNF'
000007C0  E5C3D3C6 D5C84040                        630                =CL8'VCLFNH'
000007C8  E5C3C6D5 40404040                        631                =CL8'VCFN'
000007D0  E5C3D3C6 D5D34040                        632                =CL8'VCLFNL'
000007D8  00000004                                 633                =F'4'
000007DC  0000548C                                 634                =A(E6TESTS)
000007E0  00000001                                 635                =F'1'
000007E4  0000                                     636                =H'0'
000007E6  0064                                     637                =AL2(L'MSGMSG)
000007E8  E2                                       638                =CL1'S'
                                                   639
                                                   640 *        some constants
                                                   641
                            00000400  00000001     642 K        EQU   1024             One KB
                            00001000  00000001     643 PAGE     EQU   (4*K)            Size of one page
                            00010000  00000001     644 K64      EQU   (64*K)           64 KB
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                              00100000  00000001   645 MB       EQU   (K*K)             1 MB
                                                   646
                                                   647
                              AABBCCDD  00000001   648 REG2PATT EQU   X'AABBCCDD'    Polluted Register pattern
                              000000DD  00000001   649 REG2LOW  EQU         X'DD'    (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    651 *=====================================================================
                                                    652 *
                                                    653 *  NOTE: start data on an address that is easy to display
                                                    654 *        within Hercules
                                                    655 *
                                                    656 *=====================================================================
                                                    657
000007E9                      000007E9  00001000    658          ORG   ZVE6TST+X'1000'
00001000  00000000                                  659 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                  660 TESTING  DC    F'0'                    current test #


                                                    662
                                                    663 ************************************************************************
                                                    664 *        TEST failed : FPC message
                                                    665 ************************************************************************
                                                    666 *
                                                    667 *        failed message and associated editting
                                                    668 *
00001008  40404040 4040E385                         669 FPCPLINE DC    C'      Test # '
00001015  A7A7A7                                    670 FPCPNUM  DC    C'xxx'
00001018  40A69996 958740C6                         671          DC    c' wrong FPC flags for instruction '
00001039  A7A7A7A7 A7A7A7A7                         672 FPCPNAME DC    CL8'xxxxxxxx'
00001041  4085A797 8583A385                         673          DC    C' expected: flags='
00001052  A7A7A7                                    674 FPCPEXP  DC    C'xxx'
00001055  6B                                        675          DC    C','
00001056  40998583 8589A585                         676          DC    C' received: flags='
00001067  A7A7A7                                    677 FPCPGOT  DC    C'xxx'
0000106A  4B                                        678          DC    C'.'
                              00000063  00000001    679 FPCPLNG  EQU   *-FPCPLINE


                                                    681
                                                    682 ************************************************************************
                                                    683 *        TEST failed : VXC message
                                                    684 ************************************************************************
                                                    685 *
                                                    686 *        failed message and associated editting
                                                    687 *
0000106B  40404040 4040E385                         688 VXCPLINE DC    C'      Test # '
00001078  A7A7A7                                    689 VXCPNUM  DC    C'xxx'
0000107B  40A69996 958740C6                         690          DC    c' wrong FPC VXC   for instruction '
0000109C  A7A7A7A7 A7A7A7A7                         691 VXCPNAME DC    CL8'xxxxxxxx'
000010A4  4085A797 8583A385                         692          DC    C' expected:   VXC='
000010B5  A7A7A7                                    693 VXCPEXP  DC    C'xxx'
000010B8  6B                                        694          DC    C','
000010B9  40998583 8589A585                         695          DC    C' received:   VXC='
000010CA  A7A7A7                                    696 VXCPGOT  DC    C'xxx'
000010CD  4B                                        697          DC    C'.'
                              00000063  00000001    698 VXCPLNG  EQU   *-VXCPLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    700 ************************************************************************
                                                    701 *        TEST failed : result messgae
                                                    702 ************************************************************************
                                                    703 *
                                                    704 *        failed message and associated editting
                                                    705 *
000010CE  40404040 4040E385                         706 PRTLINE  DC    C'      Test # '
000010DB  A7A7A7                                    707 PRTNUM   DC    C'xxx'
000010DE  40868189 93858440                         708          DC    c' failed for instruction '
000010F6  A7A7A7A7 A7A7A7A7                         709 PRTNAME  DC    CL8'xxxxxxxx'
000010FE  40A689A3 884094F3                         710          DC    C' with m3='
00001107  A7A7                                      711 PRTM3    DC    C'xx'
00001109  6B                                        712          DC    C','
0000110A  40A689A3 884094F4                         713          DC    C' with m4='
00001113  A7A7                                      714 PRTM4    DC    C'xx'
00001115  4B                                        715          DC    C'.'
                            00000048  00000001      716 PRTLNG   EQU   *-PRTLINE


                                                    718 ************************************************************************
                                                    719 *        TEST failed : XCHECK
                                                    720 ************************************************************************
                                                    721 *
                                                    722 *        XCHECK failed message
                                                    723 *
00001116  40404040 4040E385                         724 XCPLINE  DC    C'      Test # '
00001123  A7A7A7                                    725 XCPTNUM  DC    C'xxx'
00001126  40E7C3C8 C5C3D240                         726          DC    c' XCHECK failed for instruction '
00001145  A7A7A7A7 A7A7A7A7                         727 XCPNAME  DC    CL8'xxxxxxxx'
0000114D  40A689A3 884094F3                         728          DC    C' with m3='
00001156  A7A7                                      729 XCPM3    DC    C'xx'
00001158  40A689A3 884094F4                         730          DC    C' with m4='
00001161  A7A7                                      731 XCPM4    DC    C'xx'
00001163  4B                                        732          DC    C'.'
                            0000004E  00000001      733 XCPLNG   EQU   *-XCPLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   735 ***********************************************************************
                                                   736 *        TEST failed : message working storge
                                                   737 ***********************************************************************
00001164  40212020 20202020                        738 EDIT     DC    XL18'402120202020202020202020202020202020'
                                                   739
00001176  7E7E7E6E                                 740          DC    C'===>'
0000117A  40404040 40404040                        741 PRT3     DC    CL18' '
0000118C  4C7E7E7E                                 742          DC    C'<===='
00001190  00000000 00000000                        743 DECNUM   DS    CL16


                                                   745 *
                                                   746 *        Vector instruction results, pollution and input
                                                   747 *
000011A0  00000000 00000000                        748          DS    XL16                                          gap
000011B0  FFFFFFFF FFFFFFFF                        749 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000011C0  12345678 90123456                        750 V1INPUT  DC    XL16'12345678901234567890123456789 01D'    V1 input
000011D0  00000000 00000000                        751          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   753 ************************************************************************
                                                   754 *        E6TEST DSECT
                                                   755 ************************************************************************


                                                   757 E6TEST   DSECT ,
00000000  00000000                                 758 TSUB     DC    A(0)              pointer  to test
00000004  0000                                     759 TNUM     DC    H'00'             Test Number
00000006  00                                       760          DC    X'00'
00000007  40                                       761 XCSKIP   DC    CL1' '            Y = skip cross check
00000008  00                                       762 M3       DC    HL1'00'           m3 used
00000009  00                                       763 M4       DC    HL1'00'           m4 used
0000000A  00                                       764 FLG      DC    X'00'             expected FPC flags
0000000B  00                                       765 VXC      DC    X'00'             VXC expected
0000000C  00000000                                 766 V2ADDR   DC    A(0)              address of v2: 16-byte packed decimal
00000010  40404040 40404040                        767 OPNAME   DC    CL8' '            E6 name
00000018  00000000                                 768 RELEN    DC    A(0)              result length
0000001C  00000000                                 769 READDR   DC    A(0)              expected result address
00000020  00000000 00000000                        770          DS    FD                   gap
00000028  00000000 00000000                        771 V1OUTPUT DS    XL16              V1 Output
00000038  00000000 00000000                        772          DS    FD                   gap
00000040  00000000                                 773 FPC_R    DS    F                 FPC after instruction
00000048  00000000 00000000                        774          DS    FD                   gap
00000050  40404040 40404040                        775 SKIPXC   DC    CL8' '            was cross check skipped?
00000058  00000000 00000000                        776          DS    FD                   gap
00000060  00000000 00000000                        777 XCOUTPUT DS    XL16              Cross check Output
00000070  00000000 00000000                        778          DS    FD                   gap
00000078  00000000                                 779 FPC_XC   DS    F                 FPC after cross check
00000080  00000000 00000000                        780          DS    FD                   gap
00000088  00000000                                 781 WK1      DS    F                 debug area
0000008C  00000000                                 782 WK2      DS    F
00000090                                           783          DS    0F
                                                   784 **
                                                   785 *        test routine will be here (from VRR-a macro)


                              00000000  000055D7   787 ZVE6TST  CSECT ,
000011E0                                           788          DS    0F


                                                   790 ************************************************************************
                                                   791 *     Macros to help build test tables
                                                   792 ************************************************************************


                                                   794 *
                                                   795 * macro to generate individual test
                                                   796 *
                                                   797          MACRO
                                                   798          VRR_A &INST,&M3,&M4,&FLAGS,&VXC,&SKIP
                                                   799 .*                              &INST  - VRR-a instruction under test
                                                   800 .*                              &m3    - m3 field
                                                   801 .*                              &m4    - m4 field
                                                   802 .*                              &flags - expected FPC flags (HEX)
                                                   803 .*                              &VXC   - expected VXC (HEX)
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   .*                                &SKIP  - S = skip cross check
                                                            GBLA  &TNUM
                                                   &TNUM    SETA  &TNUM+1

                                                            DS    0FD
                                                            USING *,R5              base for test data and test routine

                                                   T&TNUM   DC    A(X&TNUM)         address of test routine
                                                            DC    H'&TNUM'          test number
                                                            DC    X'00'
                                                            DC    CL1'&SKIP'        Y = skip cross check
                                                            DC    HL1'&M3'          m3
                                                            DC    HL1'&M4'          m4
                                                   FLG&TNUM DC    X'&FLAGS'         expected FPC flags
                                                   VXC&TNUM DC    X'&VXC'           expected VXC
                                                   V2_&TNUM DC    A(RE&TNUM+16)     address of v2: 16-byte packed decimal
                                                            DC    CL8'&INST'        instruction name
                                                            DC    A(16)             result length
                                                            DC    A(RE&TNUM)        address of expected resul
                                                            DS    FD                gap
                                                   V1O&TNUM DS    XL16              V1 output
                                                            DS    FD                   gap
                                                   FPC_R_&TNUM DS F                 FPC after instruction
                                                            DS    FD                   gap
                                                            DC    CL8' '            was cross check skipped?
                                                            DS    FD                   gap
                                                   XCO&TNUM DS    XL16              Cross check Output
                                                            DS    FD                   gap
                                                   FPC_XC_&TNUM DS F                FPC after cross check
                                                            DS    FD                   gap
                                                            DS    F                 debug area
                                                            DS    F
                                                   .*
                                                   *
                                                   X&TNUM   DS    0F
                                                            LFPC  FPCINIT           initialize FPC
                                                   *         LFPC  =XL4'08000000'          set trap exception

                                                            LGF   R2,V2_&TNUM       get v2
                                                            VL    V22,0(R2)

                                                            &INST V22,V22,&M3,&M4   test instruction (dest is source)

                                                            STFPC FPC_R_&TNUM       save FPC
                                                            VST   V22,V1O&TNUM      save instruction result

                                                            BR    R11               return

                                                   RE&TNUM  DS    0F                expected 16 byte result
                                                            DROP  R5

                                                            MEND



                                                   *
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                     858 * macro to generate table of pointers to individual tests
                                                     859 *
                                                     860          MACRO
                                                     861          PTTABLE
                                                     862          GBLA  &TNUM
                                                     863          LCLA  &CUR
                                                     864 &CUR     SETA  1
                                                     865 .*
                                                     866 TTABLE   DS    0F
                                                     867 .LOOP    ANOP
                                                     868 .*
                                                     869          DC    A(T&CUR)          TEST &CUR
                                                     870 .*
                                                     871 &CUR     SETA  &CUR+1
                                                     872          AIF   (&CUR LE &TNUM).LOOP
                                                     873 *
                                                     874          DC    A(0)              END OF TABLE
                                                     875          DC    A(0)
                                                     876 .*
                                                     877          MEND
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  879 ************************************************************************
                                                  880 *        E6 VRR-a tests
                                                  881 ************************************************************************
                                                  882          PRINT DATA
                                                  883 *
                                                  884 *        E655 VCNF     - VECTOR FP CONVERT TO NNP
                                                  885 *        E656 VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                  886 *        E65D VCFN     - VECTOR FP CONVERT FROM NNP
                                                  887 *        E65E VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                  888 *
                                                  889 *-----------------------------------------------------------------------
                                                  890 *   VRR-a   instruction, m3, m4, flags, VXC, SKIP
                                                  891 *   followed by
                                                  892 *              followed by
                                                  893 *              v1 - 16 byte expected result
                                                  894 *              v2 - 16 byte source
                                                  895 *-----------------------------------------------------------------------
                                                  896 * VCNF     - VECTOR FP CONVERT TO NNP
                                                  897 *-----------------------------------------------------------------------
                                                  898 * tinyb -> dlfloat  (with cross check dlfloat -> tinyb)
                                                  899 *
                                                  900 * some of these tests use numbers from PoP SA22-7832-13,
                                                  901 * Figure 9-2. Examples of Floating-Point Numbers ( page 9-6 )
                                                  902 *
                                                  903 * +0     simple instruction test and 'test' test
                                                  904          VRR_A VCNF,0,1,00,00,N
000011E0                                          905+         DS    0FD
000011E0                       000011E0           906+         USING *,R5              base for test data and test routine
000011E0  00001270                                907+T1       DC    A(X1)             address of test routine
000011E4  0001                                    908+         DC    H'1'              test number
000011E6  00                                      909+         DC    X'00'
000011E7  D5                                      910+         DC    CL1'N'            Y = skip cross check
000011E8  00                                      911+         DC    HL1'0'            m3
000011E9  01                                      912+         DC    HL1'1'            m4
000011EA  00                                      913+FLG1     DC    X'00'             expected FPC flags
000011EB  00                                      914+VXC1     DC    X'00'             expected VXC
000011EC  000012A4                                915+V2_1     DC    A(RE1+16)         address of v2: 16-byte packed decimal
000011F0  E5C3D5C6 40404040                       916+         DC    CL8'VCNF'         instruction name
000011F8  00000010                                917+         DC    A(16)             result length
000011FC  00001294                                918+         DC    A(RE1)            address of expected resul
00001200  00000000 00000000                       919+         DS    FD                gap
00001208  00000000 00000000                       920+V1O1     DS    XL16              V1 output
00001210  00000000 00000000
00001218  00000000 00000000                       921+         DS    FD                   gap
00001220  00000000                                922+FPC_R_1  DS    F                 FPC after instruction
00001228  00000000 00000000                       923+         DS    FD                   gap
00001230  40404040 40404040                       924+         DC    CL8' '            was cross check skipped?
00001238  00000000 00000000                       925+         DS    FD                   gap
00001240  00000000 00000000                       926+XCO1     DS    XL16              Cross check Output
00001248  00000000 00000000
00001250  00000000 00000000                       927+         DS    FD                   gap
00001258  00000000                                928+FPC_XC_1 DS    F                 FPC after cross check
00001260  00000000 00000000                       929+         DS    FD                   gap
00001268  00000000                                930+         DS    F                 debug area
0000126C  00000000                                931+         DS    F
                                                  932+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001270                                          933+X1       DS    0F
00001270  B29D 85A4                    000007A4   934+         LFPC  FPCINIT           initialize FPC
                                                  935+*         LFPC  =XL4'08000000'          set trap exception
00001274  E320 500C 0014               000011EC   936+         LGF   R2,V2_1           get v2
0000127A  E762 0000 0806               00000000   937+         VL    V22,0(R2)
00001280  E666 0001 0C55                          938+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001286  B29C 9020                    00001220   939+         STFPC FPC_R_1           save FPC
0000128A  E760 9008 080E               00001208   940+         VST   V22,V1O1          save instruction result
00001290  07FB                                    941+         BR    R11               return
00001294                                          942+RE1      DS    0F                expected 16 byte result
00001294                                          943+         DROP  R5
00001294  00000000 00000000                       944          DC    XL16'00000000000000000000000000000000'
0000129C  00000000 00000000
000012A4  00000000 00000000                       945          DC    XL16'00000000000000000000000000000000'
000012AC  00000000 00000000
                                                  946
                                                  947 * 1.0, -1, .... -4096
                                                  948          VRR_A VCNF,0,1,00,00,N
000012B8                                          949+         DS    0FD
000012B8                       000012B8           950+         USING *,R5              base for test data and test routine
000012B8  00001348                                951+T2       DC    A(X2)             address of test routine
000012BC  0002                                    952+         DC    H'2'              test number
000012BE  00                                      953+         DC    X'00'
000012BF  D5                                      954+         DC    CL1'N'            Y = skip cross check
000012C0  00                                      955+         DC    HL1'0'            m3
000012C1  01                                      956+         DC    HL1'1'            m4
000012C2  00                                      957+FLG2     DC    X'00'             expected FPC flags
000012C3  00                                      958+VXC2     DC    X'00'             expected VXC
000012C4  0000137C                                959+V2_2     DC    A(RE2+16)         address of v2: 16-byte packed decimal
000012C8  E5C3D5C6 40404040                       960+         DC    CL8'VCNF'         instruction name
000012D0  00000010                                961+         DC    A(16)             result length
000012D4  0000136C                                962+         DC    A(RE2)            address of expected resul
000012D8  00000000 00000000                       963+         DS    FD                gap
000012E0  00000000 00000000                       964+V1O2     DS    XL16              V1 output
000012E8  00000000 00000000
000012F0  00000000 00000000                       965+         DS    FD                   gap
000012F8  00000000                                966+FPC_R_2  DS    F                 FPC after instruction
00001300  00000000 00000000                       967+         DS    FD                   gap
00001308  40404040 40404040                       968+         DC    CL8' '            was cross check skipped?
00001310  00000000 00000000                       969+         DS    FD                   gap
00001318  00000000 00000000                       970+XCO2     DS    XL16              Cross check Output
00001320  00000000 00000000
00001328  00000000 00000000                       971+         DS    FD                   gap
00001330  00000000                                972+FPC_XC_2 DS    F                 FPC after cross check
00001338  00000000 00000000                       973+         DS    FD                   gap
00001340  00000000                                974+         DS    F                 debug area
00001344  00000000                                975+         DS    F
                                                  976+*
00001348                                          977+X2       DS    0F
00001348  B29D 85A4                    000007A4   978+         LFPC  FPCINIT           initialize FPC
                                                  979+*         LFPC  =XL4'08000000'          set trap exception
0000134C  E320 500C 0014               000012C4   980+         LGF   R2,V2_2           get v2
00001352  E762 0000 0806               00000000   981+         VL    V22,0(R2)
00001358  E666 0001 0C55                          982+         VCNF  V22,V22,0,1       test instruction (dest is source)
0000135E  B29C 5040                    000012F8   983+         STFPC FPC_R_2           save FPC
00001362  E760 5028 080E               000012E0   984+         VST   V22,V1O2          save instruction result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001368  07FB                                     985+         BR    R11                 return
0000136C                                           986+RE2      DS    0F                  expected 16 byte result
0000136C                                           987+         DROP  R5
0000136C  3E000000 BE000000                        988          DC    XL16'3E000000BE000000000000000000D800'
00001374  00000000 0000D800
0000137C  3C000000 BC000000                        989          DC    XL16'3C000000BC000000000000000000F000'
00001384  00000000 0000F000
                                                   990 * 0.5
                                                   991          VRR_A VCNF,0,1,00,00,N
00001390                                           992+         DS    0FD
00001390                      00001390             993+         USING *,R5                base for test data and test routine
00001390  00001420                                 994+T3       DC    A(X3)               address of test routine
00001394  0003                                     995+         DC    H'3'                test number
00001396  00                                       996+         DC    X'00'
00001397  D5                                       997+         DC    CL1'N'              Y = skip cross check
00001398  00                                       998+         DC    HL1'0'              m3
00001399  01                                       999+         DC    HL1'1'              m4
0000139A  00                                      1000+FLG3     DC    X'00'               expected FPC flags
0000139B  00                                      1001+VXC3     DC    X'00'               expected VXC
0000139C  00001454                                1002+V2_3     DC    A(RE3+16)           address of v2: 16-byte packed decimal
000013A0  E5C3D5C6 40404040                       1003+         DC    CL8'VCNF'           instruction name
000013A8  00000010                                1004+         DC    A(16)               result length
000013AC  00001444                                1005+         DC    A(RE3)              address of expected resul
000013B0  00000000 00000000                       1006+         DS    FD                  gap
000013B8  00000000 00000000                       1007+V1O3     DS    XL16                V1 output
000013C0  00000000 00000000
000013C8  00000000 00000000                       1008+         DS    FD                     gap
000013D0  00000000                                1009+FPC_R_3  DS    F                   FPC after instruction
000013D8  00000000 00000000                       1010+         DS    FD                     gap
000013E0  40404040 40404040                       1011+         DC    CL8' '              was cross check skipped?
000013E8  00000000 00000000                       1012+         DS    FD                     gap
000013F0  00000000 00000000                       1013+XCO3     DS    XL16                Cross check Output
000013F8  00000000 00000000
00001400  00000000 00000000                       1014+         DS    FD                     gap
00001408  00000000                                1015+FPC_XC_3 DS    F                   FPC after cross check
00001410  00000000 00000000                       1016+         DS    FD                     gap
00001418  00000000                                1017+         DS    F                   debug area
0000141C  00000000                                1018+         DS    F
                                                  1019+*
00001420                                          1020+X3       DS    0F
00001420  B29D 85A4                    000007A4   1021+         LFPC  FPCINIT             initialize FPC
                                                  1022+*         LFPC  =XL4'08000000'            set trap exception
00001424  E320 500C 0014               0000139C   1023+         LGF   R2,V2_3             get v2
0000142A  E762 0000 0806               00000000   1024+         VL    V22,0(R2)
00001430  E666 0001 0C55                          1025+         VCNF  V22,V22,0,1         test instruction (dest is source)
00001436  B29C 5040                    000013D0   1026+         STFPC FPC_R_3             save FPC
0000143A  E760 5028 080E               000013B8   1027+         VST   V22,V1O3            save instruction result
00001440  07FB                                    1028+         BR    R11                 return
00001444                                          1029+RE3      DS    0F                  expected 16 byte result
00001444                                          1030+         DROP  R5
00001444  3C000000 00000000                       1031          DC    XL16'3C000000000000000000000000D800'
0000144C  00000000 0000D800
00001454  38000000 00000000                       1032          DC    XL16'380000000000000000000000F000'
0000145C  00000000 0000F000
                                                  1033
                                                  1034 * 1/64
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   1035          VRR_A VCNF,0,1,00,00,N
00001468                                           1036+         DS    0FD
00001468                     00001468              1037+         USING *,R5              base for test data and test routine
00001468  000014F8                                 1038+T4       DC    A(X4)             address of test routine
0000146C  0004                                     1039+         DC    H'4'              test number
0000146E  00                                       1040+         DC    X'00'
0000146F  D5                                       1041+         DC    CL1'N'            Y = skip cross check
00001470  00                                       1042+         DC    HL1'0'            m3
00001471  01                                       1043+         DC    HL1'1'            m4
00001472  00                                       1044+FLG4     DC    X'00'             expected FPC flags
00001473  00                                       1045+VXC4     DC    X'00'             expected VXC
00001474  0000152C                                 1046+V2_4     DC    A(RE4+16)         address of v2: 16-byte packed decimal
00001478  E5C3D5C6 40404040                        1047+         DC    CL8'VCNF'         instruction name
00001480  00000010                                 1048+         DC    A(16)             result length
00001484  0000151C                                 1049+         DC    A(RE4)            address of expected resul
00001488  00000000 00000000                        1050+         DS    FD                gap
00001490  00000000 00000000                        1051+V1O4     DS    XL16              V1 output
00001498  00000000 00000000
000014A0  00000000 00000000                        1052+         DS    FD                   gap
000014A8  00000000                                 1053+FPC_R_4  DS    F                 FPC after instruction
000014B0  00000000 00000000                        1054+         DS    FD                   gap
000014B8  40404040 40404040                        1055+         DC    CL8' '            was cross check skipped?
000014C0  00000000 00000000                        1056+         DS    FD                   gap
000014C8  00000000 00000000                        1057+XCO4     DS    XL16              Cross check Output
000014D0  00000000 00000000
000014D8  00000000 00000000                        1058+         DS    FD                   gap
000014E0  00000000                                 1059+FPC_XC_4 DS    F                 FPC after cross check
000014E8  00000000 00000000                        1060+         DS    FD                   gap
000014F0  00000000                                 1061+         DS    F                 debug area
000014F4  00000000                                 1062+         DS    F
                                                   1063+*
000014F8                                           1064+X4       DS    0F
000014F8  B29D 85A4                    000007A4    1065+         LFPC  FPCINIT           initialize FPC
                                                   1066+*         LFPC  =XL4'08000000'          set trap exception
000014FC  E320 500C 0014               00001474    1067+         LGF   R2,V2_4           get v2
00001502  E762 0000 0806               00000000    1068+         VL    V22,0(R2)
00001508  E666 0001 0C55                           1069+         VCNF  V22,V22,0,1       test instruction (dest is source)
0000150E  B29C 5040                    000014A8    1070+         STFPC FPC_R_4           save FPC
00001512  E760 5028 080E               00001490    1071+         VST   V22,V1O4          save instruction result
00001518  07FB                                     1072+         BR    R11               return
0000151C                                           1073+RE4      DS    0F                expected 16 byte result
0000151C                                           1074+         DROP  R5
0000151C  32000000 00000000                        1075          DC    XL16'32000000000000000000000000D800'
00001524  00000000 0000D800
0000152C  24000000 00000000                        1076          DC    XL16'24000000000000000000000000F000'
00001534  00000000 0000F000
                                                   1077
                                                   1078 * +0, -0
                                                   1079          VRR_A VCNF,0,1,00,00,N
00001540                                           1080+         DS    0FD
00001540                     00001540              1081+         USING *,R5              base for test data and test routine
00001540  000015D0                                 1082+T5       DC    A(X5)             address of test routine
00001544  0005                                     1083+         DC    H'5'              test number
00001546  00                                       1084+         DC    X'00'
00001547  D5                                       1085+         DC    CL1'N'            Y = skip cross check
00001548  00                                       1086+         DC    HL1'0'            m3
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001549  01                                       1087+         DC    HL1'1'            m4
0000154A  00                                       1088+FLG5     DC    X'00'             expected FPC flags
0000154B  00                                       1089+VXC5     DC    X'00'             expected VXC
0000154C  00001604                                 1090+V2_5     DC    A(RE5+16)         address of v2: 16-byte packed decimal
00001550  E5C3D5C6 40404040                        1091+         DC    CL8'VCNF'         instruction name
00001558  00000010                                 1092+         DC    A(16)             result length
0000155C  000015F4                                 1093+         DC    A(RE5)            address of expected resul
00001560  00000000 00000000                        1094+         DS    FD                gap
00001568  00000000 00000000                        1095+V1O5     DS    XL16              V1 output
00001570  00000000 00000000
00001578  00000000 00000000                        1096+         DS    FD                   gap
00001580  00000000                                 1097+FPC_R_5  DS    F                 FPC after instruction
00001588  00000000 00000000                        1098+         DS    FD                   gap
00001590  40404040 40404040                        1099+         DC    CL8' '            was cross check skipped?
00001598  00000000 00000000                        1100+         DS    FD                   gap
000015A0  00000000 00000000                        1101+XCO5     DS    XL16              Cross check Output
000015A8  00000000 00000000
000015B0  00000000 00000000                        1102+         DS    FD                   gap
000015B8  00000000                                 1103+FPC_XC_5 DS    F                 FPC after cross check
000015C0  00000000 00000000                        1104+         DS    FD                   gap
000015C8  00000000                                 1105+         DS    F                 debug area
000015CC  00000000                                 1106+         DS    F
                                                   1107+*
000015D0                                           1108+X5       DS    0F
000015D0  B29D 85A4                     000007A4   1109+         LFPC  FPCINIT           initialize FPC
                                                   1110+*         LFPC  =XL4'08000000'         set trap exception
000015D4  E320 500C 0014                0000154C   1111+         LGF   R2,V2_5           get v2
000015DA  E762 0000 0806                00000000   1112+         VL    V22,0(R2)
000015E0  E666 0001 0C55                           1113+         VCNF  V22,V22,0,1       test instruction (dest is source)
000015E6  B29C 5040                     00001580   1114+         STFPC FPC_R_5           save FPC
000015EA  E760 5028 080E                00001568   1115+         VST   V22,V1O5          save instruction result
000015F0  07FB                                     1116+         BR    R11               return
000015F4                                           1117+RE5      DS    0F                expected 16 byte result
000015F4                                           1118+         DROP  R5
000015F4  00008000 00000000                        1119          DC    XL16'00008000000000000000000000000D800'
000015FC  00000000 0000D800
00001604  00008000 00000000                        1120          DC    XL16'00008000000000000000000000000F000'
0000160C  00000000 0000F000
                                                   1121
                                                   1122 * -15
                                                   1123          VRR_A VCNF,0,1,00,00,N
00001618                                           1124+         DS    0FD
00001618                        00001618           1125+         USING *,R5              base for test data and test routine
00001618  000016A8                                 1126+T6       DC    A(X6)             address of test routine
0000161C  0006                                     1127+         DC    H'6'              test number
0000161E  00                                       1128+         DC    X'00'
0000161F  D5                                       1129+         DC    CL1'N'            Y = skip cross check
00001620  00                                       1130+         DC    HL1'0'            m3
00001621  01                                       1131+         DC    HL1'1'            m4
00001622  00                                       1132+FLG6     DC    X'00'             expected FPC flags
00001623  00                                       1133+VXC6     DC    X'00'             expected VXC
00001624  000016DC                                 1134+V2_6     DC    A(RE6+16)         address of v2: 16-byte packed decimal
00001628  E5C3D5C6 40404040                        1135+         DC    CL8'VCNF'         instruction name
00001630  00000010                                 1136+         DC    A(16)             result length
00001634  000016CC                                 1137+         DC    A(RE6)            address of expected resul
00001638  00000000 00000000                        1138+         DS    FD                gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001640  00000000 00000000                        1139+V1O6     DS    XL16              V1 output
00001648  00000000 00000000
00001650  00000000 00000000                        1140+         DS    FD                   gap
00001658  00000000                                 1141+FPC_R_6  DS    F                 FPC after instruction
00001660  00000000 00000000                        1142+         DS    FD                   gap
00001668  40404040 40404040                        1143+         DC    CL8' '            was cross check skipped?
00001670  00000000 00000000                        1144+         DS    FD                   gap
00001678  00000000 00000000                        1145+XCO6     DS    XL16              Cross check Output
00001680  00000000 00000000
00001688  00000000 00000000                        1146+         DS    FD                   gap
00001690  00000000                                 1147+FPC_XC_6 DS    F                 FPC after cross check
00001698  00000000 00000000                        1148+         DS    FD                   gap
000016A0  00000000                                 1149+         DS    F                 debug area
000016A4  00000000                                 1150+         DS    F
                                                   1151+*
000016A8                                           1152+X6       DS    0F
000016A8  B29D 85A4                     000007A4   1153+         LFPC  FPCINIT           initialize FPC
                                                   1154+*         LFPC  =XL4'08000000'         set trap exception
000016AC  E320 500C 0014                00001624   1155+         LGF   R2,V2_6           get v2
000016B2  E762 0000 0806                00000000   1156+         VL    V22,0(R2)
000016B8  E666 0001 0C55                           1157+         VCNF  V22,V22,0,1       test instruction (dest is source)
000016BE  B29C 5040                     00001658   1158+         STFPC FPC_R_6           save FPC
000016C2  E760 5028 080E                00001640   1159+         VST   V22,V1O6          save instruction result
000016C8  07FB                                     1160+         BR    R11               return
000016CC                                           1161+RE6      DS    0F                expected 16 byte result
000016CC                                           1162+         DROP  R5
000016CC  C5C00000 00000000                        1163          DC    XL16'C5C0000000000000000000000D800'
000016D4  00000000 0000D800
000016DC  CB800000 00000000                        1164          DC    XL16'CB800000000000000000000000F000'
000016E4  00000000 0000F000
                                                   1165
                                                   1166 * 20/7 (about)
                                                   1167          VRR_A VCNF,0,1,00,00,N
000016F0                                           1168+         DS    0FD
000016F0                        000016F0           1169+         USING *,R5              base for test data and test routine
000016F0  00001780                                 1170+T7       DC    A(X7)             address of test routine
000016F4  0007                                     1171+         DC    H'7'              test number
000016F6  00                                       1172+         DC    X'00'
000016F7  D5                                       1173+         DC    CL1'N'            Y = skip cross check
000016F8  00                                       1174+         DC    HL1'0'            m3
000016F9  01                                       1175+         DC    HL1'1'            m4
000016FA  00                                       1176+FLG7     DC    X'00'             expected FPC flags
000016FB  00                                       1177+VXC7     DC    X'00'             expected VXC
000016FC  000017B4                                 1178+V2_7     DC    A(RE7+16)         address of v2: 16-byte packed decimal
00001700  E5C3D5C6 40404040                        1179+         DC    CL8'VCNF'         instruction name
00001708  00000010                                 1180+         DC    A(16)             result length
0000170C  000017A4                                 1181+         DC    A(RE7)            address of expected resul
00001710  00000000 00000000                        1182+         DS    FD                gap
00001718  00000000 00000000                        1183+V1O7     DS    XL16              V1 output
00001720  00000000 00000000
00001728  00000000 00000000                        1184+         DS    FD                   gap
00001730  00000000                                 1185+FPC_R_7  DS    F                 FPC after instruction
00001738  00000000 00000000                        1186+         DS    FD                   gap
00001740  40404040 40404040                        1187+         DC    CL8' '            was cross check skipped?
00001748  00000000 00000000                        1188+         DS    FD                   gap
00001750  00000000 00000000                        1189+XCO7     DS    XL16              Cross check Output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001758  00000000 00000000
00001760  00000000 00000000                        1190+          DS    FD                   gap
00001768  00000000                                 1191+FPC_XC_7  DS    F                 FPC after cross check
00001770  00000000 00000000                        1192+          DS    FD                   gap
00001778  00000000                                 1193+          DS    F                 debug area
0000177C  00000000                                 1194+          DS    F
                                                   1195+*
00001780                                           1196+X7        DS    0F
00001780  B29D 85A4                     000007A4   1197+          LFPC  FPCINIT           initialize FPC
                                                   1198+*          LFPC  =XL4'08000000'          set trap exception
00001784  E320 500C 0014                000016FC   1199+          LGF   R2,V2_7           get v2
0000178A  E762 0000 0806                00000000   1200+          VL    V22,0(R2)
00001790  E666 0001 0C55                           1201+          VCNF  V22,V22,0,1       test instruction (dest is source)
00001796  B29C 5040                     00001730   1202+          STFPC FPC_R_7           save FPC
0000179A  E760 5028 080E                00001718   1203+          VST   V22,V1O7          save instruction result
000017A0  07FB                                     1204+          BR    R11               return
000017A4                                           1205+RE7       DS    0F                expected 16 byte result
000017A4                                           1206+          DROP  R5
000017A4  40DB0000 00000000                        1207           DC    XL16'40DB0000000000000000000000D800'
000017AC  00000000 0000D800
000017B4  41B60000 00000000                        1208           DC    XL16'41B6000000000000000000000000F000'
000017BC  00000000 0000F000
                                                   1209
                                                   1210 * additional tests
                                                   1211 * max  tiny:  (1 - 2^-11) * 2^16 (65504)
                                                   1212           VRR_A VCNF,0,1,00,00,S                    skip xc - rounded
000017C8                                           1213+          DS    0FD
000017C8                        000017C8           1214+          USING *,R5              base for test data and test routine
000017C8  00001858                                 1215+T8        DC    A(X8)             address of test routine
000017CC  0008                                     1216+          DC    H'8'              test number
000017CE  00                                       1217+          DC    X'00'
000017CF  E2                                       1218+          DC    CL1'S'            Y = skip cross check
000017D0  00                                       1219+          DC    HL1'0'            m3
000017D1  01                                       1220+          DC    HL1'1'            m4
000017D2  00                                       1221+FLG8      DC    X'00'             expected FPC flags
000017D3  00                                       1222+VXC8      DC    X'00'             expected VXC
000017D4  0000188C                                 1223+V2_8      DC    A(RE8+16)         address of v2: 16-byte packed decimal
000017D8  E5C3D5C6 40404040                        1224+          DC    CL8'VCNF'         instruction name
000017E0  00000010                                 1225+          DC    A(16)             result length
000017E4  0000187C                                 1226+          DC    A(RE8)            address of expected resul
000017E8  00000000 00000000                        1227+          DS    FD                gap
000017F0  00000000 00000000                        1228+V1O8      DS    XL16              V1 output
000017F8  00000000 00000000
00001800  00000000 00000000                        1229+          DS    FD                   gap
00001808  00000000                                 1230+FPC_R_8   DS    F                 FPC after instruction
00001810  00000000 00000000                        1231+          DS    FD                   gap
00001818  40404040 40404040                        1232+          DC    CL8' '            was cross check skipped?
00001820  00000000 00000000                        1233+          DS    FD                   gap
00001828  00000000 00000000                        1234+XCO8      DS    XL16              Cross check Output
00001830  00000000 00000000
00001838  00000000 00000000                        1235+          DS    FD                   gap
00001840  00000000                                 1236+FPC_XC_8  DS    F                 FPC after cross check
00001848  00000000 00000000                        1237+          DS    FD                   gap
00001850  00000000                                 1238+          DS    F                 debug area
00001854  00000000                                 1239+          DS    F
                                                   1240+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001858                                          1241+X8       DS    0F
00001858  B29D 85A4                     000007A4  1242+         LFPC  FPCINIT           initialize FPC
                                                  1243+*         LFPC  =XL4'08000000'         set trap exception
0000185C  E320 500C 0014                000017D4  1244+         LGF   R2,V2_8           get v2
00001862  E762 0000 0806                00000000  1245+         VL    V22,0(R2)
00001868  E666 0001 0C55                          1246+         VCNF  V22,V22,0,1       test instruction (dest is source)
0000186E  B29C 5040                     00001808  1247+         STFPC FPC_R_8           save FPC
00001872  E760 5028 080E                000017F0  1248+         VST   V22,V1O8          save instruction result
00001878  07FB                                    1249+         BR    R11               return
0000187C                                          1250+RE8      DS    0F                expected 16 byte result
0000187C                                          1251+         DROP  R5
0000187C  5E000000 00000000                       1252          DC    XL16'5E000000000000000000000000D800'
00001884  00000000 0000D800
0000188C  7BFF0000 00000000                       1253          DC    XL16'7BFF000000000000000000000000F000'
00001894  00000000 0000F000
                                                  1254
                                                  1255 * min tiny (normal): 2^-14 (0.00006103515625)
                                                  1256          VRR_A VCNF,0,1,00,00,N
000018A0                                          1257+         DS    0FD
000018A0                        000018A0          1258+         USING *,R5              base for test data and test routine
000018A0  00001930                                1259+T9       DC    A(X9)             address of test routine
000018A4  0009                                    1260+         DC    H'9'              test number
000018A6  00                                      1261+         DC    X'00'
000018A7  D5                                      1262+         DC    CL1'N'            Y = skip cross check
000018A8  00                                      1263+         DC    HL1'0'            m3
000018A9  01                                      1264+         DC    HL1'1'            m4
000018AA  00                                      1265+FLG9     DC    X'00'             expected FPC flags
000018AB  00                                      1266+VXC9     DC    X'00'             expected VXC
000018AC  00001964                                1267+V2_9     DC    A(RE9+16)         address of v2: 16-byte packed decimal
000018B0  E5C3D5C6 40404040                       1268+         DC    CL8'VCNF'         instruction name
000018B8  00000010                                1269+         DC    A(16)             result length
000018BC  00001954                                1270+         DC    A(RE9)            address of expected resul
000018C0  00000000 00000000                       1271+         DS    FD                gap
000018C8  00000000 00000000                       1272+V1O9     DS    XL16              V1 output
000018D0  00000000 00000000
000018D8  00000000 00000000                       1273+         DS    FD                   gap
000018E0  00000000                                1274+FPC_R_9  DS    F                 FPC after instruction
000018E8  00000000 00000000                       1275+         DS    FD                   gap
000018F0  40404040 40404040                       1276+         DC    CL8' '            was cross check skipped?
000018F8  00000000 00000000                       1277+         DS    FD                   gap
00001900  00000000 00000000                       1278+XCO9     DS    XL16              Cross check Output
00001908  00000000 00000000
00001910  00000000 00000000                       1279+         DS    FD                   gap
00001918  00000000                                1280+FPC_XC_9 DS    F                 FPC after cross check
00001920  00000000 00000000                       1281+         DS    FD                   gap
00001928  00000000                                1282+         DS    F                 debug area
0000192C  00000000                                1283+         DS    F
                                                  1284+*
00001930                                          1285+X9       DS    0F
00001930  B29D 85A4                     000007A4  1286+         LFPC  FPCINIT           initialize FPC
                                                  1287+*         LFPC  =XL4'08000000'         set trap exception
00001934  E320 500C 0014                000018AC  1288+         LGF   R2,V2_9           get v2
0000193A  E762 0000 0806                00000000  1289+         VL    V22,0(R2)
00001940  E666 0001 0C55                          1290+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001946  B29C 5040                     000018E0  1291+         STFPC FPC_R_9           save FPC
0000194A  E760 5028 080E                000018C8  1292+         VST   V22,V1O9          save instruction result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001950  07FB                                     1293+         BR    R11                 return
00001954                                           1294+RE9      DS    0F                  expected 16 byte result
00001954                                           1295+         DROP  R5
00001954  22000000 00000000                        1296          DC    XL16'22000000000000000000000000000D800'
0000195C  00000000 0000D800
00001964  04000000 00000000                        1297          DC    XL16'04000000000000000000000000000F000'
0000196C  00000000 0000F000
                                                   1298
                                                   1299 * min tiny (subnormal): 2^-24 (0.00000005960464477539062 5)
                                                   1300          VRR_A VCNF,0,1,00,00,N
00001978                                           1301+         DS    0FD
00001978                      00001978             1302+         USING *,R5                base for test data and test routine
00001978  00001A08                                 1303+T10      DC    A(X10)              address of test routine
0000197C  000A                                     1304+         DC    H'10'               test number
0000197E  00                                       1305+         DC    X'00'
0000197F  D5                                       1306+         DC    CL1'N'              Y = skip cross check
00001980  00                                       1307+         DC    HL1'0'              m3
00001981  01                                       1308+         DC    HL1'1'              m4
00001982  00                                       1309+FLG10    DC    X'00'               expected FPC flags
00001983  00                                       1310+VXC10    DC    X'00'               expected VXC
00001984  00001A3C                                 1311+V2_10    DC    A(RE10+16)          address of v2: 16-byte packed decimal
00001988  E5C3D5C6 40404040                        1312+         DC    CL8'VCNF'           instruction name
00001990  00000010                                 1313+         DC    A(16)               result length
00001994  00001A2C                                 1314+         DC    A(RE10)             address of expected resul
00001998  00000000 00000000                        1315+         DS    FD                  gap
000019A0  00000000 00000000                        1316+V1O10    DS    XL16                V1 output
000019A8  00000000 00000000
000019B0  00000000 00000000                        1317+         DS    FD                     gap
000019B8  00000000                                 1318+FPC_R_10 DS    F                   FPC after instruction
000019C0  00000000 00000000                        1319+         DS    FD                     gap
000019C8  40404040 40404040                        1320+         DC    CL8' '              was cross check skipped?
000019D0  00000000 00000000                        1321+         DS    FD                     gap
000019D8  00000000 00000000                        1322+XCO10    DS    XL16                Cross check Output
000019E0  00000000 00000000
000019E8  00000000 00000000                        1323+         DS    FD                     gap
000019F0  00000000                                 1324+FPC_XC_10 DS   F                   FPC after cross check
000019F8  00000000 00000000                        1325+         DS    FD                     gap
00001A00  00000000                                 1326+         DS    F                   debug area
00001A04  00000000                                 1327+         DS    F
                                                   1328+*
00001A08                                           1329+X10      DS    0F
00001A08  B29D 85A4                    000007A4    1330+         LFPC  FPCINIT             initialize FPC
                                                   1331+*         LFPC  =XL4'08000000'          set trap exception
00001A0C  E320 500C 0014               00001984    1332+         LGF   R2,V2_10            get v2
00001A12  E762 0000 0806               00000000    1333+         VL    V22,0(R2)
00001A18  E666 0001 0C55                           1334+         VCNF  V22,V22,0,1         test instruction (dest is source)
00001A1E  B29C 5040                    000019B8    1335+         STFPC FPC_R_10            save FPC
00001A22  E760 5028 080E               000019A0    1336+         VST   V22,V1O10           save instruction result
00001A28  07FB                                     1337+         BR    R11                 return
00001A2C                                           1338+RE10     DS    0F                  expected 16 byte result
00001A2C                                           1339+         DROP  R5
00001A2C  0E000000 00000000                        1340          DC    XL16'0E000000000000000000000000D800'
00001A34  00000000 0000D800
00001A3C  00010000 00000000                        1341          DC    XL16'00010000000000000000000000F000'
00001A44  00000000 0000F000
                                                   1342
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   1343 * NAN,
                                                   1344          VRR_A VCNF,0,1,80,01,S          skip xcheck - includes NAN
00001A50                                           1345+         DS    0FD
00001A50                     00001A50              1346+         USING *,R5              base for test data and test routine
00001A50  00001AE0                                 1347+T11      DC    A(X11)            address of test routine
00001A54  000B                                     1348+         DC    H'11'             test number
00001A56  00                                       1349+         DC    X'00'
00001A57  E2                                       1350+         DC    CL1'S'            Y = skip cross check
00001A58  00                                       1351+         DC    HL1'0'            m3
00001A59  01                                       1352+         DC    HL1'1'            m4
00001A5A  80                                       1353+FLG11    DC    X'80'             expected FPC flags
00001A5B  01                                       1354+VXC11    DC    X'01'             expected VXC
00001A5C  00001B14                                 1355+V2_11    DC    A(RE11+16)        address of v2: 16-byte packed decimal
00001A60  E5C3D5C6 40404040                        1356+         DC    CL8'VCNF'         instruction name
00001A68  00000010                                 1357+         DC    A(16)             result length
00001A6C  00001B04                                 1358+         DC    A(RE11)           address of expected resul
00001A70  00000000 00000000                        1359+         DS    FD                gap
00001A78  00000000 00000000                        1360+V1O11    DS    XL16              V1 output
00001A80  00000000 00000000
00001A88  00000000 00000000                        1361+         DS    FD                   gap
00001A90  00000000                                 1362+FPC_R_11 DS    F                 FPC after instruction
00001A98  00000000 00000000                        1363+         DS    FD                   gap
00001AA0  40404040 40404040                        1364+         DC    CL8' '            was cross check skipped?
00001AA8  00000000 00000000                        1365+         DS    FD                   gap
00001AB0  00000000 00000000                        1366+XCO11    DS    XL16              Cross check Output
00001AB8  00000000 00000000
00001AC0  00000000 00000000                        1367+         DS    FD                   gap
00001AC8  00000000                                 1368+FPC_XC_11 DS   F                 FPC after cross check
00001AD0  00000000 00000000                        1369+         DS    FD                   gap
00001AD8  00000000                                 1370+         DS    F                 debug area
00001ADC  00000000                                 1371+         DS    F
                                                   1372+*
00001AE0                                           1373+X11      DS    0F
00001AE0  B29D 85A4                     000007A4   1374+         LFPC  FPCINIT           initialize FPC
                                                   1375+*         LFPC  =XL4'08000000'          set trap exception
00001AE4  E320 500C 0014                00001A5C   1376+         LGF   R2,V2_11          get v2
00001AEA  E762 0000 0806                00000000   1377+         VL    V22,0(R2)
00001AF0  E666 0001 0C55                           1378+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001AF6  B29C 5040                     00001A90   1379+         STFPC FPC_R_11          save FPC
00001AFA  E760 5028 080E                00001A78   1380+         VST   V22,V1O11         save instruction result
00001B00  07FB                                     1381+         BR    R11               return
00001B04                                           1382+RE11     DS    0F                expected 16 byte result
00001B04                                           1383+         DROP  R5
00001B04  FFFF0000 00000000                        1384          DC    XL16'FFFF0000000000000000000000D800'
00001B0C  00000000 0000D800
00001B14  FFFF0000 00000000                        1385          DC    XL16'FFFF0000000000000000000000F000'
00001B1C  00000000 0000F000
                                                   1386
                                                   1387 * inexact - bad m3
                                                   1388          VRR_A VCNF,5,1,08,05,S                skip xc - inexact
00001B28                                           1389+         DS    0FD
00001B28                     00001B28              1390+         USING *,R5              base for test data and test routine
00001B28  00001BB8                                 1391+T12      DC    A(X12)            address of test routine
00001B2C  000C                                     1392+         DC    H'12'             test number
00001B2E  00                                       1393+         DC    X'00'
00001B2F  E2                                       1394+         DC    CL1'S'            Y = skip cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001B30  05                                       1395+          DC    HL1'5'            m3
00001B31  01                                       1396+          DC    HL1'1'            m4
00001B32  08                                       1397+FLG12     DC    X'08'             expected FPC flags
00001B33  05                                       1398+VXC12     DC    X'05'             expected VXC
00001B34  00001BEC                                 1399+V2_12     DC    A(RE12+16)        address of v2: 16-byte packed decimal
00001B38  E5C3D5C6 40404040                        1400+          DC    CL8'VCNF'         instruction name
00001B40  00000010                                 1401+          DC    A(16)             result length
00001B44  00001BDC                                 1402+          DC    A(RE12)           address of expected resul
00001B48  00000000 00000000                        1403+          DS    FD                gap
00001B50  00000000 00000000                        1404+V1O12     DS    XL16              V1 output
00001B58  00000000 00000000
00001B60  00000000 00000000                        1405+          DS    FD                   gap
00001B68  00000000                                 1406+FPC_R_12  DS    F                 FPC after instruction
00001B70  00000000 00000000                        1407+          DS    FD                   gap
00001B78  40404040 40404040                        1408+          DC    CL8' '            was cross check skipped?
00001B80  00000000 00000000                        1409+          DS    FD                   gap
00001B88  00000000 00000000                        1410+XCO12     DS    XL16              Cross check Output
00001B90  00000000 00000000
00001B98  00000000 00000000                        1411+          DS    FD                   gap
00001BA0  00000000                                 1412+FPC_XC_12 DS    F                 FPC after cross check
00001BA8  00000000 00000000                        1413+          DS    FD                   gap
00001BB0  00000000                                 1414+          DS    F                 debug area
00001BB4  00000000                                 1415+          DS    F
                                                   1416+*
00001BB8                                           1417+X12       DS    0F
00001BB8  B29D 85A4                     000007A4   1418+          LFPC  FPCINIT           initialize FPC
                                                   1419+*          LFPC  =XL4'08000000'          set trap exception
00001BBC  E320 500C 0014                00001B34   1420+          LGF   R2,V2_12          get v2
00001BC2  E762 0000 0806                00000000   1421+          VL    V22,0(R2)
00001BC8  E666 0001 5C55                           1422+          VCNF  V22,V22,5,1       test instruction (dest is source)
00001BCE  B29C 5040                     00001B68   1423+          STFPC FPC_R_12          save FPC
00001BD2  E760 5028 080E                00001B50   1424+          VST   V22,V1O12         save instruction result
00001BD8  07FB                                     1425+          BR    R11               return
00001BDC                                           1426+RE12      DS    0F                expected 16 byte result
00001BDC                                           1427+          DROP  R5
00001BDC  00000000 00000000                        1428           DC    XL16'00000000000000000000000000000000'
00001BE4  00000000 00000000
00001BEC  00010000 00000000                        1429           DC    XL16'00010000000000000000000000000F000'
00001BF4  00000000 0000F000
                                                   1430
                                                   1431 * inexact - bad m4
                                                   1432           VRR_A VCNF,0,5,08,05,S                    skip xc - inexact
00001C00                                           1433+          DS    0FD
00001C00                        00001C00           1434+          USING *,R5              base for test data and test routine
00001C00  00001C90                                 1435+T13       DC    A(X13)            address of test routine
00001C04  000D                                     1436+          DC    H'13'             test number
00001C06  00                                       1437+          DC    X'00'
00001C07  E2                                       1438+          DC    CL1'S'            Y = skip cross check
00001C08  00                                       1439+          DC    HL1'0'            m3
00001C09  05                                       1440+          DC    HL1'5'            m4
00001C0A  08                                       1441+FLG13     DC    X'08'             expected FPC flags
00001C0B  05                                       1442+VXC13     DC    X'05'             expected VXC
00001C0C  00001CC4                                 1443+V2_13     DC    A(RE13+16)        address of v2: 16-byte packed decimal
00001C10  E5C3D5C6 40404040                        1444+          DC    CL8'VCNF'         instruction name
00001C18  00000010                                 1445+          DC    A(16)             result length
00001C1C  00001CB4                                 1446+          DC    A(RE13)           address of expected resul
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001C20  00000000 00000000                       1447+          DS    FD                gap
00001C28  00000000 00000000                       1448+V1O13     DS    XL16              V1 output
00001C30  00000000 00000000
00001C38  00000000 00000000                       1449+          DS    FD                   gap
00001C40  00000000                                1450+FPC_R_13  DS    F                 FPC after instruction
00001C48  00000000 00000000                       1451+          DS    FD                   gap
00001C50  40404040 40404040                       1452+          DC    CL8' '            was cross check skipped?
00001C58  00000000 00000000                       1453+          DS    FD                   gap
00001C60  00000000 00000000                       1454+XCO13     DS    XL16              Cross check Output
00001C68  00000000 00000000
00001C70  00000000 00000000                       1455+          DS    FD                   gap
00001C78  00000000                                1456+FPC_XC_13 DS    F                 FPC after cross check
00001C80  00000000 00000000                       1457+          DS    FD                   gap
00001C88  00000000                                1458+          DS    F                 debug area
00001C8C  00000000                                1459+          DS    F
                                                  1460+*
00001C90                                          1461+X13       DS    0F
00001C90  B29D 85A4                    000007A4   1462+          LFPC  FPCINIT           initialize FPC
                                                  1463+*          LFPC  =XL4'08000000'          set trap exception
00001C94  E320 500C 0014               00001C0C   1464+          LGF   R2,V2_13          get v2
00001C9A  E762 0000 0806               00000000   1465+          VL    V22,0(R2)
00001CA0  E666 0005 0C55                          1466+          VCNF  V22,V22,0,5       test instruction (dest is source)
00001CA6  B29C 5040                    00001C40   1467+          STFPC FPC_R_13          save FPC
00001CAA  E760 5028 080E               00001C28   1468+          VST   V22,V1O13         save instruction result
00001CB0  07FB                                    1469+          BR    R11               return
00001CB4                                          1470+RE13      DS    0F                expected 16 byte result
00001CB4                                          1471+          DROP  R5
00001CB4  00000000 00000000                       1472           DC    XL16'00000000000000000000000000000000'
00001CBC  00000000 00000000
00001CC4  00010000 00000000                       1473           DC    XL16'00010000000000000000000000000F000'
00001CCC  00000000 0000F000
                                                  1474
                                                  1475 * more tests
                                                  1476 * +3.140625, -3.140625
                                                  1477           VRR_A VCNF,0,1,00,00,N
00001CD8                                          1478+          DS    0FD
00001CD8                       00001CD8           1479+          USING *,R5              base for test data and test routine
00001CD8  00001D68                                1480+T14       DC    A(X14)            address of test routine
00001CDC  000E                                    1481+          DC    H'14'             test number
00001CDE  00                                      1482+          DC    X'00'
00001CDF  D5                                      1483+          DC    CL1'N'            Y = skip cross check
00001CE0  00                                      1484+          DC    HL1'0'            m3
00001CE1  01                                      1485+          DC    HL1'1'            m4
00001CE2  00                                      1486+FLG14     DC    X'00'             expected FPC flags
00001CE3  00                                      1487+VXC14     DC    X'00'             expected VXC
00001CE4  00001D9C                                1488+V2_14     DC    A(RE14+16)        address of v2: 16-byte packed decimal
00001CE8  E5C3D5C6 40404040                       1489+          DC    CL8'VCNF'         instruction name
00001CF0  00000010                                1490+          DC    A(16)             result length
00001CF4  00001D8C                                1491+          DC    A(RE14)           address of expected resul
00001CF8  00000000 00000000                       1492+          DS    FD                gap
00001D00  00000000 00000000                       1493+V1O14     DS    XL16              V1 output
00001D08  00000000 00000000
00001D10  00000000 00000000                       1494+          DS    FD                   gap
00001D18  00000000                                1495+FPC_R_14  DS    F                 FPC after instruction
00001D20  00000000 00000000                       1496+          DS    FD                   gap
00001D28  40404040 40404040                       1497+          DC    CL8' '            was cross check skipped?
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001D30  00000000 00000000                       1498+          DS    FD                   gap
00001D38  00000000 00000000                       1499+XCO14     DS    XL16               Cross check Output
00001D40  00000000 00000000
00001D48  00000000 00000000                       1500+          DS    FD                   gap
00001D50  00000000                                1501+FPC_XC_14 DS    F                  FPC after cross check
00001D58  00000000 00000000                       1502+          DS    FD                   gap
00001D60  00000000                                1503+          DS    F                  debug area
00001D64  00000000                                1504+          DS    F
                                                  1505+*
00001D68                                          1506+X14       DS    0F
00001D68  B29D 85A4                     000007A4  1507+          LFPC  FPCINIT            initialize FPC
                                                  1508+*          LFPC  =XL4'08000000'          set trap exception
00001D6C  E320 500C 0014                00001CE4  1509+          LGF   R2,V2_14           get v2
00001D72  E762 0000 0806                00000000  1510+          VL    V22,0(R2)
00001D78  E666 0001 0C55                          1511+          VCNF  V22,V22,0,1        test instruction (dest is source)
00001D7E  B29C 5040                     00001D18  1512+          STFPC FPC_R_14           save FPC
00001D82  E760 5028 080E                00001D00  1513+          VST   V22,V1O14          save instruction result
00001D88  07FB                                    1514+          BR    R11                return
00001D8C                                          1515+RE14      DS    0F                 expected 16 byte result
00001D8C                                          1516+          DROP  R5
00001D8C  42240000 C2240000                       1517           DC    XL16'42240000C224000000000000000D800'
00001D94  00000000 0000D800
00001D9C  44480000 C4480000                       1518           DC    XL16'44480000C448000000000000000F000'
00001DA4  00000000 0000F000
                                                  1519
                                                  1520 * +27.15625, -27.15625                          skip xc - lost digits
                                                  1521           VRR_A VCNF,0,1,00,00,S
00001DB0                                          1522+          DS    0FD
00001DB0                        00001DB0          1523+          USING *,R5               base for test data and test routine
00001DB0  00001E40                                1524+T15       DC    A(X15)             address of test routine
00001DB4  000F                                    1525+          DC    H'15'              test number
00001DB6  00                                      1526+          DC    X'00'
00001DB7  E2                                      1527+          DC    CL1'S'             Y = skip cross check
00001DB8  00                                      1528+          DC    HL1'0'             m3
00001DB9  01                                      1529+          DC    HL1'1'             m4
00001DBA  00                                      1530+FLG15     DC    X'00'              expected FPC flags
00001DBB  00                                      1531+VXC15     DC    X'00'              expected VXC
00001DBC  00001E74                                1532+V2_15     DC    A(RE15+16)         address of v2: 16-byte packed decimal
00001DC0  E5C3D5C6 40404040                       1533+          DC    CL8'VCNF'          instruction name
00001DC8  00000010                                1534+          DC    A(16)              result length
00001DCC  00001E64                                1535+          DC    A(RE15)            address of expected resul
00001DD0  00000000 00000000                       1536+          DS    FD                 gap
00001DD8  00000000 00000000                       1537+V1O15     DS    XL16               V1 output
00001DE0  00000000 00000000
00001DE8  00000000 00000000                       1538+          DS    FD                   gap
00001DF0  00000000                                1539+FPC_R_15  DS    F                  FPC after instruction
00001DF8  00000000 00000000                       1540+          DS    FD                   gap
00001E00  40404040 40404040                       1541+          DC    CL8' '             was cross check skipped?
00001E08  00000000 00000000                       1542+          DS    FD                   gap
00001E10  00000000 00000000                       1543+XCO15     DS    XL16               Cross check Output
00001E18  00000000 00000000
00001E20  00000000 00000000                       1544+          DS    FD                   gap
00001E28  00000000                                1545+FPC_XC_15 DS    F                  FPC after cross check
00001E30  00000000 00000000                       1546+          DS    FD                   gap
00001E38  00000000                                1547+          DS    F                  debug area
00001E3C  00000000                                1548+          DS    F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  1549+*
00001E40                                          1550+X15      DS    0F
00001E40  B29D 85A4                     000007A4  1551+         LFPC  FPCINIT           initialize FPC
                                                  1552+*         LFPC  =XL4'08000000'         set trap exception
00001E44  E320 500C 0014                00001DBC  1553+         LGF   R2,V2_15          get v2
00001E4A  E762 0000 0806                00000000  1554+         VL    V22,0(R2)
00001E50  E666 0001 0C55                          1555+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001E56  B29C 5040                     00001DF0  1556+         STFPC FPC_R_15          save FPC
00001E5A  E760 5028 080E                00001DD8  1557+         VST   V22,V1O15         save instruction result
00001E60  07FB                                    1558+         BR    R11               return
00001E64                                          1559+RE15     DS    0F                expected 16 byte result
00001E64                                          1560+         DROP  R5
00001E64  2F650000 AF650000                       1561          DC    XL16'2F650000AF65000000000000000D800'
00001E6C  00000000 0000D800
00001E74  1EC90000 9EC90000                       1562          DC    XL16'1EC900009EC90000000000000000F000'
00001E7C  00000000 0000F000
                                                  1563
                                                  1564 * +65504, -65504
                                                  1565          VRR_A VCNF,0,1,00,00,N
00001E88                                          1566+         DS    0FD
00001E88                        00001E88          1567+         USING *,R5              base for test data and test routine
00001E88  00001F18                                1568+T16      DC    A(X16)            address of test routine
00001E8C  0010                                    1569+         DC    H'16'             test number
00001E8E  00                                      1570+         DC    X'00'
00001E8F  D5                                      1571+         DC    CL1'N'            Y = skip cross check
00001E90  00                                      1572+         DC    HL1'0'            m3
00001E91  01                                      1573+         DC    HL1'1'            m4
00001E92  00                                      1574+FLG16    DC    X'00'             expected FPC flags
00001E93  00                                      1575+VXC16    DC    X'00'             expected VXC
00001E94  00001F4C                                1576+V2_16    DC    A(RE16+16)        address of v2: 16-byte packed decimal
00001E98  E5C3D5C6 40404040                       1577+         DC    CL8'VCNF'         instruction name
00001EA0  00000010                                1578+         DC    A(16)             result length
00001EA4  00001F3C                                1579+         DC    A(RE16)           address of expected resul
00001EA8  00000000 00000000                       1580+         DS    FD                gap
00001EB0  00000000 00000000                       1581+V1O16    DS    XL16              V1 output
00001EB8  00000000 00000000
00001EC0  00000000 00000000                       1582+         DS    FD                   gap
00001EC8  00000000                                1583+FPC_R_16 DS    F                 FPC after instruction
00001ED0  00000000 00000000                       1584+         DS    FD                   gap
00001ED8  40404040 40404040                       1585+         DC    CL8' '            was cross check skipped?
00001EE0  00000000 00000000                       1586+         DS    FD                   gap
00001EE8  00000000 00000000                       1587+XCO16    DS    XL16              Cross check Output
00001EF0  00000000 00000000
00001EF8  00000000 00000000                       1588+         DS    FD                   gap
00001F00  00000000                                1589+FPC_XC_16 DS   F                 FPC after cross check
00001F08  00000000 00000000                       1590+         DS    FD                   gap
00001F10  00000000                                1591+         DS    F                 debug area
00001F14  00000000                                1592+         DS    F
                                                  1593+*
00001F18                                          1594+X16      DS    0F
00001F18  B29D 85A4                     000007A4  1595+         LFPC  FPCINIT           initialize FPC
                                                  1596+*         LFPC  =XL4'08000000'         set trap exception
00001F1C  E320 500C 0014                00001E94  1597+         LGF   R2,V2_16          get v2
00001F22  E762 0000 0806                00000000  1598+         VL    V22,0(R2)
00001F28  E666 0001 0C55                          1599+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001F2E  B29C 5040                     00001EC8  1600+         STFPC FPC_R_16          save FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001F32  E760 5028 080E                00001EB0  1601+         VST   V22,V1O16         save instruction result
00001F38  07FB                                    1602+         BR    R11               return
00001F3C                                          1603+RE16     DS    0F                expected 16 byte result
00001F3C                                          1604+         DROP  R5
00001F3C  5E000000 DE000000                       1605          DC    XL16'5E000000DE000000000000000000D800'
00001F44  00000000 0000D800
00001F4C  7BFF0000 FBFF0000                       1606          DC    XL16'7BFF0000FBFF0000000000000000F000'
00001F54  00000000 0000F000
                                                  1607
                                                  1608 * +Normal, -Normal
                                                  1609          VRR_A VCNF,0,1,00,00,N
00001F60                                          1610+         DS    0FD
00001F60                      00001F60            1611+         USING *,R5              base for test data and test routine
00001F60  00001FF0                                1612+T17      DC    A(X17)            address of test routine
00001F64  0011                                    1613+         DC    H'17'             test number
00001F66  00                                      1614+         DC    X'00'
00001F67  D5                                      1615+         DC    CL1'N'            Y = skip cross check
00001F68  00                                      1616+         DC    HL1'0'            m3
00001F69  01                                      1617+         DC    HL1'1'            m4
00001F6A  00                                      1618+FLG17    DC    X'00'             expected FPC flags
00001F6B  00                                      1619+VXC17    DC    X'00'             expected VXC
00001F6C  00002024                                1620+V2_17    DC    A(RE17+16)        address of v2: 16-byte packed decimal
00001F70  E5C3D5C6 40404040                       1621+         DC    CL8'VCNF'         instruction name
00001F78  00000010                                1622+         DC    A(16)             result length
00001F7C  00002014                                1623+         DC    A(RE17)           address of expected resul
00001F80  00000000 00000000                       1624+         DS    FD                gap
00001F88  00000000 00000000                       1625+V1O17    DS    XL16              V1 output
00001F90  00000000 00000000
00001F98  00000000 00000000                       1626+         DS    FD                   gap
00001FA0  00000000                                1627+FPC_R_17 DS    F                 FPC after instruction
00001FA8  00000000 00000000                       1628+         DS    FD                   gap
00001FB0  40404040 40404040                       1629+         DC    CL8' '            was cross check skipped?
00001FB8  00000000 00000000                       1630+         DS    FD                   gap
00001FC0  00000000 00000000                       1631+XCO17    DS    XL16              Cross check Output
00001FC8  00000000 00000000
00001FD0  00000000 00000000                       1632+         DS    FD                   gap
00001FD8  00000000                                1633+FPC_XC_17 DS   F                 FPC after cross check
00001FE0  00000000 00000000                       1634+         DS    FD                   gap
00001FE8  00000000                                1635+         DS    F                 debug area
00001FEC  00000000                                1636+         DS    F
                                                  1637+*
00001FF0                                          1638+X17      DS    0F
00001FF0  B29D 85A4                     000007A4  1639+         LFPC  FPCINIT           initialize FPC
                                                  1640+*         LFPC  =XL4'08000000'         set trap exception
00001FF4  E320 500C 0014                00001F6C  1641+         LGF   R2,V2_17          get v2
00001FFA  E762 0000 0806                00000000  1642+         VL    V22,0(R2)
00002000  E666 0001 0C55                          1643+         VCNF  V22,V22,0,1       test instruction (dest is source)
00002006  B29C 5040                     00001FA0  1644+         STFPC FPC_R_17          save FPC
0000200A  E760 5028 080E                00001F88  1645+         VST   V22,V1O17         save instruction result
00002010  07FB                                    1646+         BR    R11               return
00002014                                          1647+RE17     DS    0F                expected 16 byte result
00002014                                          1648+         DROP  R5
00002014  40800000 C0800000                       1649          DC    XL16'40800000C0800000000000000000D800'
0000201C  00000000 0000D800
00002024  41000000 C1000000                       1650          DC    XL16'41000000C1000000000000000000F000'
0000202C  00000000 0000F000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   1651
                                                   1652 * +Subnormal, -Subnormal
                                                   1653          VRR_A VCNF,0,1,00,00,N
00002038                                           1654+         DS    0FD
00002038                       00002038            1655+         USING *,R5              base for test data and test routine
00002038  000020C8                                 1656+T18      DC    A(X18)            address of test routine
0000203C  0012                                     1657+         DC    H'18'             test number
0000203E  00                                       1658+         DC    X'00'
0000203F  D5                                       1659+         DC    CL1'N'            Y = skip cross check
00002040  00                                       1660+         DC    HL1'0'            m3
00002041  01                                       1661+         DC    HL1'1'            m4
00002042  00                                       1662+FLG18    DC    X'00'             expected FPC flags
00002043  00                                       1663+VXC18    DC    X'00'             expected VXC
00002044  000020FC                                 1664+V2_18    DC    A(RE18+16)        address of v2: 16-byte packed decimal
00002048  E5C3D5C6 40404040                        1665+         DC    CL8'VCNF'         instruction name
00002050  00000010                                 1666+         DC    A(16)             result length
00002054  000020EC                                 1667+         DC    A(RE18)           address of expected resul
00002058  00000000 00000000                        1668+         DS    FD                gap
00002060  00000000 00000000                        1669+V1O18    DS    XL16              V1 output
00002068  00000000 00000000
00002070  00000000 00000000                        1670+         DS    FD                   gap
00002078  00000000                                 1671+FPC_R_18 DS    F                 FPC after instruction
00002080  00000000 00000000                        1672+         DS    FD                   gap
00002088  40404040 40404040                        1673+         DC    CL8' '            was cross check skipped?
00002090  00000000 00000000                        1674+         DS    FD                   gap
00002098  00000000 00000000                        1675+XCO18    DS    XL16              Cross check Output
000020A0  00000000 00000000
000020A8  00000000 00000000                        1676+         DS    FD                   gap
000020B0  00000000                                 1677+FPC_XC_18 DS   F                 FPC after cross check
000020B8  00000000 00000000                        1678+         DS    FD                   gap
000020C0  00000000                                 1679+         DS    F                 debug area
000020C4  00000000                                 1680+         DS    F
                                                   1681+*
000020C8                                           1682+X18      DS    0F
000020C8  B29D 85A4                     000007A4   1683+         LFPC  FPCINIT           initialize FPC
                                                   1684+*         LFPC  =XL4'08000000'         set trap exception
000020CC  E320 500C 0014                00002044   1685+         LGF   R2,V2_18          get v2
000020D2  E762 0000 0806                00000000   1686+         VL    V22,0(R2)
000020D8  E666 0001 0C55                           1687+         VCNF  V22,V22,0,1       test instruction (dest is source)
000020DE  B29C 5040                     00002078   1688+         STFPC FPC_R_18          save FPC
000020E2  E760 5028 080E                00002060   1689+         VST   V22,V1O18         save instruction result
000020E8  07FB                                     1690+         BR    R11               return
000020EC                                           1691+RE18     DS    0F                expected 16 byte result
000020EC                                           1692+         DROP  R5
000020EC  21FF0000 A1FF0000                        1693          DC    XL16'21FF0000A1FF000000000000000D800'
000020F4  00000000 0000D800
000020FC  03FF0000 83FF0000                        1694          DC    XL16'03FF000083FF000000000000000F000'
00002104  00000000 0000F000
                                                   1695
                                                   1696 * +Infinity, -Infinity                          skip xc - infinity
                                                   1697          VRR_A VCNF,0,1,20,23,S
00002110                                           1698+         DS    0FD
00002110                       00002110            1699+         USING *,R5              base for test data and test routine
00002110  000021A0                                 1700+T19      DC    A(X19)            address of test routine
00002114  0013                                     1701+         DC    H'19'             test number
00002116  00                                       1702+         DC    X'00'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002117  E2                                       1703+          DC    CL1'S'              Y = skip cross check
00002118  00                                       1704+          DC    HL1'0'              m3
00002119  01                                       1705+          DC    HL1'1'              m4
0000211A  20                                       1706+FLG19     DC    X'20'               expected FPC flags
0000211B  23                                       1707+VXC19     DC    X'23'               expected VXC
0000211C  000021D4                                 1708+V2_19     DC    A(RE19+16)          address of v2: 16-byte packed decimal
00002120  E5C3D5C6 40404040                        1709+          DC    CL8'VCNF'           instruction name
00002128  00000010                                 1710+          DC    A(16)               result length
0000212C  000021C4                                 1711+          DC    A(RE19)             address of expected resul
00002130  00000000 00000000                        1712+          DS    FD                  gap
00002138  00000000 00000000                        1713+V1O19     DS    XL16                V1 output
00002140  00000000 00000000
00002148  00000000 00000000                        1714+          DS    FD                     gap
00002150  00000000                                 1715+FPC_R_19 DS    F                   FPC after instruction
00002158  00000000 00000000                        1716+          DS    FD                     gap
00002160  40404040 40404040                        1717+          DC    CL8' '              was cross check skipped?
00002168  00000000 00000000                        1718+          DS    FD                     gap
00002170  00000000 00000000                        1719+XCO19     DS    XL16                Cross check Output
00002178  00000000 00000000
00002180  00000000 00000000                        1720+          DS    FD                     gap
00002188  00000000                                 1721+FPC_XC_19 DS    F                   FPC after cross check
00002190  00000000 00000000                        1722+          DS    FD                     gap
00002198  00000000                                 1723+          DS    F                   debug area
0000219C  00000000                                 1724+          DS    F
                                                   1725+*
000021A0                                           1726+X19       DS    0F
000021A0  B29D 85A4                     000007A4   1727+          LFPC  FPCINIT             initialize FPC
                                                   1728+*          LFPC  =XL4'08000000'            set trap exception
000021A4  E320 500C 0014                0000211C   1729+          LGF   R2,V2_19            get v2
000021AA  E762 0000 0806                00000000   1730+          VL    V22,0(R2)
000021B0  E666 0001 0C55                           1731+          VCNF  V22,V22,0,1         test instruction (dest is source)
000021B6  B29C 5040                     00002150   1732+          STFPC FPC_R_19            save FPC
000021BA  E760 5028 080E                00002138   1733+          VST   V22,V1O19           save instruction result
000021C0  07FB                                     1734+          BR    R11                 return
000021C4                                           1735+RE19      DS    0F                  expected 16 byte result
000021C4                                           1736+          DROP  R5
000021C4  7FFF0000 FFFF0000                        1737           DC    XL16'7FFF0000FFFF0000000000000000D800'
000021CC  00000000 0000D800
000021D4  7C000000 FC000000                        1738           DC    XL16'7C000000FC00000000000000000F000'
000021DC  00000000 0000F000
                                                   1739
                                                   1740 * +QNaN, -QNaN                                   skip xc - NaN
                                                   1741           VRR_A VCNF,0,1,80,21,S
000021E8                                           1742+          DS    0FD
000021E8                        000021E8           1743+          USING *,R5                base for test data and test routine
000021E8  00002278                                 1744+T20       DC    A(X20)              address of test routine
000021EC  0014                                     1745+          DC    H'20'               test number
000021EE  00                                       1746+          DC    X'00'
000021EF  E2                                       1747+          DC    CL1'S'              Y = skip cross check
000021F0  00                                       1748+          DC    HL1'0'              m3
000021F1  01                                       1749+          DC    HL1'1'              m4
000021F2  80                                       1750+FLG20     DC    X'80'               expected FPC flags
000021F3  21                                       1751+VXC20     DC    X'21'               expected VXC
000021F4  000022AC                                 1752+V2_20     DC    A(RE20+16)          address of v2: 16-byte packed decimal
000021F8  E5C3D5C6 40404040                        1753+          DC    CL8'VCNF'           instruction name
00002200  00000010                                 1754+          DC    A(16)               result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002204  0000229C                                1755+          DC    A(RE20)            address of expected resul
00002208  00000000 00000000                       1756+          DS    FD                 gap
00002210  00000000 00000000                       1757+V1O20     DS    XL16               V1 output
00002218  00000000 00000000
00002220  00000000 00000000                       1758+          DS    FD                    gap
00002228  00000000                                1759+FPC_R_20  DS    F                  FPC after instruction
00002230  00000000 00000000                       1760+          DS    FD                    gap
00002238  40404040 40404040                       1761+          DC    CL8' '             was cross check skipped?
00002240  00000000 00000000                       1762+          DS    FD                    gap
00002248  00000000 00000000                       1763+XCO20     DS    XL16               Cross check Output
00002250  00000000 00000000
00002258  00000000 00000000                       1764+          DS    FD                    gap
00002260  00000000                                1765+FPC_XC_20 DS    F                  FPC after cross check
00002268  00000000 00000000                       1766+          DS    FD                    gap
00002270  00000000                                1767+          DS    F                  debug area
00002274  00000000                                1768+          DS    F
                                                  1769+*
00002278                                          1770+X20       DS    0F
00002278  B29D 85A4                    000007A4   1771+          LFPC  FPCINIT            initialize FPC
                                                  1772+*          LFPC  =XL4'08000000'          set trap exception
0000227C  E320 500C 0014               000021F4   1773+          LGF   R2,V2_20           get v2
00002282  E762 0000 0806               00000000   1774+          VL    V22,0(R2)
00002288  E666 0001 0C55                          1775+          VCNF  V22,V22,0,1        test instruction (dest is source)
0000228E  B29C A028                    00002228   1776+          STFPC FPC_R_20           save FPC
00002292  E760 A010 080E               00002210   1777+          VST   V22,V1O20          save instruction result
00002298  07FB                                    1778+          BR    R11                return
0000229C                                          1779+RE20      DS    0F                 expected 16 byte result
0000229C                                          1780+          DROP  R5
0000229C  7FFF0000 FFFF0000                       1781           DC    XL16'7FFF0000FFFF000000000000000D800'
000022A4  00000000 0000D800
000022AC  7E080000 FE080000                       1782           DC    XL16'7E080000FE080000000000000000F000'
000022B4  00000000 0000F000
                                                  1783
                                                  1784 * +SNaN, -SNaN                                  skip xc - NaN
                                                  1785           VRR_A VCNF,0,1,80,21,S
000022C0                                          1786+          DS    0FD
000022C0                       000022C0           1787+          USING *,R5               base for test data and test routine
000022C0  00002350                                1788+T21       DC    A(X21)             address of test routine
000022C4  0015                                    1789+          DC    H'21'              test number
000022C6  00                                      1790+          DC    X'00'
000022C7  E2                                      1791+          DC    CL1'S'             Y = skip cross check
000022C8  00                                      1792+          DC    HL1'0'             m3
000022C9  01                                      1793+          DC    HL1'1'             m4
000022CA  80                                      1794+FLG21     DC    X'80'              expected FPC flags
000022CB  21                                      1795+VXC21     DC    X'21'              expected VXC
000022CC  00002384                                1796+V2_21     DC    A(RE21+16)         address of v2: 16-byte packed decimal
000022D0  E5C3D5C6 40404040                       1797+          DC    CL8'VCNF'          instruction name
000022D8  00000010                                1798+          DC    A(16)              result length
000022DC  00002374                                1799+          DC    A(RE21)            address of expected resul
000022E0  00000000 00000000                       1800+          DS    FD                 gap
000022E8  00000000 00000000                       1801+V1O21     DS    XL16               V1 output
000022F0  00000000 00000000
000022F8  00000000 00000000                       1802+          DS    FD                    gap
00002300  00000000                                1803+FPC_R_21  DS    F                  FPC after instruction
00002308  00000000 00000000                       1804+          DS    FD                    gap
00002310  40404040 40404040                       1805+          DC    CL8' '             was cross check skipped?
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002318  00000000 00000000                       1806+          DS    FD                   gap
00002320  00000000 00000000                       1807+XCO21     DS    XL16               Cross check Output
00002328  00000000 00000000
00002330  00000000 00000000                       1808+          DS    FD                   gap
00002338  00000000                                1809+FPC_XC_21 DS    F                  FPC after cross check
00002340  00000000 00000000                       1810+          DS    FD                   gap
00002348  00000000                                1811+          DS    F                  debug area
0000234C  00000000                                1812+          DS    F
                                                  1813+*
00002350                                          1814+X21       DS    0F
00002350  B29D 85A4                    000007A4   1815+          LFPC  FPCINIT            initialize FPC
                                                  1816+*          LFPC  =XL4'08000000'         set trap exception
00002354  E320 500C 0014               000022CC   1817+          LGF   R2,V2_21           get v2
0000235A  E762 0000 0806               00000000   1818+          VL    V22,0(R2)
00002360  E666 0001 0C55                          1819+          VCNF  V22,V22,0,1        test instruction (dest is source)
00002366  B29C 5040                    00002300   1820+          STFPC FPC_R_21           save FPC
0000236A  E760 5028 080E               000022E8   1821+          VST   V22,V1O21          save instruction result
00002370  07FB                                    1822+          BR    R11                return
00002374                                          1823+RE21      DS    0F                 expected 16 byte result
00002374                                          1824+          DROP  R5
00002374  7FFF0000 FFFF0000                       1825           DC    XL16'7FFF0000FFFF000000000000000D800'
0000237C  00000000 0000D800
00002384  7C080000 FC080000                       1826           DC    XL16'7C080000FC080000000000000000F000'
0000238C  00000000 0000F000
                                                  1827
                                                  1828 * multiple exception types
                                                  1829 * +Infinity,  -QNaN                                skip xc - infinity
                                                  1830           VRR_A VCNF,0,1,A0,21,S
00002398                                          1831+          DS    0FD
00002398                       00002398           1832+          USING *,R5               base for test data and test routine
00002398  00002428                                1833+T22       DC    A(X22)             address of test routine
0000239C  0016                                    1834+          DC    H'22'              test number
0000239E  00                                      1835+          DC    X'00'
0000239F  E2                                      1836+          DC    CL1'S'             Y = skip cross check
000023A0  00                                      1837+          DC    HL1'0'             m3
000023A1  01                                      1838+          DC    HL1'1'             m4
000023A2  A0                                      1839+FLG22     DC    X'A0'              expected FPC flags
000023A3  21                                      1840+VXC22     DC    X'21'              expected VXC
000023A4  0000245C                                1841+V2_22     DC    A(RE22+16)         address of v2: 16-byte packed decimal
000023A8  E5C3D5C6 40404040                       1842+          DC    CL8'VCNF'          instruction name
000023B0  00000010                                1843+          DC    A(16)              result length
000023B4  0000244C                                1844+          DC    A(RE22)            address of expected resul
000023B8  00000000 00000000                       1845+          DS    FD                 gap
000023C0  00000000 00000000                       1846+V1O22     DS    XL16               V1 output
000023C8  00000000 00000000
000023D0  00000000 00000000                       1847+          DS    FD                   gap
000023D8  00000000                                1848+FPC_R_22  DS    F                  FPC after instruction
000023E0  00000000 00000000                       1849+          DS    FD                   gap
000023E8  40404040 40404040                       1850+          DC    CL8' '             was cross check skipped?
000023F0  00000000 00000000                       1851+          DS    FD                   gap
000023F8  00000000 00000000                       1852+XCO22     DS    XL16               Cross check Output
00002400  00000000 00000000
00002408  00000000 00000000                       1853+          DS    FD                   gap
00002410  00000000                                1854+FPC_XC_22 DS    F                  FPC after cross check
00002418  00000000 00000000                       1855+          DS    FD                   gap
00002420  00000000                                1856+          DS    F                  debug area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002424  00000000                                1857+         DS    F
                                                  1858+*
00002428                                          1859+X22      DS    0F
00002428  B29D 85A4                     000007A4  1860+         LFPC  FPCINIT           initialize FPC
                                                  1861+*         LFPC  =XL4'08000000'         set trap exception
0000242C  E320 500C 0014                000023A4  1862+         LGF   R2,V2_22          get v2
00002432  E762 0000 0806                00000000  1863+         VL    V22,0(R2)
00002438  E666 0001 0C55                          1864+         VCNF  V22,V22,0,1       test instruction (dest is source)
0000243E  B29C 5040                     000023D8  1865+         STFPC FPC_R_22          save FPC
00002442  E760 5028 080E                000023C0  1866+         VST   V22,V1O22         save instruction result
00002448  07FB                                    1867+         BR    R11               return
0000244C                                          1868+RE22     DS    0F                expected 16 byte result
0000244C                                          1869+         DROP  R5
0000244C  7FFF0000 FFFF0000                       1870          DC    XL16'7FFF0000FFFF000000000000000D800'
00002454  00000000 0000D800
0000245C  7C000000 FE080000                       1871          DC    XL16'7C000000FE080000000000000000F000'
00002464  00000000 0000F000
                                                  1872
                                                  1873 * +Infinity,  -QNaN, -SNaN                         skip xc - infinity
                                                  1874          VRR_A VCNF,0,1,A0,41,S
00002470                                          1875+         DS    0FD
00002470                        00002470          1876+         USING *,R5              base for test data and test routine
00002470  00002500                                1877+T23      DC    A(X23)            address of test routine
00002474  0017                                    1878+         DC    H'23'             test number
00002476  00                                      1879+         DC    X'00'
00002477  E2                                      1880+         DC    CL1'S'            Y = skip cross check
00002478  00                                      1881+         DC    HL1'0'            m3
00002479  01                                      1882+         DC    HL1'1'            m4
0000247A  A0                                      1883+FLG23    DC    X'A0'             expected FPC flags
0000247B  41                                      1884+VXC23    DC    X'41'             expected VXC
0000247C  00002534                                1885+V2_23    DC    A(RE23+16)        address of v2: 16-byte packed decimal
00002480  E5C3D5C6 40404040                       1886+         DC    CL8'VCNF'         instruction name
00002488  00000010                                1887+         DC    A(16)             result length
0000248C  00002524                                1888+         DC    A(RE23)           address of expected resul
00002490  00000000 00000000                       1889+         DS    FD                gap
00002498  00000000 00000000                       1890+V1O23    DS    XL16              V1 output
000024A0  00000000 00000000
000024A8  00000000 00000000                       1891+         DS    FD                   gap
000024B0  00000000                                1892+FPC_R_23 DS    F                 FPC after instruction
000024B8  00000000 00000000                       1893+         DS    FD                   gap
000024C0  40404040 40404040                       1894+         DC    CL8' '            was cross check skipped?
000024C8  00000000 00000000                       1895+         DS    FD                   gap
000024D0  00000000 00000000                       1896+XCO23    DS    XL16              Cross check Output
000024D8  00000000 00000000
000024E0  00000000 00000000                       1897+         DS    FD                   gap
000024E8  00000000                                1898+FPC_XC_23 DS   F                 FPC after cross check
000024F0  00000000 00000000                       1899+         DS    FD                   gap
000024F8  00000000                                1900+         DS    F                 debug area
000024FC  00000000                                1901+         DS    F
                                                  1902+*
00002500                                          1903+X23      DS    0F
00002500  B29D 85A4                     000007A4  1904+         LFPC  FPCINIT           initialize FPC
                                                  1905+*         LFPC  =XL4'08000000'         set trap exception
00002504  E320 500C 0014                0000247C  1906+         LGF   R2,V2_23          get v2
0000250A  E762 0000 0806                00000000  1907+         VL    V22,0(R2)
00002510  E666 0001 0C55                          1908+         VCNF  V22,V22,0,1       test instruction (dest is source)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002516  B29C 5040                     000024B0  1909+         STFPC FPC_R_23          save FPC
0000251A  E760 5028 080E                00002498  1910+         VST   V22,V1O23         save instruction result
00002520  07FB                                    1911+         BR    R11               return
00002524                                          1912+RE23     DS    0F                expected 16 byte result
00002524                                          1913+         DROP  R5
00002524  7FFF0000 FFFF0000                       1914          DC    XL16'7FFF0000FFFF0000FFFF00000000D800'
0000252C  FFFF0000 0000D800
00002534  7C000000 FE080000                       1915          DC    XL16'7C000000FE080000FC0800000000F000'
0000253C  FC080000 0000F000
                                                  1916
                                                  1917 *-------------------------------------------------------------------
                                                  1918 * VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                  1919 *-------------------------------------------------------------------
                                                  1920 *  dlfloat -> short float (with cross check: short float -> dlfloat)
                                                  1921 *
                                                  1922
                                                  1923 * +0, -0     simple instruction and 'test' test
                                                  1924          VRR_A VCLFNH,2,0,00,00,N
00002548                                          1925+         DS    0FD
00002548                        00002548          1926+         USING *,R5              base for test data and test routine
00002548  000025D8                                1927+T24      DC    A(X24)            address of test routine
0000254C  0018                                    1928+         DC    H'24'             test number
0000254E  00                                      1929+         DC    X'00'
0000254F  D5                                      1930+         DC    CL1'N'            Y = skip cross check
00002550  02                                      1931+         DC    HL1'2'            m3
00002551  00                                      1932+         DC    HL1'0'            m4
00002552  00                                      1933+FLG24    DC    X'00'             expected FPC flags
00002553  00                                      1934+VXC24    DC    X'00'             expected VXC
00002554  0000260C                                1935+V2_24    DC    A(RE24+16)        address of v2: 16-byte packed decimal
00002558  E5C3D3C6 D5C84040                       1936+         DC    CL8'VCLFNH'       instruction name
00002560  00000010                                1937+         DC    A(16)             result length
00002564  000025FC                                1938+         DC    A(RE24)           address of expected resul
00002568  00000000 00000000                       1939+         DS    FD                gap
00002570  00000000 00000000                       1940+V1O24    DS    XL16              V1 output
00002578  00000000 00000000
00002580  00000000 00000000                       1941+         DS    FD                   gap
00002588  00000000                                1942+FPC_R_24 DS    F                 FPC after instruction
00002590  00000000 00000000                       1943+         DS    FD                   gap
00002598  40404040 40404040                       1944+         DC    CL8' '            was cross check skipped?
000025A0  00000000 00000000                       1945+         DS    FD                   gap
000025A8  00000000 00000000                       1946+XCO24    DS    XL16              Cross check Output
000025B0  00000000 00000000
000025B8  00000000 00000000                       1947+         DS    FD                   gap
000025C0  00000000                                1948+FPC_XC_24 DS   F                 FPC after cross check
000025C8  00000000 00000000                       1949+         DS    FD                   gap
000025D0  00000000                                1950+         DS    F                 debug area
000025D4  00000000                                1951+         DS    F
                                                  1952+*
000025D8                                          1953+X24      DS    0F
000025D8  B29D 85A4                     000007A4  1954+         LFPC  FPCINIT           initialize FPC
                                                  1955+*         LFPC  =XL4'08000000'         set trap exception
000025DC  E320 500C 0014                00002554  1956+         LGF   R2,V2_24          get v2
000025E2  E762 0000 0806                00000000  1957+         VL    V22,0(R2)
000025E8  E666 0000 2C56                          1958+         VCLFNH V22,V22,2,0      test instruction (dest is source)
000025EE  B29C 5040                     00002588  1959+         STFPC FPC_R_24          save FPC
000025F2  E760 5028 080E                00002570  1960+         VST   V22,V1O24         save instruction result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000025F8  07FB                                     1961+         BR    R11                 return
000025FC                                           1962+RE24     DS    0F                  expected 16 byte result
000025FC                                           1963+         DROP  R5
000025FC  00000000 80000000                        1964          DC    XL16'00000000800000000000000000000000'
00002604  00000000 00000000
0000260C  00008000 00000000                        1965          DC    XL16'00008000000000000000000000000000'
00002614  00000000 00000000
                                                   1966
                                                   1967 * +1, -1
                                                   1968          VRR_A VCLFNH,2,0,00,00,N
00002620                                           1969+         DS    0FD
00002620                      00002620             1970+         USING *,R5                base for test data and test routine
00002620  000026B0                                 1971+T25      DC    A(X25)              address of test routine
00002624  0019                                     1972+         DC    H'25'               test number
00002626  00                                       1973+         DC    X'00'
00002627  D5                                       1974+         DC    CL1'N'              Y = skip cross check
00002628  02                                       1975+         DC    HL1'2'              m3
00002629  00                                       1976+         DC    HL1'0'              m4
0000262A  00                                       1977+FLG25    DC    X'00'               expected FPC flags
0000262B  00                                       1978+VXC25    DC    X'00'               expected VXC
0000262C  000026E4                                 1979+V2_25    DC    A(RE25+16)          address of v2: 16-byte packed decimal
00002630  E5C3D3C6 D5C84040                        1980+         DC    CL8'VCLFNH'         instruction name
00002638  00000010                                 1981+         DC    A(16)               result length
0000263C  000026D4                                 1982+         DC    A(RE25)             address of expected resul
00002640  00000000 00000000                        1983+         DS    FD                  gap
00002648  00000000 00000000                        1984+V1O25    DS    XL16                V1 output
00002650  00000000 00000000
00002658  00000000 00000000                        1985+         DS    FD                     gap
00002660  00000000                                 1986+FPC_R_25 DS    F                   FPC after instruction
00002668  00000000 00000000                        1987+         DS    FD                     gap
00002670  40404040 40404040                        1988+         DC    CL8' '              was cross check skipped?
00002678  00000000 00000000                        1989+         DS    FD                     gap
00002680  00000000 00000000                        1990+XCO25    DS    XL16                Cross check Output
00002688  00000000 00000000
00002690  00000000 00000000                        1991+         DS    FD                     gap
00002698  00000000                                 1992+FPC_XC_25 DS   F                   FPC after cross check
000026A0  00000000 00000000                        1993+         DS    FD                     gap
000026A8  00000000                                 1994+         DS    F                   debug area
000026AC  00000000                                 1995+         DS    F
                                                   1996+*
000026B0                                           1997+X25      DS    0F
000026B0  B29D 85A4                    000007A4    1998+         LFPC  FPCINIT             initialize FPC
                                                   1999+*         LFPC  =XL4'08000000'          set trap exception
000026B4  E320 500C 0014               0000262C    2000+         LGF   R2,V2_25            get v2
000026BA  E762 0000 0806               00000000    2001+         VL    V22,0(R2)
000026C0  E666 0000 2C56                           2002+         VCLFNH V22,V22,2,0        test instruction (dest is source)
000026C6  B29C 5040                    00002660    2003+         STFPC FPC_R_25            save FPC
000026CA  E760 5028 080E               00002648    2004+         VST   V22,V1O25           save instruction result
000026D0  07FB                                     2005+         BR    R11                 return
000026D4                                           2006+RE25     DS    0F                  expected 16 byte result
000026D4                                           2007+         DROP  R5
000026D4  3F800000 BF800000                        2008          DC    XL16'3F800000BF800000000000000000000'
000026DC  00000000 00000000
000026E4  3E00BE00 00000000                        2009          DC    XL16'3E00BE000000000000000000000000'
000026EC  00000000 00000000
                                                   2010
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2011 * +0.5, -0.5
                                                   2012          VRR_A VCLFNH,2,0,00,00,N
000026F8                                           2013+         DS    0FD
000026F8                     000026F8              2014+         USING *,R5              base for test data and test routine
000026F8  00002788                                 2015+T26      DC    A(X26)            address of test routine
000026FC  001A                                     2016+         DC    H'26'             test number
000026FE  00                                       2017+         DC    X'00'
000026FF  D5                                       2018+         DC    CL1'N'            Y = skip cross check
00002700  02                                       2019+         DC    HL1'2'            m3
00002701  00                                       2020+         DC    HL1'0'            m4
00002702  00                                       2021+FLG26    DC    X'00'             expected FPC flags
00002703  00                                       2022+VXC26    DC    X'00'             expected VXC
00002704  000027BC                                 2023+V2_26    DC    A(RE26+16)        address of v2: 16-byte packed decimal
00002708  E5C3D3C6 D5C84040                        2024+         DC    CL8'VCLFNH'       instruction name
00002710  00000010                                 2025+         DC    A(16)             result length
00002714  000027AC                                 2026+         DC    A(RE26)           address of expected resul
00002718  00000000 00000000                        2027+         DS    FD                gap
00002720  00000000 00000000                        2028+V1O26    DS    XL16              V1 output
00002728  00000000 00000000
00002730  00000000 00000000                        2029+         DS    FD                   gap
00002738  00000000                                 2030+FPC_R_26 DS    F                 FPC after instruction
00002740  00000000 00000000                        2031+         DS    FD                   gap
00002748  40404040 40404040                        2032+         DC    CL8' '            was cross check skipped?
00002750  00000000 00000000                        2033+         DS    FD                   gap
00002758  00000000 00000000                        2034+XCO26    DS    XL16              Cross check Output
00002760  00000000 00000000
00002768  00000000 00000000                        2035+         DS    FD                   gap
00002770  00000000                                 2036+FPC_XC_26 DS   F                 FPC after cross check
00002778  00000000 00000000                        2037+         DS    FD                   gap
00002780  00000000                                 2038+         DS    F                 debug area
00002784  00000000                                 2039+         DS    F
                                                   2040+*
00002788                                           2041+X26      DS    0F
00002788  B29D 85A4                     000007A4   2042+         LFPC  FPCINIT           initialize FPC
                                                   2043+*         LFPC  =XL4'08000000'          set trap exception
0000278C  E320 500C 0014                00002704   2044+         LGF   R2,V2_26          get v2
00002792  E762 0000 0806                00000000   2045+         VL    V22,0(R2)
00002798  E666 0000 2C56                           2046+         VCLFNH V22,V22,2,0      test instruction (dest is source)
0000279E  B29C 5040                     00002738   2047+         STFPC FPC_R_26          save FPC
000027A2  E760 5028 080E                00002720   2048+         VST   V22,V1O26         save instruction result
000027A8  07FB                                     2049+         BR    R11               return
000027AC                                           2050+RE26     DS    0F                expected 16 byte result
000027AC                                           2051+         DROP  R5
000027AC  3F000000 BF000000                        2052          DC    XL16'3F000000BF000000000000000000000000'
000027B4  00000000 00000000
000027BC  3C00BC00 00000000                        2053          DC    XL16'3C00BC000000000000000000000000'
000027C4  00000000 00000000
                                                   2054
                                                   2055 * 1/64, -1/64
                                                   2056          VRR_A VCLFNH,2,0,00,00,N
000027D0                                           2057+         DS    0FD
000027D0                     000027D0              2058+         USING *,R5              base for test data and test routine
000027D0  00002860                                 2059+T27      DC    A(X27)            address of test routine
000027D4  001B                                     2060+         DC    H'27'             test number
000027D6  00                                       2061+         DC    X'00'
000027D7  D5                                       2062+         DC    CL1'N'            Y = skip cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000027D8  02                                       2063+         DC    HL1'2'            m3
000027D9  00                                       2064+         DC    HL1'0'            m4
000027DA  00                                       2065+FLG27    DC    X'00'             expected FPC flags
000027DB  00                                       2066+VXC27    DC    X'00'             expected VXC
000027DC  00002894                                 2067+V2_27    DC    A(RE27+16)        address of v2: 16-byte packed decimal
000027E0  E5C3D3C6 D5C84040                        2068+         DC    CL8'VCLFNH'       instruction name
000027E8  00000010                                 2069+         DC    A(16)             result length
000027EC  00002884                                 2070+         DC    A(RE27)           address of expected resul
000027F0  00000000 00000000                        2071+         DS    FD                gap
000027F8  00000000 00000000                        2072+V1O27    DS    XL16              V1 output
00002800  00000000 00000000
00002808  00000000 00000000                        2073+         DS    FD                   gap
00002810  00000000                                 2074+FPC_R_27 DS    F                 FPC after instruction
00002818  00000000 00000000                        2075+         DS    FD                   gap
00002820  40404040 40404040                        2076+         DC    CL8' '            was cross check skipped?
00002828  00000000 00000000                        2077+         DS    FD                   gap
00002830  00000000 00000000                        2078+XCO27    DS    XL16              Cross check Output
00002838  00000000 00000000
00002840  00000000 00000000                        2079+         DS    FD                   gap
00002848  00000000                                 2080+FPC_XC_27 DS   F                 FPC after cross check
00002850  00000000 00000000                        2081+         DS    FD                   gap
00002858  00000000                                 2082+         DS    F                 debug area
0000285C  00000000                                 2083+         DS    F
                                                   2084+*
00002860                                           2085+X27      DS    0F
00002860  B29D 85A4                     000007A4   2086+         LFPC  FPCINIT           initialize FPC
                                                   2087+*         LFPC  =XL4'08000000'          set trap exception
00002864  E320 500C 0014                000027DC   2088+         LGF   R2,V2_27          get v2
0000286A  E762 0000 0806                00000000   2089+         VL    V22,0(R2)
00002870  E666 0000 2C56                           2090+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00002876  B29C 5040                     00002810   2091+         STFPC FPC_R_27          save FPC
0000287A  E760 5028 080E                000027F8   2092+         VST   V22,V1O27         save instruction result
00002880  07FB                                     2093+         BR    R11               return
00002884                                           2094+RE27     DS    0F                expected 16 byte result
00002884                                           2095+         DROP  R5
00002884  3C800000 BC800000                        2096          DC    XL16'3C800000BC80000000000000000000000'
0000288C  00000000 00000000
00002894  3200B200 00000000                        2097          DC    XL16'3200B200000000000000000000000000'
0000289C  00000000 00000000
                                                   2098
                                                   2099 * +15, -15
                                                   2100          VRR_A VCLFNH,2,0,00,00,N
000028A8                                           2101+         DS    0FD
000028A8                        000028A8           2102+         USING *,R5              base for test data and test routine
000028A8  00002938                                 2103+T28      DC    A(X28)            address of test routine
000028AC  001C                                     2104+         DC    H'28'             test number
000028AE  00                                       2105+         DC    X'00'
000028AF  D5                                       2106+         DC    CL1'N'            Y = skip cross check
000028B0  02                                       2107+         DC    HL1'2'            m3
000028B1  00                                       2108+         DC    HL1'0'            m4
000028B2  00                                       2109+FLG28    DC    X'00'             expected FPC flags
000028B3  00                                       2110+VXC28    DC    X'00'             expected VXC
000028B4  0000296C                                 2111+V2_28    DC    A(RE28+16)        address of v2: 16-byte packed decimal
000028B8  E5C3D3C6 D5C84040                        2112+         DC    CL8'VCLFNH'       instruction name
000028C0  00000010                                 2113+         DC    A(16)             result length
000028C4  0000295C                                 2114+         DC    A(RE28)           address of expected resul
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000028C8  00000000 00000000                        2115+          DS    FD                 gap
000028D0  00000000 00000000                        2116+V1O28     DS    XL16               V1 output
000028D8  00000000 00000000
000028E0  00000000 00000000                        2117+          DS    FD                    gap
000028E8  00000000                                 2118+FPC_R_28  DS    F                  FPC after instruction
000028F0  00000000 00000000                        2119+          DS    FD                    gap
000028F8  40404040 40404040                        2120+          DC    CL8' '             was cross check skipped?
00002900  00000000 00000000                        2121+          DS    FD                    gap
00002908  00000000 00000000                        2122+XCO28     DS    XL16               Cross check Output
00002910  00000000 00000000
00002918  00000000 00000000                        2123+          DS    FD                    gap
00002920  00000000                                 2124+FPC_XC_28 DS    F                  FPC after cross check
00002928  00000000 00000000                        2125+          DS    FD                    gap
00002930  00000000                                 2126+          DS    F                  debug area
00002934  00000000                                 2127+          DS    F
                                                   2128+*
00002938                                           2129+X28       DS    0F
00002938  B29D 85A4                     000007A4   2130+          LFPC  FPCINIT            initialize FPC
                                                   2131+*         LFPC  =XL4'08000000'          set trap exception
0000293C  E320 500C 0014                000028B4   2132+          LGF   R2,V2_28           get v2
00002942  E762 0000 0806                00000000   2133+          VL    V22,0(R2)
00002948  E666 0000 2C56                           2134+          VCLFNH V22,V22,2,0       test instruction (dest is source)
0000294E  B29C 5040                     000028E8   2135+          STFPC FPC_R_28           save FPC
00002952  E760 5028 080E                000028D0   2136+          VST   V22,V1O28          save instruction result
00002958  07FB                                     2137+          BR    R11                return
0000295C                                           2138+RE28      DS    0F                 expected 16 byte result
0000295C                                           2139+          DROP  R5
0000295C  41700000 C1700000                        2140           DC    XL16'41700000C17000000000000000000000'
00002964  00000000 00000000
0000296C  45C0C5C0 00000000                        2141           DC    XL16'45C0C5C00000000000000000000000000'
00002974  00000000 00000000
                                                   2142
                                                   2143 * +20/7, -20/7 (about)
                                                   2144           VRR_A VCLFNH,2,0,00,00,N
00002980                                           2145+          DS    0FD
00002980                        00002980           2146+          USING *,R5               base for test data and test routine
00002980  00002A10                                 2147+T29       DC    A(X29)             address of test routine
00002984  001D                                     2148+          DC    H'29'              test number
00002986  00                                       2149+          DC    X'00'
00002987  D5                                       2150+          DC    CL1'N'             Y = skip cross check
00002988  02                                       2151+          DC    HL1'2'             m3
00002989  00                                       2152+          DC    HL1'0'             m4
0000298A  00                                       2153+FLG29     DC    X'00'              expected FPC flags
0000298B  00                                       2154+VXC29     DC    X'00'              expected VXC
0000298C  00002A44                                 2155+V2_29     DC    A(RE29+16)         address of v2: 16-byte packed decimal
00002990  E5C3D3C6 D5C84040                        2156+          DC    CL8'VCLFNH'        instruction name
00002998  00000010                                 2157+          DC    A(16)              result length
0000299C  00002A34                                 2158+          DC    A(RE29)            address of expected resul
000029A0  00000000 00000000                        2159+          DS    FD                 gap
000029A8  00000000 00000000                        2160+V1O29     DS    XL16               V1 output
000029B0  00000000 00000000
000029B8  00000000 00000000                        2161+          DS    FD                    gap
000029C0  00000000                                 2162+FPC_R_29  DS    F                  FPC after instruction
000029C8  00000000 00000000                        2163+          DS    FD                    gap
000029D0  40404040 40404040                        2164+          DC    CL8' '             was cross check skipped?
000029D8  00000000 00000000                        2165+          DS    FD                    gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000029E0  00000000 00000000                       2166+XCO29    DS    XL16              Cross check Output
000029E8  00000000 00000000
000029F0  00000000 00000000                       2167+         DS    FD                   gap
000029F8  00000000                                2168+FPC_XC_29 DS   F                 FPC after cross check
00002A00  00000000 00000000                       2169+         DS    FD                   gap
00002A08  00000000                                2170+         DS    F                 debug area
00002A0C  00000000                                2171+         DS    F
                                                  2172+*
00002A10                                          2173+X29      DS    0F
00002A10  B29D 85A4                     000007A4  2174+         LFPC  FPCINIT           initialize FPC
                                                  2175+*         LFPC  =XL4'08000000'         set trap exception
00002A14  E320 500C 0014                0000298C  2176+         LGF   R2,V2_29          get v2
00002A1A  E762 0000 0806                00000000  2177+         VL    V22,0(R2)
00002A20  E666 0000 2C56                          2178+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00002A26  B29C 5040                     000029C0  2179+         STFPC FPC_R_29          save FPC
00002A2A  E760 5028 080E                000029A8  2180+         VST   V22,V1O29         save instruction result
00002A30  07FB                                    2181+         BR    R11               return
00002A34                                          2182+RE29     DS    0F                expected 16 byte result
00002A34                                          2183+         DROP  R5
00002A34  4036C000 C036C000                       2184          DC    XL16'4036C000C036C000000000000000000'
00002A3C  00000000 00000000
00002A44  40DBC0DB 00000000                       2185          DC    XL16'40DBC0DB000000000000000000000000'
00002A4C  00000000 00000000
                                                  2186
                                                  2187 * additional tests
                                                  2188 * max  tiny:  (1 - 2^-11) * 2^16 (65504)
                                                  2189          VRR_A VCLFNH,2,0,00,00,N
00002A58                                          2190+         DS    0FD
00002A58                        00002A58          2191+         USING *,R5              base for test data and test routine
00002A58  00002AE8                                2192+T30      DC    A(X30)            address of test routine
00002A5C  001E                                    2193+         DC    H'30'             test number
00002A5E  00                                      2194+         DC    X'00'
00002A5F  D5                                      2195+         DC    CL1'N'            Y = skip cross check
00002A60  02                                      2196+         DC    HL1'2'            m3
00002A61  00                                      2197+         DC    HL1'0'            m4
00002A62  00                                      2198+FLG30    DC    X'00'             expected FPC flags
00002A63  00                                      2199+VXC30    DC    X'00'             expected VXC
00002A64  00002B1C                                2200+V2_30    DC    A(RE30+16)        address of v2: 16-byte packed decimal
00002A68  E5C3D3C6 D5C84040                       2201+         DC    CL8'VCLFNH'       instruction name
00002A70  00000010                                2202+         DC    A(16)             result length
00002A74  00002B0C                                2203+         DC    A(RE30)           address of expected resul
00002A78  00000000 00000000                       2204+         DS    FD                gap
00002A80  00000000 00000000                       2205+V1O30    DS    XL16              V1 output
00002A88  00000000 00000000
00002A90  00000000 00000000                       2206+         DS    FD                   gap
00002A98  00000000                                2207+FPC_R_30 DS    F                 FPC after instruction
00002AA0  00000000 00000000                       2208+         DS    FD                   gap
00002AA8  40404040 40404040                       2209+         DC    CL8' '            was cross check skipped?
00002AB0  00000000 00000000                       2210+         DS    FD                   gap
00002AB8  00000000 00000000                       2211+XCO30    DS    XL16              Cross check Output
00002AC0  00000000 00000000
00002AC8  00000000 00000000                       2212+         DS    FD                   gap
00002AD0  00000000                                2213+FPC_XC_30 DS   F                 FPC after cross check
00002AD8  00000000 00000000                       2214+         DS    FD                   gap
00002AE0  00000000                                2215+         DS    F                 debug area
00002AE4  00000000                                2216+         DS    F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  2217+*
00002AE8                                          2218+X30      DS    0F
00002AE8  B29D 85A4                     000007A4  2219+         LFPC  FPCINIT           initialize FPC
                                                  2220+*         LFPC  =XL4'08000000'         set trap exception
00002AEC  E320 500C 0014                00002A64  2221+         LGF   R2,V2_30          get v2
00002AF2  E762 0000 0806                00000000  2222+         VL    V22,0(R2)
00002AF8  E666 0000 2C56                          2223+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00002AFE  B29C 5040                     00002A98  2224+         STFPC FPC_R_30          save FPC
00002B02  E760 5028 080E                00002A80  2225+         VST   V22,V1O30         save instruction result
00002B08  07FB                                    2226+         BR    R11               return
00002B0C                                          2227+RE30     DS    0F                expected 16 byte result
00002B0C                                          2228+         DROP  R5
00002B0C  47800000 00000000                       2229          DC    XL16'47800000000000000000000000000000'
00002B14  00000000 00000000
00002B1C  5E000000 00000000                       2230          DC    XL16'5E00000000000000000000000000000'
00002B24  00000000 00000000
                                                  2231
                                                  2232 * max  dlfloat:  2^(33)-2ulp
                                                  2233          VRR_A VCLFNH,2,0,00,00,N
00002B30                                          2234+         DS    0FD
00002B30                        00002B30          2235+         USING *,R5              base for test data and test routine
00002B30  00002BC0                                2236+T31      DC    A(X31)            address of test routine
00002B34  001F                                    2237+         DC    H'31'             test number
00002B36  00                                      2238+         DC    X'00'
00002B37  D5                                      2239+         DC    CL1'N'            Y = skip cross check
00002B38  02                                      2240+         DC    HL1'2'            m3
00002B39  00                                      2241+         DC    HL1'0'            m4
00002B3A  00                                      2242+FLG31    DC    X'00'             expected FPC flags
00002B3B  00                                      2243+VXC31    DC    X'00'             expected VXC
00002B3C  00002BF4                                2244+V2_31    DC    A(RE31+16)        address of v2: 16-byte packed decimal
00002B40  E5C3D3C6 D5C84040                       2245+         DC    CL8'VCLFNH'       instruction name
00002B48  00000010                                2246+         DC    A(16)             result length
00002B4C  00002BE4                                2247+         DC    A(RE31)           address of expected resul
00002B50  00000000 00000000                       2248+         DS    FD                gap
00002B58  00000000 00000000                       2249+V1O31    DS    XL16              V1 output
00002B60  00000000 00000000
00002B68  00000000 00000000                       2250+         DS    FD                   gap
00002B70  00000000                                2251+FPC_R_31 DS    F                 FPC after instruction
00002B78  00000000 00000000                       2252+         DS    FD                   gap
00002B80  40404040 40404040                       2253+         DC    CL8' '            was cross check skipped?
00002B88  00000000 00000000                       2254+         DS    FD                   gap
00002B90  00000000 00000000                       2255+XCO31    DS    XL16              Cross check Output
00002B98  00000000 00000000
00002BA0  00000000 00000000                       2256+         DS    FD                   gap
00002BA8  00000000                                2257+FPC_XC_31 DS   F                 FPC after cross check
00002BB0  00000000 00000000                       2258+         DS    FD                   gap
00002BB8  00000000                                2259+         DS    F                 debug area
00002BBC  00000000                                2260+         DS    F
                                                  2261+*
00002BC0                                          2262+X31      DS    0F
00002BC0  B29D 85A4                     000007A4  2263+         LFPC  FPCINIT           initialize FPC
                                                  2264+*         LFPC  =XL4'08000000'         set trap exception
00002BC4  E320 500C 0014                00002B3C  2265+         LGF   R2,V2_31          get v2
00002BCA  E762 0000 0806                00000000  2266+         VL    V22,0(R2)
00002BD0  E666 0000 2C56                          2267+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00002BD6  B29C 5040                     00002B70  2268+         STFPC FPC_R_31          save FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002BDA  E760 5028 080E                00002B58  2269+          VST   V22,V1O31         save instruction result
00002BE0  07FB                                    2270+          BR    R11               return
00002BE4                                          2271+RE31      DS    0F                expected 16 byte result
00002BE4                                          2272+          DROP  R5
00002BE4  4FFF8000 00000000                       2273           DC    XL16'4FFF8000000000000000000000000000'
00002BEC  00000000 00000000
00002BF4  7FFE0000 00000000                       2274           DC    XL16'7FFE0000000000000000000000000000'
00002BFC  00000000 00000000
                                                  2275
                                                  2276 * min  dlfloat: 2^(-31)*+ulp
                                                  2277           VRR_A VCLFNH,2,0,00,00,N
00002C08                                          2278+          DS    0FD
00002C08                      00002C08            2279+          USING *,R5              base for test data and test routine
00002C08  00002C98                                2280+T32       DC    A(X32)            address of test routine
00002C0C  0020                                    2281+          DC    H'32'             test number
00002C0E  00                                      2282+          DC    X'00'
00002C0F  D5                                      2283+          DC    CL1'N'            Y = skip cross check
00002C10  02                                      2284+          DC    HL1'2'            m3
00002C11  00                                      2285+          DC    HL1'0'            m4
00002C12  00                                      2286+FLG32     DC    X'00'             expected FPC flags
00002C13  00                                      2287+VXC32     DC    X'00'             expected VXC
00002C14  00002CCC                                2288+V2_32     DC    A(RE32+16)        address of v2: 16-byte packed decimal
00002C18  E5C3D3C6 D5C84040                       2289+          DC    CL8'VCLFNH'       instruction name
00002C20  00000010                                2290+          DC    A(16)             result length
00002C24  00002CBC                                2291+          DC    A(RE32)           address of expected resul
00002C28  00000000 00000000                       2292+          DS    FD                gap
00002C30  00000000 00000000                       2293+V1O32     DS    XL16              V1 output
00002C38  00000000 00000000
00002C40  00000000 00000000                       2294+          DS    FD                   gap
00002C48  00000000                                2295+FPC_R_32 DS     F                 FPC after instruction
00002C50  00000000 00000000                       2296+          DS    FD                   gap
00002C58  40404040 40404040                       2297+          DC    CL8' '            was cross check skipped?
00002C60  00000000 00000000                       2298+          DS    FD                   gap
00002C68  00000000 00000000                       2299+XCO32     DS    XL16              Cross check Output
00002C70  00000000 00000000
00002C78  00000000 00000000                       2300+          DS    FD                   gap
00002C80  00000000                                2301+FPC_XC_32 DS    F                 FPC after cross check
00002C88  00000000 00000000                       2302+          DS    FD                   gap
00002C90  00000000                                2303+          DS    F                 debug area
00002C94  00000000                                2304+          DS    F
                                                  2305+*
00002C98                                          2306+X32       DS    0F
00002C98  B29D 85A4                     000007A4  2307+          LFPC  FPCINIT           initialize FPC
                                                  2308+*          LFPC  =XL4'08000000'          set trap exception
00002C9C  E320 500C 0014                00002C14  2309+          LGF   R2,V2_32          get v2
00002CA2  E762 0000 0806                00000000  2310+          VL    V22,0(R2)
00002CA8  E666 0000 2C56                          2311+          VCLFNH V22,V22,2,0      test instruction (dest is source)
00002CAE  B29C 5040                     00002C48  2312+          STFPC FPC_R_32          save FPC
00002CB2  E760 5028 080E                00002C30  2313+          VST   V22,V1O32         save instruction result
00002CB8  07FB                                    2314+          BR    R11               return
00002CBC                                          2315+RE32      DS    0F                expected 16 byte result
00002CBC                                          2316+          DROP  R5
00002CBC  30004000 00000000                       2317           DC    XL16'30004000000000000000000000000000'
00002CC4  00000000 00000000
00002CCC  00010000 00000000                       2318           DC    XL16'00010000000000000000000000000000'
00002CD4  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2319
                                                   2320 * +Infinity, -Infinity
                                                   2321          VRR_A VCLFNH,2,0,80,21,S                skip xcheck - infinity
00002CE0                                           2322+         DS    0FD
00002CE0                       00002CE0            2323+         USING *,R5              base for test data and test routine
00002CE0  00002D70                                 2324+T33      DC    A(X33)            address of test routine
00002CE4  0021                                     2325+         DC    H'33'             test number
00002CE6  00                                       2326+         DC    X'00'
00002CE7  E2                                       2327+         DC    CL1'S'            Y = skip cross check
00002CE8  02                                       2328+         DC    HL1'2'            m3
00002CE9  00                                       2329+         DC    HL1'0'            m4
00002CEA  80                                       2330+FLG33    DC    X'80'             expected FPC flags
00002CEB  21                                       2331+VXC33    DC    X'21'             expected VXC
00002CEC  00002DA4                                 2332+V2_33    DC    A(RE33+16)        address of v2: 16-byte packed decimal
00002CF0  E5C3D3C6 D5C84040                        2333+         DC    CL8'VCLFNH'       instruction name
00002CF8  00000010                                 2334+         DC    A(16)             result length
00002CFC  00002D94                                 2335+         DC    A(RE33)           address of expected resul
00002D00  00000000 00000000                        2336+         DS    FD                gap
00002D08  00000000 00000000                        2337+V1O33    DS    XL16              V1 output
00002D10  00000000 00000000
00002D18  00000000 00000000                        2338+         DS    FD                   gap
00002D20  00000000                                 2339+FPC_R_33 DS    F                 FPC after instruction
00002D28  00000000 00000000                        2340+         DS    FD                   gap
00002D30  40404040 40404040                        2341+         DC    CL8' '            was cross check skipped?
00002D38  00000000 00000000                        2342+         DS    FD                   gap
00002D40  00000000 00000000                        2343+XCO33    DS    XL16              Cross check Output
00002D48  00000000 00000000
00002D50  00000000 00000000                        2344+         DS    FD                   gap
00002D58  00000000                                 2345+FPC_XC_33 DS   F                 FPC after cross check
00002D60  00000000 00000000                        2346+         DS    FD                   gap
00002D68  00000000                                 2347+         DS    F                 debug area
00002D6C  00000000                                 2348+         DS    F
                                                   2349+*
00002D70                                           2350+X33      DS    0F
00002D70  B29D 85A4                    000007A4    2351+         LFPC  FPCINIT           initialize FPC
                                                   2352+*         LFPC  =XL4'08000000'         set trap exception
00002D74  E320 500C 0014               00002CEC    2353+         LGF   R2,V2_33          get v2
00002D7A  E762 0000 0806               00000000    2354+         VL    V22,0(R2)
00002D80  E666 0000 2C56                           2355+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00002D86  B29C 5040                    00002D20    2356+         STFPC FPC_R_33          save FPC
00002D8A  E760 5028 080E               00002D08    2357+         VST   V22,V1O33         save instruction result
00002D90  07FB                                     2358+         BR    R11               return
00002D94                                           2359+RE33     DS    0F                expected 16 byte result
00002D94                                           2360+         DROP  R5
00002D94  7FC00000 00000000                        2361          DC    XL16'7FC0000000000000FFC0000000000000'
00002D9C  FFC00000 00000000
00002DA4  7FFF0000 FFFF0000                        2362          DC    XL16'7FFF0000FFFF0000000000000000000000'
00002DAC  00000000 00000000
                                                   2363
                                                   2364 * inexact - bad m3
                                                   2365          VRR_A VCLFNH,5,0,08,05,S                skip xc - inexact
00002DB8                                           2366+         DS    0FD
00002DB8                       00002DB8            2367+         USING *,R5              base for test data and test routine
00002DB8  00002E48                                 2368+T34      DC    A(X34)            address of test routine
00002DBC  0022                                     2369+         DC    H'34'             test number
00002DBE  00                                       2370+         DC    X'00'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002DBF  E2                                      2371+          DC    CL1'S'             Y = skip cross check
00002DC0  05                                      2372+          DC    HL1'5'             m3
00002DC1  00                                      2373+          DC    HL1'0'             m4
00002DC2  08                                      2374+FLG34     DC    X'08'              expected FPC flags
00002DC3  05                                      2375+VXC34     DC    X'05'              expected VXC
00002DC4  00002E7C                                2376+V2_34     DC    A(RE34+16)         address of v2: 16-byte packed decimal
00002DC8  E5C3D3C6 D5C84040                       2377+          DC    CL8'VCLFNH'        instruction name
00002DD0  00000010                                2378+          DC    A(16)              result length
00002DD4  00002E6C                                2379+          DC    A(RE34)            address of expected resul
00002DD8  00000000 00000000                       2380+          DS    FD                 gap
00002DE0  00000000 00000000                       2381+V1O34     DS    XL16               V1 output
00002DE8  00000000 00000000
00002DF0  00000000 00000000                       2382+          DS    FD                    gap
00002DF8  00000000                                2383+FPC_R_34  DS    F                  FPC after instruction
00002E00  00000000 00000000                       2384+          DS    FD                    gap
00002E08  40404040 40404040                       2385+          DC    CL8' '             was cross check skipped?
00002E10  00000000 00000000                       2386+          DS    FD                    gap
00002E18  00000000 00000000                       2387+XCO34     DS    XL16               Cross check Output
00002E20  00000000 00000000
00002E28  00000000 00000000                       2388+          DS    FD                    gap
00002E30  00000000                                2389+FPC_XC_34 DS    F                  FPC after cross check
00002E38  00000000 00000000                       2390+          DS    FD                    gap
00002E40  00000000                                2391+          DS    F                  debug area
00002E44  00000000                                2392+          DS    F
                                                  2393+*
00002E48                                          2394+X34       DS    0F
00002E48  B29D 85A4                     000007A4  2395+          LFPC  FPCINIT            initialize FPC
                                                  2396+*          LFPC  =XL4'08000000'          set trap exception
00002E4C  E320 500C 0014                00002DC4  2397+          LGF   R2,V2_34           get v2
00002E52  E762 0000 0806                00000000  2398+          VL    V22,0(R2)
00002E58  E666 0000 5C56                          2399+          VCLFNH V22,V22,5,0       test instruction (dest is source)
00002E5E  B29C 5040                     00002DF8  2400+          STFPC FPC_R_34           save FPC
00002E62  E760 5028 080E                00002DE0  2401+          VST   V22,V1O34          save instruction result
00002E68  07FB                                    2402+          BR    R11                return
00002E6C                                          2403+RE34      DS    0F                 expected 16 byte result
00002E6C                                          2404+          DROP  R5
00002E6C  00000000 00000000                       2405           DC    XL16'00000000000000000000000000000000'
00002E74  00000000 00000000
00002E7C  00010000 00000000                       2406           DC    XL16'00010000000000000000000000000F000'
00002E84  00000000 0000F000
                                                  2407
                                                  2408 * inexact - bad m4
                                                  2409           VRR_A VCLFNH,2,5,08,05,S                    skip xc - inexact
00002E90                                          2410+          DS    0FD
00002E90                        00002E90          2411+          USING *,R5               base for test data and test routine
00002E90  00002F20                                2412+T35       DC    A(X35)             address of test routine
00002E94  0023                                    2413+          DC    H'35'              test number
00002E96  00                                      2414+          DC    X'00'
00002E97  E2                                      2415+          DC    CL1'S'             Y = skip cross check
00002E98  02                                      2416+          DC    HL1'2'             m3
00002E99  05                                      2417+          DC    HL1'5'             m4
00002E9A  08                                      2418+FLG35     DC    X'08'              expected FPC flags
00002E9B  05                                      2419+VXC35     DC    X'05'              expected VXC
00002E9C  00002F54                                2420+V2_35     DC    A(RE35+16)         address of v2: 16-byte packed decimal
00002EA0  E5C3D3C6 D5C84040                       2421+          DC    CL8'VCLFNH'        instruction name
00002EA8  00000010                                2422+          DC    A(16)              result length
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002EAC  00002F44                                 2423+          DC    A(RE35)            address of expected resul
00002EB0  00000000 00000000                        2424+          DS    FD                 gap
00002EB8  00000000 00000000                        2425+V1O35     DS    XL16               V1 output
00002EC0  00000000 00000000
00002EC8  00000000 00000000                        2426+          DS    FD                    gap
00002ED0  00000000                                 2427+FPC_R_35  DS    F                  FPC after instruction
00002ED8  00000000 00000000                        2428+          DS    FD                    gap
00002EE0  40404040 40404040                        2429+          DC    CL8' '             was cross check skipped?
00002EE8  00000000 00000000                        2430+          DS    FD                    gap
00002EF0  00000000 00000000                        2431+XCO35     DS    XL16               Cross check Output
00002EF8  00000000 00000000
00002F00  00000000 00000000                        2432+          DS    FD                    gap
00002F08  00000000                                 2433+FPC_XC_35 DS    F                  FPC after cross check
00002F10  00000000 00000000                        2434+          DS    FD                    gap
00002F18  00000000                                 2435+          DS    F                  debug area
00002F1C  00000000                                 2436+          DS    F
                                                   2437+*
00002F20                                           2438+X35       DS    0F
00002F20  B29D 85A4                    000007A4    2439+          LFPC  FPCINIT            initialize FPC
                                                   2440+*          LFPC  =XL4'08000000'          set trap exception
00002F24  E320 500C 0014               00002E9C    2441+          LGF   R2,V2_35           get v2
00002F2A  E762 0000 0806               00000000    2442+          VL    V22,0(R2)
00002F30  E666 0005 2C56                           2443+          VCLFNH V22,V22,2,5       test instruction (dest is source)
00002F36  B29C 5040                    00002ED0    2444+          STFPC FPC_R_35           save FPC
00002F3A  E760 5028 080E               00002EB8    2445+          VST   V22,V1O35          save instruction result
00002F40  07FB                                     2446+          BR    R11                return
00002F44                                           2447+RE35      DS    0F                 expected 16 byte result
00002F44                                           2448+          DROP  R5
00002F44  00000000 00000000                        2449           DC    XL16'00000000000000000000000000000000'
00002F4C  00000000 00000000
00002F54  00010000 00000000                        2450           DC    XL16'00010000000000000000000000000F000'
00002F5C  00000000 0000F000
                                                   2451
                                                   2452 * more tests
                                                   2453 * +3.140625, -3.140625
                                                   2454           VRR_A VCLFNH,2,0,00,00,N
00002F68                                           2455+          DS    0FD
00002F68                       00002F68            2456+          USING *,R5               base for test data and test routine
00002F68  00002FF8                                 2457+T36       DC    A(X36)             address of test routine
00002F6C  0024                                     2458+          DC    H'36'              test number
00002F6E  00                                       2459+          DC    X'00'
00002F6F  D5                                       2460+          DC    CL1'N'             Y = skip cross check
00002F70  02                                       2461+          DC    HL1'2'             m3
00002F71  00                                       2462+          DC    HL1'0'             m4
00002F72  00                                       2463+FLG36     DC    X'00'              expected FPC flags
00002F73  00                                       2464+VXC36     DC    X'00'              expected VXC
00002F74  0000302C                                 2465+V2_36     DC    A(RE36+16)         address of v2: 16-byte packed decimal
00002F78  E5C3D3C6 D5C84040                        2466+          DC    CL8'VCLFNH'        instruction name
00002F80  00000010                                 2467+          DC    A(16)              result length
00002F84  0000301C                                 2468+          DC    A(RE36)            address of expected resul
00002F88  00000000 00000000                        2469+          DS    FD                 gap
00002F90  00000000 00000000                        2470+V1O36     DS    XL16               V1 output
00002F98  00000000 00000000
00002FA0  00000000 00000000                        2471+          DS    FD                    gap
00002FA8  00000000                                 2472+FPC_R_36  DS    F                  FPC after instruction
00002FB0  00000000 00000000                        2473+          DS    FD                    gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002FB8  40404040 40404040                       2474+          DC    CL8' '            was cross check skipped?
00002FC0  00000000 00000000                       2475+          DS    FD                   gap
00002FC8  00000000 00000000                       2476+XCO36     DS    XL16              Cross check Output
00002FD0  00000000 00000000
00002FD8  00000000 00000000                       2477+          DS    FD                   gap
00002FE0  00000000                                2478+FPC_XC_36 DS    F                 FPC after cross check
00002FE8  00000000 00000000                       2479+          DS    FD                   gap
00002FF0  00000000                                2480+          DS    F                 debug area
00002FF4  00000000                                2481+          DS    F
                                                  2482+*
00002FF8                                          2483+X36       DS    0F
00002FF8  B29D 85A4                    000007A4   2484+          LFPC  FPCINIT           initialize FPC
                                                  2485+*          LFPC  =XL4'08000000'         set trap exception
00002FFC  E320 500C 0014               00002F74   2486+          LGF   R2,V2_36          get v2
00003002  E762 0000 0806               00000000   2487+          VL    V22,0(R2)
00003008  E666 0000 2C56                          2488+          VCLFNH V22,V22,2,0      test instruction (dest is source)
0000300E  B29C 5040                    00002FA8   2489+          STFPC FPC_R_36          save FPC
00003012  E760 5028 080E               00002F90   2490+          VST   V22,V1O36         save instruction result
00003018  07FB                                    2491+          BR    R11               return
0000301C                                          2492+RE36      DS    0F                expected 16 byte result
0000301C                                          2493+          DROP  R5
0000301C  40890000 00000000                       2494           DC    XL16'40890000000000000C089000000000000'
00003024  C0890000 00000000
0000302C  42240000 C2240000                       2495           DC    XL16'42240000C22400000000000000000000'
00003034  00000000 00000000
                                                  2496
                                                  2497
                                                  2498 * +27.15625, -27.15625
                                                  2499           VRR_A VCLFNH,2,0,00,00,N
00003040                                          2500+          DS    0FD
00003040                       00003040           2501+          USING *,R5              base for test data and test routine
00003040  000030D0                                2502+T37       DC    A(X37)            address of test routine
00003044  0025                                    2503+          DC    H'37'             test number
00003046  00                                      2504+          DC    X'00'
00003047  D5                                      2505+          DC    CL1'N'            Y = skip cross check
00003048  02                                      2506+          DC    HL1'2'            m3
00003049  00                                      2507+          DC    HL1'0'            m4
0000304A  00                                      2508+FLG37     DC    X'00'             expected FPC flags
0000304B  00                                      2509+VXC37     DC    X'00'             expected VXC
0000304C  00003104                                2510+V2_37     DC    A(RE37+16)        address of v2: 16-byte packed decimal
00003050  E5C3D3C6 D5C84040                       2511+          DC    CL8'VCLFNH'       instruction name
00003058  00000010                                2512+          DC    A(16)             result length
0000305C  000030F4                                2513+          DC    A(RE37)           address of expected resul
00003060  00000000 00000000                       2514+          DS    FD                gap
00003068  00000000 00000000                       2515+V1O37     DS    XL16              V1 output
00003070  00000000 00000000
00003078  00000000 00000000                       2516+          DS    FD                   gap
00003080  00000000                                2517+FPC_R_37  DS    F                 FPC after instruction
00003088  00000000 00000000                       2518+          DS    FD                   gap
00003090  40404040 40404040                       2519+          DC    CL8' '            was cross check skipped?
00003098  00000000 00000000                       2520+          DS    FD                   gap
000030A0  00000000 00000000                       2521+XCO37     DS    XL16              Cross check Output
000030A8  00000000 00000000
000030B0  00000000 00000000                       2522+          DS    FD                   gap
000030B8  00000000                                2523+FPC_XC_37 DS    F                 FPC after cross check
000030C0  00000000 00000000                       2524+          DS    FD                   gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000030C8  00000000                                2525+         DS    F                 debug area
000030CC  00000000                                2526+         DS    F
                                                  2527+*
000030D0                                          2528+X37      DS    0F
000030D0  B29D 85A4                     000007A4  2529+         LFPC  FPCINIT           initialize FPC
                                                  2530+*         LFPC  =XL4'08000000'         set trap exception
000030D4  E320 500C 0014                0000304C  2531+         LGF   R2,V2_37          get v2
000030DA  E762 0000 0806                00000000  2532+         VL    V22,0(R2)
000030E0  E666 0000 2C56                          2533+         VCLFNH V22,V22,2,0      test instruction (dest is source)
000030E6  B29C 5040                     00003080  2534+         STFPC FPC_R_37          save FPC
000030EA  E760 5028 080E                00003068  2535+         VST   V22,V1O37         save instruction result
000030F0  07FB                                    2536+         BR    R11               return
000030F4                                          2537+RE37     DS    0F                expected 16 byte result
000030F4                                          2538+         DROP  R5
000030F4  3BD94000 00000000                       2539          DC    XL16'3BD9400000000000BBD9400000000000'
000030FC  BBD94000 00000000
00003104  2F650000 AF650000                       2540          DC    XL16'2F650000AF650000000000000000000'
0000310C  00000000 00000000
                                                  2541
                                                  2542 * +65504, -65504
                                                  2543          VRR_A VCLFNH,2,0,00,00,N
00003118                                          2544+         DS    0FD
00003118                        00003118          2545+         USING *,R5              base for test data and test routine
00003118  000031A8                                2546+T38      DC    A(X38)            address of test routine
0000311C  0026                                    2547+         DC    H'38'             test number
0000311E  00                                      2548+         DC    X'00'
0000311F  D5                                      2549+         DC    CL1'N'            Y = skip cross check
00003120  02                                      2550+         DC    HL1'2'            m3
00003121  00                                      2551+         DC    HL1'0'            m4
00003122  00                                      2552+FLG38    DC    X'00'             expected FPC flags
00003123  00                                      2553+VXC38    DC    X'00'             expected VXC
00003124  000031DC                                2554+V2_38    DC    A(RE38+16)        address of v2: 16-byte packed decimal
00003128  E5C3D3C6 D5C84040                       2555+         DC    CL8'VCLFNH'       instruction name
00003130  00000010                                2556+         DC    A(16)             result length
00003134  000031CC                                2557+         DC    A(RE38)           address of expected resul
00003138  00000000 00000000                       2558+         DS    FD                gap
00003140  00000000 00000000                       2559+V1O38    DS    XL16              V1 output
00003148  00000000 00000000
00003150  00000000 00000000                       2560+         DS    FD                   gap
00003158  00000000                                2561+FPC_R_38 DS    F                 FPC after instruction
00003160  00000000 00000000                       2562+         DS    FD                   gap
00003168  40404040 40404040                       2563+         DC    CL8' '            was cross check skipped?
00003170  00000000 00000000                       2564+         DS    FD                   gap
00003178  00000000 00000000                       2565+XCO38    DS    XL16              Cross check Output
00003180  00000000 00000000
00003188  00000000 00000000                       2566+         DS    FD                   gap
00003190  00000000                                2567+FPC_XC_38 DS   F                 FPC after cross check
00003198  00000000 00000000                       2568+         DS    FD                   gap
000031A0  00000000                                2569+         DS    F                 debug area
000031A4  00000000                                2570+         DS    F
                                                  2571+*
000031A8                                          2572+X38      DS    0F
000031A8  B29D 85A4                     000007A4  2573+         LFPC  FPCINIT           initialize FPC
                                                  2574+*         LFPC  =XL4'08000000'         set trap exception
000031AC  E320 500C 0014                00003124  2575+         LGF   R2,V2_38          get v2
000031B2  E762 0000 0806                00000000  2576+         VL    V22,0(R2)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000031B8  E666 0000 2C56                          2577+         VCLFNH V22,V22,2,0      test instruction (dest is source)
000031BE  B29C 5040                     00003158  2578+         STFPC FPC_R_38          save FPC
000031C2  E760 5028 080E                00003140  2579+         VST   V22,V1O38         save instruction result
000031C8  07FB                                    2580+         BR    R11               return
000031CC                                          2581+RE38     DS    0F                expected 16 byte result
000031CC                                          2582+         DROP  R5
000031CC  47800000 00000000                       2583          DC    XL16'478000000000000C780000000000000'
000031D4  C7800000 00000000
000031DC  5E000000 DE000000                       2584          DC    XL16'5E000000DE000000000000000000000'
000031E4  00000000 00000000
                                                  2585
                                                  2586 * +Normal, -Normal (2.5)
                                                  2587          VRR_A VCLFNH,2,0,00,00,N
000031F0                                          2588+         DS    0FD
000031F0                        000031F0          2589+         USING *,R5              base for test data and test routine
000031F0  00003280                                2590+T39      DC    A(X39)            address of test routine
000031F4  0027                                    2591+         DC    H'39'             test number
000031F6  00                                      2592+         DC    X'00'
000031F7  D5                                      2593+         DC    CL1'N'            Y = skip cross check
000031F8  02                                      2594+         DC    HL1'2'            m3
000031F9  00                                      2595+         DC    HL1'0'            m4
000031FA  00                                      2596+FLG39    DC    X'00'             expected FPC flags
000031FB  00                                      2597+VXC39    DC    X'00'             expected VXC
000031FC  000032B4                                2598+V2_39    DC    A(RE39+16)        address of v2: 16-byte packed decimal
00003200  E5C3D3C6 D5C84040                       2599+         DC    CL8'VCLFNH'       instruction name
00003208  00000010                                2600+         DC    A(16)             result length
0000320C  000032A4                                2601+         DC    A(RE39)           address of expected resul
00003210  00000000 00000000                       2602+         DS    FD                gap
00003218  00000000 00000000                       2603+V1O39    DS    XL16              V1 output
00003220  00000000 00000000
00003228  00000000 00000000                       2604+         DS    FD                   gap
00003230  00000000                                2605+FPC_R_39 DS    F                 FPC after instruction
00003238  00000000 00000000                       2606+         DS    FD                   gap
00003240  40404040 40404040                       2607+         DC    CL8' '            was cross check skipped?
00003248  00000000 00000000                       2608+         DS    FD                   gap
00003250  00000000 00000000                       2609+XCO39    DS    XL16              Cross check Output
00003258  00000000 00000000
00003260  00000000 00000000                       2610+         DS    FD                   gap
00003268  00000000                                2611+FPC_XC_39 DS   F                 FPC after cross check
00003270  00000000 00000000                       2612+         DS    FD                   gap
00003278  00000000                                2613+         DS    F                 debug area
0000327C  00000000                                2614+         DS    F
                                                  2615+*
00003280                                          2616+X39      DS    0F
00003280  B29D 85A4                     000007A4  2617+         LFPC  FPCINIT           initialize FPC
                                                  2618+*         LFPC  =XL4'08000000'          set trap exception
00003284  E320 500C 0014                000031FC  2619+         LGF   R2,V2_39          get v2
0000328A  E762 0000 0806                00000000  2620+         VL    V22,0(R2)
00003290  E666 0000 2C56                          2621+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00003296  B29C 5040                     00003230  2622+         STFPC FPC_R_39          save FPC
0000329A  E760 5028 080E                00003218  2623+         VST   V22,V1O39         save instruction result
000032A0  07FB                                    2624+         BR    R11               return
000032A4                                          2625+RE39     DS    0F                expected 16 byte result
000032A4                                          2626+         DROP  R5
000032A4  40200000 00000000                       2627          DC    XL16'402000000000000C020000000000000'
000032AC  C0200000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000032B4  40800000 C0800000                        2628          DC    XL16'40800000C08000000000000000000000'
000032BC  00000000 00000000
                                                   2629
                                                   2630 * +0.00006097, -0.00006097 (about)
                                                   2631          VRR_A VCLFNH,2,0,00,00,N
000032C8                                           2632+         DS    0FD
000032C8                       000032C8            2633+         USING *,R5              base for test data and test routine
000032C8  00003358                                 2634+T40      DC    A(X40)            address of test routine
000032CC  0028                                     2635+         DC    H'40'             test number
000032CE  00                                       2636+         DC    X'00'
000032CF  D5                                       2637+         DC    CL1'N'            Y = skip cross check
000032D0  02                                       2638+         DC    HL1'2'            m3
000032D1  00                                       2639+         DC    HL1'0'            m4
000032D2  00                                       2640+FLG40    DC    X'00'             expected FPC flags
000032D3  00                                       2641+VXC40    DC    X'00'             expected VXC
000032D4  0000338C                                 2642+V2_40    DC    A(RE40+16)        address of v2: 16-byte packed decimal
000032D8  E5C3D3C6 D5C84040                        2643+         DC    CL8'VCLFNH'       instruction name
000032E0  00000010                                 2644+         DC    A(16)             result length
000032E4  0000337C                                 2645+         DC    A(RE40)           address of expected resul
000032E8  00000000 00000000                        2646+         DS    FD                gap
000032F0  00000000 00000000                        2647+V1O40    DS    XL16              V1 output
000032F8  00000000 00000000
00003300  00000000 00000000                        2648+         DS    FD                   gap
00003308  00000000                                 2649+FPC_R_40 DS    F                 FPC after instruction
00003310  00000000 00000000                        2650+         DS    FD                   gap
00003318  40404040 40404040                        2651+         DC    CL8' '            was cross check skipped?
00003320  00000000 00000000                        2652+         DS    FD                   gap
00003328  00000000 00000000                        2653+XCO40    DS    XL16              Cross check Output
00003330  00000000 00000000
00003338  00000000 00000000                        2654+         DS    FD                   gap
00003340  00000000                                 2655+FPC_XC_40 DS   F                 FPC after cross check
00003348  00000000 00000000                        2656+         DS    FD                   gap
00003350  00000000                                 2657+         DS    F                 debug area
00003354  00000000                                 2658+         DS    F
                                                   2659+*
00003358                                           2660+X40      DS    0F
00003358  B29D 85A4                    000007A4    2661+         LFPC  FPCINIT           initialize FPC
                                                   2662+*         LFPC  =XL4'08000000'         set trap exception
0000335C  E320 500C 0014               000032D4    2663+         LGF   R2,V2_40          get v2
00003362  E762 0000 0806               00000000    2664+         VL    V22,0(R2)
00003368  E666 0000 2C56                           2665+         VCLFNH V22,V22,2,0      test instruction (dest is source)
0000336E  B29C 5040                    00003308    2666+         STFPC FPC_R_40          save FPC
00003372  E760 5028 080E               000032F0    2667+         VST   V22,V1O40         save instruction result
00003378  07FB                                     2668+         BR    R11               return
0000337C                                           2669+RE40     DS    0F                expected 16 byte result
0000337C                                           2670+         DROP  R5
0000337C  387FC000 00000000                        2671          DC    XL16'387FC00000000000B87FC00000000000'
00003384  B87FC000 00000000
0000338C  21FF0000 A1FF0000                        2672          DC    XL16'21FF0000A1FF00000000000000000000'
00003394  00000000 00000000
                                                   2673
                                                   2674 *-----------------------------------------------------------------
                                                   2675 *  VCFN     - VECTOR FP CONVERT FROM NNP
                                                   2676 *-----------------------------------------------------------------
                                                   2677 *  dlfloat -> tiny float (with cross check: tiny float -> dlfloat)
                                                   2678 *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2679
                                                   2680 * +0, -0     simple instruction and 'test' test
                                                   2681          VRR_A VCFN,1,0,00,00,N
000033A0                                           2682+         DS    0FD
000033A0                        000033A0           2683+         USING *,R5              base for test data and test routine
000033A0  00003430                                 2684+T41      DC    A(X41)            address of test routine
000033A4  0029                                     2685+         DC    H'41'             test number
000033A6  00                                       2686+         DC    X'00'
000033A7  D5                                       2687+         DC    CL1'N'            Y = skip cross check
000033A8  01                                       2688+         DC    HL1'1'            m3
000033A9  00                                       2689+         DC    HL1'0'            m4
000033AA  00                                       2690+FLG41    DC    X'00'             expected FPC flags
000033AB  00                                       2691+VXC41    DC    X'00'             expected VXC
000033AC  00003464                                 2692+V2_41    DC    A(RE41+16)        address of v2: 16-byte packed decimal
000033B0  E5C3C6D5 40404040                        2693+         DC    CL8'VCFN'         instruction name
000033B8  00000010                                 2694+         DC    A(16)             result length
000033BC  00003454                                 2695+         DC    A(RE41)           address of expected resul
000033C0  00000000 00000000                        2696+         DS    FD                gap
000033C8  00000000 00000000                        2697+V1O41    DS    XL16              V1 output
000033D0  00000000 00000000
000033D8  00000000 00000000                        2698+         DS    FD                   gap
000033E0  00000000                                 2699+FPC_R_41 DS    F                 FPC after instruction
000033E8  00000000 00000000                        2700+         DS    FD                   gap
000033F0  40404040 40404040                        2701+         DC    CL8' '            was cross check skipped?
000033F8  00000000 00000000                        2702+         DS    FD                   gap
00003400  00000000 00000000                        2703+XCO41    DS    XL16              Cross check Output
00003408  00000000 00000000
00003410  00000000 00000000                        2704+         DS    FD                   gap
00003418  00000000                                 2705+FPC_XC_41 DS   F                 FPC after cross check
00003420  00000000 00000000                        2706+         DS    FD                   gap
00003428  00000000                                 2707+         DS    F                 debug area
0000342C  00000000                                 2708+         DS    F
                                                   2709+*
00003430                                           2710+X41      DS    0F
00003430  B29D 85A4                     000007A4   2711+         LFPC  FPCINIT           initialize FPC
                                                   2712+*         LFPC  =XL4'08000000'          set trap exception
00003434  E320 500C 0014                000033AC   2713+         LGF   R2,V2_41          get v2
0000343A  E762 0000 0806                00000000   2714+         VL    V22,0(R2)
00003440  E666 0000 1C5D                           2715+         VCFN  V22,V22,1,0       test instruction (dest is source)
00003446  B29C 5040                     000033E0   2716+         STFPC FPC_R_41          save FPC
0000344A  E760 5028 080E                000033C8   2717+         VST   V22,V1O41         save instruction result
00003450  07FB                                     2718+         BR    R11               return
00003454                                           2719+RE41     DS    0F                expected 16 byte result
00003454                                           2720+         DROP  R5
00003454  00008000 00000000                        2721          DC    XL16'00008000000000000000000000000000'
0000345C  00000000 00000000
00003464  00008000 00000000                        2722          DC    XL16'00008000000000000000000000000000'
0000346C  00000000 00000000
                                                   2723
                                                   2724 * 1.0, -1
                                                   2725          VRR_A VCFN,1,0,00,00,N
00003478                                           2726+         DS    0FD
00003478                        00003478           2727+         USING *,R5              base for test data and test routine
00003478  00003508                                 2728+T42      DC    A(X42)            address of test routine
0000347C  002A                                     2729+         DC    H'42'             test number
0000347E  00                                       2730+         DC    X'00'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000347F  D5                                      2731+          DC    CL1'N'              Y = skip cross check
00003480  01                                      2732+          DC    HL1'1'              m3
00003481  00                                      2733+          DC    HL1'0'              m4
00003482  00                                      2734+FLG42     DC    X'00'               expected FPC flags
00003483  00                                      2735+VXC42     DC    X'00'               expected VXC
00003484  0000353C                                2736+V2_42     DC    A(RE42+16)          address of v2: 16-byte packed decimal
00003488  E5C3C6D5 40404040                       2737+          DC    CL8'VCFN'           instruction name
00003490  00000010                                2738+          DC    A(16)               result length
00003494  0000352C                                2739+          DC    A(RE42)             address of expected resul
00003498  00000000 00000000                       2740+          DS    FD                  gap
000034A0  00000000 00000000                       2741+V1O42     DS    XL16                V1 output
000034A8  00000000 00000000
000034B0  00000000 00000000                       2742+          DS    FD                     gap
000034B8  00000000                                2743+FPC_R_42  DS    F                   FPC after instruction
000034C0  00000000 00000000                       2744+          DS    FD                     gap
000034C8  40404040 40404040                       2745+          DC    CL8' '              was cross check skipped?
000034D0  00000000 00000000                       2746+          DS    FD                     gap
000034D8  00000000 00000000                       2747+XCO42     DS    XL16                Cross check Output
000034E0  00000000 00000000
000034E8  00000000 00000000                       2748+          DS    FD                     gap
000034F0  00000000                                2749+FPC_XC_42 DS    F                   FPC after cross check
000034F8  00000000 00000000                       2750+          DS    FD                     gap
00003500  00000000                                2751+          DS    F                   debug area
00003504  00000000                                2752+          DS    F
                                                  2753+*
00003508                                          2754+X42       DS    0F
00003508  B29D 85A4                     000007A4  2755+          LFPC  FPCINIT             initialize FPC
                                                  2756+*          LFPC  =XL4'08000000'            set trap exception
0000350C  E320 500C 0014                00003484  2757+          LGF   R2,V2_42            get v2
00003512  E762 0000 0806                00000000  2758+          VL    V22,0(R2)
00003518  E666 0000 1C5D                          2759+          VCFN  V22,V22,1,0         test instruction (dest is source)
0000351E  B29C 5040                     000034B8  2760+          STFPC FPC_R_42            save FPC
00003522  E760 5028 080E                000034A0  2761+          VST   V22,V1O42           save instruction result
00003528  07FB                                    2762+          BR    R11                 return
0000352C                                          2763+RE42      DS    0F                  expected 16 byte result
0000352C                                          2764+          DROP  R5
0000352C  3C000000 BC000000                       2765           DC    XL16'3C000000BC00000000000000000F000'
00003534  00000000 0000F000
0000353C  3E000000 BE000000                       2766           DC    XL16'3E000000BE00000000000000000D800'
00003544  00000000 0000D800
                                                  2767
                                                  2768 * 0.5
                                                  2769           VRR_A VCFN,1,0,00,00,N
00003550                                          2770+          DS    0FD
00003550                        00003550          2771+          USING *,R5                base for test data and test routine
00003550  000035E0                                2772+T43       DC    A(X43)              address of test routine
00003554  002B                                    2773+          DC    H'43'               test number
00003556  00                                      2774+          DC    X'00'
00003557  D5                                      2775+          DC    CL1'N'              Y = skip cross check
00003558  01                                      2776+          DC    HL1'1'              m3
00003559  00                                      2777+          DC    HL1'0'              m4
0000355A  00                                      2778+FLG43     DC    X'00'               expected FPC flags
0000355B  00                                      2779+VXC43     DC    X'00'               expected VXC
0000355C  00003614                                2780+V2_43     DC    A(RE43+16)          address of v2: 16-byte packed decimal
00003560  E5C3C6D5 40404040                       2781+          DC    CL8'VCFN'           instruction name
00003568  00000010                                2782+          DC    A(16)               result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000356C  00003604                                2783+          DC    A(RE43)            address of expected resul
00003570  00000000 00000000                       2784+          DS    FD                 gap
00003578  00000000 00000000                       2785+V1O43     DS    XL16               V1 output
00003580  00000000 00000000
00003588  00000000 00000000                       2786+          DS    FD                    gap
00003590  00000000                                2787+FPC_R_43  DS    F                  FPC after instruction
00003598  00000000 00000000                       2788+          DS    FD                    gap
000035A0  40404040 40404040                       2789+          DC    CL8' '             was cross check skipped?
000035A8  00000000 00000000                       2790+          DS    FD                    gap
000035B0  00000000 00000000                       2791+XCO43     DS    XL16               Cross check Output
000035B8  00000000 00000000
000035C0  00000000 00000000                       2792+          DS    FD                    gap
000035C8  00000000                                2793+FPC_XC_43 DS    F                  FPC after cross check
000035D0  00000000 00000000                       2794+          DS    FD                    gap
000035D8  00000000                                2795+          DS    F                  debug area
000035DC  00000000                                2796+          DS    F
                                                  2797+*
000035E0                                          2798+X43       DS    0F
000035E0  B29D 85A4                    000007A4   2799+          LFPC  FPCINIT            initialize FPC
                                                  2800+*          LFPC  =XL4'08000000'          set trap exception
000035E4  E320 500C 0014               0000355C   2801+          LGF   R2,V2_43           get v2
000035EA  E762 0000 0806               00000000   2802+          VL    V22,0(R2)
000035F0  E666 0000 1C5D                          2803+          VCFN  V22,V22,1,0        test instruction (dest is source)
000035F6  B29C 5040                    00003590   2804+          STFPC FPC_R_43           save FPC
000035FA  E760 5028 080E               00003578   2805+          VST   V22,V1O43          save instruction result
00003600  07FB                                    2806+          BR    R11                return
00003604                                          2807+RE43      DS    0F                 expected 16 byte result
00003604                                          2808+          DROP  R5
00003604  38000000 00000000                       2809           DC    XL16'380000000000000000000000000F000'
0000360C  00000000 0000F000
00003614  3C000000 00000000                       2810           DC    XL16'3C000000000000000000000000D800'
0000361C  00000000 0000D800
                                                  2811
                                                  2812 * 1/64
                                                  2813           VRR_A VCFN,1,0,00,00,N
00003628                                          2814+          DS    0FD
00003628                       00003628           2815+          USING *,R5               base for test data and test routine
00003628  000036B8                                2816+T44       DC    A(X44)             address of test routine
0000362C  002C                                    2817+          DC    H'44'              test number
0000362E  00                                      2818+          DC    X'00'
0000362F  D5                                      2819+          DC    CL1'N'             Y = skip cross check
00003630  01                                      2820+          DC    HL1'1'             m3
00003631  00                                      2821+          DC    HL1'0'             m4
00003632  00                                      2822+FLG44     DC    X'00'              expected FPC flags
00003633  00                                      2823+VXC44     DC    X'00'              expected VXC
00003634  000036EC                                2824+V2_44     DC    A(RE44+16)         address of v2: 16-byte packed decimal
00003638  E5C3C6D5 40404040                       2825+          DC    CL8'VCFN'          instruction name
00003640  00000010                                2826+          DC    A(16)              result length
00003644  000036DC                                2827+          DC    A(RE44)            address of expected resul
00003648  00000000 00000000                       2828+          DS    FD                 gap
00003650  00000000 00000000                       2829+V1O44     DS    XL16               V1 output
00003658  00000000 00000000
00003660  00000000 00000000                       2830+          DS    FD                    gap
00003668  00000000                                2831+FPC_R_44  DS    F                  FPC after instruction
00003670  00000000 00000000                       2832+          DS    FD                    gap
00003678  40404040 40404040                       2833+          DC    CL8' '             was cross check skipped?
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003680  00000000 00000000                        2834+          DS    FD                    gap
00003688  00000000 00000000                        2835+XCO44     DS    XL16               Cross check Output
00003690  00000000 00000000
00003698  00000000 00000000                        2836+          DS    FD                    gap
000036A0  00000000                                 2837+FPC_XC_44 DS    F                  FPC after cross check
000036A8  00000000 00000000                        2838+          DS    FD                    gap
000036B0  00000000                                 2839+          DS    F                  debug area
000036B4  00000000                                 2840+          DS    F
                                                   2841+*
000036B8                                           2842+X44       DS    0F
000036B8  B29D 85A4                     000007A4   2843+          LFPC  FPCINIT            initialize FPC
                                                   2844+*          LFPC  =XL4'08000000'         set trap exception
000036BC  E320 500C 0014                00003634   2845+          LGF   R2,V2_44           get v2
000036C2  E762 0000 0806                00000000   2846+          VL    V22,0(R2)
000036C8  E666 0000 1C5D                           2847+          VCFN  V22,V22,1,0        test instruction (dest is source)
000036CE  B29C 5040                     00003668   2848+          STFPC FPC_R_44           save FPC
000036D2  E760 5028 080E                00003650   2849+          VST   V22,V1O44          save instruction result
000036D8  07FB                                     2850+          BR    R11                return
000036DC                                           2851+RE44      DS    0F                 expected 16 byte result
000036DC                                           2852+          DROP  R5
000036DC  24000000 00000000                        2853           DC    XL16'24000000000000000000000000F000'
000036E4  00000000 0000F000
000036EC  32000000 00000000                        2854           DC    XL16'32000000000000000000000000D800'
000036F4  00000000 0000D800
                                                   2855
                                                   2856 * +0, -0
                                                   2857           VRR_A VCFN,1,0,00,00,N
00003700                                           2858+          DS    0FD
00003700                        00003700           2859+          USING *,R5               base for test data and test routine
00003700  00003790                                 2860+T45       DC    A(X45)             address of test routine
00003704  002D                                     2861+          DC    H'45'              test number
00003706  00                                       2862+          DC    X'00'
00003707  D5                                       2863+          DC    CL1'N'             Y = skip cross check
00003708  01                                       2864+          DC    HL1'1'             m3
00003709  00                                       2865+          DC    HL1'0'             m4
0000370A  00                                       2866+FLG45     DC    X'00'              expected FPC flags
0000370B  00                                       2867+VXC45     DC    X'00'              expected VXC
0000370C  000037C4                                 2868+V2_45     DC    A(RE45+16)         address of v2: 16-byte packed decimal
00003710  E5C3C6D5 40404040                        2869+          DC    CL8'VCFN'          instruction name
00003718  00000010                                 2870+          DC    A(16)              result length
0000371C  000037B4                                 2871+          DC    A(RE45)            address of expected resul
00003720  00000000 00000000                        2872+          DS    FD                 gap
00003728  00000000 00000000                        2873+V1O45     DS    XL16               V1 output
00003730  00000000 00000000
00003738  00000000 00000000                        2874+          DS    FD                    gap
00003740  00000000                                 2875+FPC_R_45  DS    F                  FPC after instruction
00003748  00000000 00000000                        2876+          DS    FD                    gap
00003750  40404040 40404040                        2877+          DC    CL8' '             was cross check skipped?
00003758  00000000 00000000                        2878+          DS    FD                    gap
00003760  00000000 00000000                        2879+XCO45     DS    XL16               Cross check Output
00003768  00000000 00000000
00003770  00000000 00000000                        2880+          DS    FD                    gap
00003778  00000000                                 2881+FPC_XC_45 DS    F                  FPC after cross check
00003780  00000000 00000000                        2882+          DS    FD                    gap
00003788  00000000                                 2883+          DS    F                  debug area
0000378C  00000000                                 2884+          DS    F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  2885+*
00003790                                          2886+X45      DS    0F
00003790  B29D 85A4                     000007A4  2887+         LFPC  FPCINIT           initialize FPC
                                                  2888+*         LFPC  =XL4'08000000'         set trap exception
00003794  E320 500C 0014                0000370C  2889+         LGF   R2,V2_45          get v2
0000379A  E762 0000 0806                00000000  2890+         VL    V22,0(R2)
000037A0  E666 0000 1C5D                          2891+         VCFN  V22,V22,1,0       test instruction (dest is source)
000037A6  B29C 5040                     00003740  2892+         STFPC FPC_R_45          save FPC
000037AA  E760 5028 080E                00003728  2893+         VST   V22,V1O45         save instruction result
000037B0  07FB                                    2894+         BR    R11               return
000037B4                                          2895+RE45     DS    0F                expected 16 byte result
000037B4                                          2896+         DROP  R5
000037B4  00008000 00000000                       2897          DC    XL16'00008000000000000000000000000F000'
000037BC  00000000 0000F000
000037C4  00008000 00000000                       2898          DC    XL16'00008000000000000000000000000D800'
000037CC  00000000 0000D800
                                                  2899
                                                  2900 * -15
                                                  2901          VRR_A VCFN,1,0,00,00,N
000037D8                                          2902+         DS    0FD
000037D8                        000037D8          2903+         USING *,R5              base for test data and test routine
000037D8  00003868                                2904+T46      DC    A(X46)            address of test routine
000037DC  002E                                    2905+         DC    H'46'             test number
000037DE  00                                      2906+         DC    X'00'
000037DF  D5                                      2907+         DC    CL1'N'            Y = skip cross check
000037E0  01                                      2908+         DC    HL1'1'            m3
000037E1  00                                      2909+         DC    HL1'0'            m4
000037E2  00                                      2910+FLG46    DC    X'00'             expected FPC flags
000037E3  00                                      2911+VXC46    DC    X'00'             expected VXC
000037E4  0000389C                                2912+V2_46    DC    A(RE46+16)        address of v2: 16-byte packed decimal
000037E8  E5C3C6D5 40404040                       2913+         DC    CL8'VCFN'         instruction name
000037F0  00000010                                2914+         DC    A(16)             result length
000037F4  0000388C                                2915+         DC    A(RE46)           address of expected resul
000037F8  00000000 00000000                       2916+         DS    FD                gap
00003800  00000000 00000000                       2917+V1O46    DS    XL16              V1 output
00003808  00000000 00000000
00003810  00000000 00000000                       2918+         DS    FD                   gap
00003818  00000000                                2919+FPC_R_46 DS    F                 FPC after instruction
00003820  00000000 00000000                       2920+         DS    FD                   gap
00003828  40404040 40404040                       2921+         DC    CL8' '            was cross check skipped?
00003830  00000000 00000000                       2922+         DS    FD                   gap
00003838  00000000 00000000                       2923+XCO46    DS    XL16              Cross check Output
00003840  00000000 00000000
00003848  00000000 00000000                       2924+         DS    FD                   gap
00003850  00000000                                2925+FPC_XC_46 DS   F                 FPC after cross check
00003858  00000000 00000000                       2926+         DS    FD                   gap
00003860  00000000                                2927+         DS    F                 debug area
00003864  00000000                                2928+         DS    F
                                                  2929+*
00003868                                          2930+X46      DS    0F
00003868  B29D 85A4                     000007A4  2931+         LFPC  FPCINIT           initialize FPC
                                                  2932+*         LFPC  =XL4'08000000'         set trap exception
0000386C  E320 500C 0014                000037E4  2933+         LGF   R2,V2_46          get v2
00003872  E762 0000 0806                00000000  2934+         VL    V22,0(R2)
00003878  E666 0000 1C5D                          2935+         VCFN  V22,V22,1,0       test instruction (dest is source)
0000387E  B29C 5040                     00003818  2936+         STFPC FPC_R_46          save FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00003882  E760 5028 080E                00003800  2937+         VST   V22,V1O46         save instruction result
00003888  07FB                                    2938+         BR    R11               return
0000388C                                          2939+RE46     DS    0F                expected 16 byte result
0000388C                                          2940+         DROP  R5
0000388C  CB800000 00000000                       2941          DC    XL16'CB800000000000000000000000F000'
00003894  00000000 0000F000
0000389C  C5C00000 00000000                       2942          DC    XL16'C5C000000000000000000000000D800'
000038A4  00000000 0000D800
                                                  2943
                                                  2944 * 20/7 (about)
                                                  2945          VRR_A VCFN,1,0,00,00,N
000038B0                                          2946+         DS    0FD
000038B0                      000038B0            2947+         USING *,R5              base for test data and test routine
000038B0  00003940                                2948+T47      DC    A(X47)            address of test routine
000038B4  002F                                    2949+         DC    H'47'             test number
000038B6  00                                      2950+         DC    X'00'
000038B7  D5                                      2951+         DC    CL1'N'            Y = skip cross check
000038B8  01                                      2952+         DC    HL1'1'            m3
000038B9  00                                      2953+         DC    HL1'0'            m4
000038BA  00                                      2954+FLG47    DC    X'00'             expected FPC flags
000038BB  00                                      2955+VXC47    DC    X'00'             expected VXC
000038BC  00003974                                2956+V2_47    DC    A(RE47+16)        address of v2: 16-byte packed decimal
000038C0  E5C3C6D5 40404040                       2957+         DC    CL8'VCFN'         instruction name
000038C8  00000010                                2958+         DC    A(16)             result length
000038CC  00003964                                2959+         DC    A(RE47)           address of expected resul
000038D0  00000000 00000000                       2960+         DS    FD                gap
000038D8  00000000 00000000                       2961+V1O47    DS    XL16              V1 output
000038E0  00000000 00000000
000038E8  00000000 00000000                       2962+         DS    FD                   gap
000038F0  00000000                                2963+FPC_R_47 DS    F                 FPC after instruction
000038F8  00000000 00000000                       2964+         DS    FD                   gap
00003900  40404040 40404040                       2965+         DC    CL8' '            was cross check skipped?
00003908  00000000 00000000                       2966+         DS    FD                   gap
00003910  00000000 00000000                       2967+XCO47    DS    XL16              Cross check Output
00003918  00000000 00000000
00003920  00000000 00000000                       2968+         DS    FD                   gap
00003928  00000000                                2969+FPC_XC_47 DS   F                 FPC after cross check
00003930  00000000 00000000                       2970+         DS    FD                   gap
00003938  00000000                                2971+         DS    F                 debug area
0000393C  00000000                                2972+         DS    F
                                                  2973+*
00003940                                          2974+X47      DS    0F
00003940  B29D 85A4                     000007A4  2975+         LFPC  FPCINIT           initialize FPC
                                                  2976+*         LFPC  =XL4'08000000'         set trap exception
00003944  E320 500C 0014                000038BC  2977+         LGF   R2,V2_47          get v2
0000394A  E762 0000 0806                00000000  2978+         VL    V22,0(R2)
00003950  E666 0000 1C5D                          2979+         VCFN  V22,V22,1,0       test instruction (dest is source)
00003956  B29C 5040                     000038F0  2980+         STFPC FPC_R_47          save FPC
0000395A  E760 5028 080E                000038D8  2981+         VST   V22,V1O47         save instruction result
00003960  07FB                                    2982+         BR    R11               return
00003964                                          2983+RE47     DS    0F                expected 16 byte result
00003964                                          2984+         DROP  R5
00003964  41B60000 00000000                       2985          DC    XL16'41B600000000000000000000000F000'
0000396C  00000000 0000F000
00003974  40DB0000 00000000                       2986          DC    XL16'40DB000000000000000000000000D800'
0000397C  00000000 0000D800
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2987
                                                   2988 * additional tests
                                                   2989 * max  tiny:  (1 - 2^-11) * 2^16 (65504) +1 (overflow)
                                                   2990          VRR_A VCFN,1,0,20,03,S
00003988                                           2991+         DS    0FD
00003988                       00003988            2992+         USING *,R5              base for test data and test routine
00003988  00003A18                                 2993+T48      DC    A(X48)            address of test routine
0000398C  0030                                     2994+         DC    H'48'             test number
0000398E  00                                       2995+         DC    X'00'
0000398F  E2                                       2996+         DC    CL1'S'            Y = skip cross check
00003990  01                                       2997+         DC    HL1'1'            m3
00003991  00                                       2998+         DC    HL1'0'            m4
00003992  20                                       2999+FLG48    DC    X'20'             expected FPC flags
00003993  03                                       3000+VXC48    DC    X'03'             expected VXC
00003994  00003A4C                                 3001+V2_48    DC    A(RE48+16)        address of v2: 16-byte packed decimal
00003998  E5C3C6D5 40404040                        3002+         DC    CL8'VCFN'         instruction name
000039A0  00000010                                 3003+         DC    A(16)             result length
000039A4  00003A3C                                 3004+         DC    A(RE48)           address of expected resul
000039A8  00000000 00000000                        3005+         DS    FD                gap
000039B0  00000000 00000000                        3006+V1O48    DS    XL16              V1 output
000039B8  00000000 00000000
000039C0  00000000 00000000                        3007+         DS    FD                   gap
000039C8  00000000                                 3008+FPC_R_48 DS    F                 FPC after instruction
000039D0  00000000 00000000                        3009+         DS    FD                   gap
000039D8  40404040 40404040                        3010+         DC    CL8' '            was cross check skipped?
000039E0  00000000 00000000                        3011+         DS    FD                   gap
000039E8  00000000 00000000                        3012+XCO48    DS    XL16              Cross check Output
000039F0  00000000 00000000
000039F8  00000000 00000000                        3013+         DS    FD                   gap
00003A00  00000000                                 3014+FPC_XC_48 DS   F                 FPC after cross check
00003A08  00000000 00000000                        3015+         DS    FD                   gap
00003A10  00000000                                 3016+         DS    F                 debug area
00003A14  00000000                                 3017+         DS    F
                                                   3018+*
00003A18                                           3019+X48      DS    0F
00003A18  B29D 85A4                     000007A4   3020+         LFPC  FPCINIT           initialize FPC
                                                   3021+*         LFPC  =XL4'08000000'         set trap exception
00003A1C  E320 500C 0014                00003994   3022+         LGF   R2,V2_48          get v2
00003A22  E762 0000 0806                00000000   3023+         VL    V22,0(R2)
00003A28  E666 0000 1C5D                           3024+         VCFN  V22,V22,1,0       test instruction (dest is source)
00003A2E  B29C 5040                     000039C8   3025+         STFPC FPC_R_48          save FPC
00003A32  E760 5028 080E                000039B0   3026+         VST   V22,V1O48         save instruction result
00003A38  07FB                                     3027+         BR    R11               return
00003A3C                                           3028+RE48     DS    0F                expected 16 byte result
00003A3C                                           3029+         DROP  R5
00003A3C  7C000000 00000000                        3030          DC    XL16'7C000000000000000000000000F000'
00003A44  00000000 0000F000
00003A4C  5E000000 00000000                        3031          DC    XL16'5E000000000000000000000000D800'
00003A54  00000000 0000D800
                                                   3032
                                                   3033 * min tiny (normal): 2^-14 (0.00006103515625)
                                                   3034          VRR_A VCFN,1,0,00,00,N
00003A60                                           3035+         DS    0FD
00003A60                       00003A60            3036+         USING *,R5              base for test data and test routine
00003A60  00003AF0                                 3037+T49      DC    A(X49)            address of test routine
00003A64  0031                                     3038+         DC    H'49'             test number
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003A66  00                                       3039+          DC    X'00'
00003A67  D5                                       3040+          DC    CL1'N'            Y = skip cross check
00003A68  01                                       3041+          DC    HL1'1'            m3
00003A69  00                                       3042+          DC    HL1'0'            m4
00003A6A  00                                       3043+FLG49     DC    X'00'             expected FPC flags
00003A6B  00                                       3044+VXC49     DC    X'00'             expected VXC
00003A6C  00003B24                                 3045+V2_49     DC    A(RE49+16)        address of v2: 16-byte packed decimal
00003A70  E5C3C6D5 40404040                        3046+          DC    CL8'VCFN'         instruction name
00003A78  00000010                                 3047+          DC    A(16)             result length
00003A7C  00003B14                                 3048+          DC    A(RE49)           address of expected resul
00003A80  00000000 00000000                        3049+          DS    FD                gap
00003A88  00000000 00000000                        3050+V1O49     DS    XL16              V1 output
00003A90  00000000 00000000
00003A98  00000000 00000000                        3051+          DS    FD                   gap
00003AA0  00000000                                 3052+FPC_R_49 DS    F                 FPC after instruction
00003AA8  00000000 00000000                        3053+          DS    FD                   gap
00003AB0  40404040 40404040                        3054+          DC    CL8' '            was cross check skipped?
00003AB8  00000000 00000000                        3055+          DS    FD                   gap
00003AC0  00000000 00000000                        3056+XCO49     DS    XL16              Cross check Output
00003AC8  00000000 00000000
00003AD0  00000000 00000000                        3057+          DS    FD                   gap
00003AD8  00000000                                 3058+FPC_XC_49 DS    F                 FPC after cross check
00003AE0  00000000 00000000                        3059+          DS    FD                   gap
00003AE8  00000000                                 3060+          DS    F                 debug area
00003AEC  00000000                                 3061+          DS    F
                                                   3062+*
00003AF0                                           3063+X49       DS    0F
00003AF0  B29D 85A4                     000007A4   3064+          LFPC  FPCINIT           initialize FPC
                                                   3065+*          LFPC  =XL4'08000000'          set trap exception
00003AF4  E320 500C 0014                00003A6C   3066+          LGF   R2,V2_49          get v2
00003AFA  E762 0000 0806                00000000   3067+          VL    V22,0(R2)
00003B00  E666 0000 1C5D                           3068+          VCFN  V22,V22,1,0       test instruction (dest is source)
00003B06  B29C 5040                     00003AA0   3069+          STFPC FPC_R_49          save FPC
00003B0A  E760 5028 080E                00003A88   3070+          VST   V22,V1O49         save instruction result
00003B10  07FB                                     3071+          BR    R11               return
00003B14                                           3072+RE49      DS    0F                expected 16 byte result
00003B14                                           3073+          DROP  R5
00003B14  04000000 00000000                        3074           DC    XL16'04000000000000000000000000000F000'
00003B1C  00000000 0000F000
00003B24  22000000 00000000                        3075           DC    XL16'22000000000000000000000000000D800'
00003B2C  00000000 0000D800
                                                   3076
                                                   3077 * min tiny (subnormal): 2^-24 (0.00000005960464477539062 5)
                                                   3078           VRR_A VCFN,1,0,00,00,N
00003B38                                           3079+          DS    0FD
00003B38                        00003B38           3080+          USING *,R5              base for test data and test routine
00003B38  00003BC8                                 3081+T50       DC    A(X50)            address of test routine
00003B3C  0032                                     3082+          DC    H'50'             test number
00003B3E  00                                       3083+          DC    X'00'
00003B3F  D5                                       3084+          DC    CL1'N'            Y = skip cross check
00003B40  01                                       3085+          DC    HL1'1'            m3
00003B41  00                                       3086+          DC    HL1'0'            m4
00003B42  00                                       3087+FLG50     DC    X'00'             expected FPC flags
00003B43  00                                       3088+VXC50     DC    X'00'             expected VXC
00003B44  00003BFC                                 3089+V2_50     DC    A(RE50+16)        address of v2: 16-byte packed decimal
00003B48  E5C3C6D5 40404040                        3090+          DC    CL8'VCFN'         instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003B50  00000010                                 3091+         DC    A(16)              result length
00003B54  00003BEC                                 3092+         DC    A(RE50)            address of expected resul
00003B58  00000000 00000000                        3093+         DS    FD                 gap
00003B60  00000000 00000000                        3094+V1O50    DS    XL16               V1 output
00003B68  00000000 00000000
00003B70  00000000 00000000                        3095+         DS    FD                    gap
00003B78  00000000                                 3096+FPC_R_50 DS    F                  FPC after instruction
00003B80  00000000 00000000                        3097+         DS    FD                    gap
00003B88  40404040 40404040                        3098+         DC    CL8' '             was cross check skipped?
00003B90  00000000 00000000                        3099+         DS    FD                    gap
00003B98  00000000 00000000                        3100+XCO50    DS    XL16               Cross check Output
00003BA0  00000000 00000000
00003BA8  00000000 00000000                        3101+         DS    FD                    gap
00003BB0  00000000                                 3102+FPC_XC_50 DS   F                  FPC after cross check
00003BB8  00000000 00000000                        3103+         DS    FD                    gap
00003BC0  00000000                                 3104+         DS    F                  debug area
00003BC4  00000000                                 3105+         DS    F
                                                   3106+*
00003BC8                                           3107+X50      DS    0F
00003BC8  B29D 85A4                     000007A4   3108+         LFPC  FPCINIT            initialize FPC
                                                   3109+*         LFPC  =XL4'08000000'         set trap exception
00003BCC  E320 500C 0014                00003B44   3110+         LGF   R2,V2_50           get v2
00003BD2  E762 0000 0806                00000000   3111+         VL    V22,0(R2)
00003BD8  E666 0000 1C5D                           3112+         VCFN  V22,V22,1,0        test instruction (dest is source)
00003BDE  B29C 5040                     00003B78   3113+         STFPC FPC_R_50           save FPC
00003BE2  E760 5028 080E                00003B60   3114+         VST   V22,V1O50          save instruction result
00003BE8  07FB                                     3115+         BR    R11                return
00003BEC                                           3116+RE50     DS    0F                 expected 16 byte result
00003BEC                                           3117+         DROP  R5
00003BEC  00010000 00000000                        3118          DC    XL16'00010000000000000000000000000F000'
00003BF4  00000000 0000F000
00003BFC  0E000000 00000000                        3119          DC    XL16'0E000000000000000000000000000D800'
00003C04  00000000 0000D800
                                                   3120
                                                   3121 *  2 underflows
                                                   3122          VRR_A VCFN,1,0,10,14,S
00003C10                                           3123+         DS    0FD
00003C10                        00003C10           3124+         USING *,R5               base for test data and test routine
00003C10  00003CA0                                 3125+T51      DC    A(X51)             address of test routine
00003C14  0033                                     3126+         DC    H'51'              test number
00003C16  00                                       3127+         DC    X'00'
00003C17  E2                                       3128+         DC    CL1'S'             Y = skip cross check
00003C18  01                                       3129+         DC    HL1'1'             m3
00003C19  00                                       3130+         DC    HL1'0'             m4
00003C1A  10                                       3131+FLG51    DC    X'10'              expected FPC flags
00003C1B  14                                       3132+VXC51    DC    X'14'              expected VXC
00003C1C  00003CD4                                 3133+V2_51    DC    A(RE51+16)         address of v2: 16-byte packed decimal
00003C20  E5C3C6D5 40404040                        3134+         DC    CL8'VCFN'          instruction name
00003C28  00000010                                 3135+         DC    A(16)              result length
00003C2C  00003CC4                                 3136+         DC    A(RE51)            address of expected resul
00003C30  00000000 00000000                        3137+         DS    FD                 gap
00003C38  00000000 00000000                        3138+V1O51    DS    XL16               V1 output
00003C40  00000000 00000000
00003C48  00000000 00000000                        3139+         DS    FD                    gap
00003C50  00000000                                 3140+FPC_R_51 DS    F                  FPC after instruction
00003C58  00000000 00000000                        3141+         DS    FD                    gap
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00003C60  40404040 40404040                         3142+          DC    CL8' '             was cross check skipped?
00003C68  00000000 00000000                         3143+          DS    FD                    gap
00003C70  00000000 00000000                         3144+XCO51     DS    XL16               Cross check Output
00003C78  00000000 00000000
00003C80  00000000 00000000                         3145+          DS    FD                    gap
00003C88  00000000                                  3146+FPC_XC_51 DS    F                  FPC after cross check
00003C90  00000000 00000000                         3147+          DS    FD                    gap
00003C98  00000000                                  3148+          DS    F                  debug area
00003C9C  00000000                                  3149+          DS    F
                                                    3150+*
00003CA0                                            3151+X51       DS    0F
00003CA0  B29D 85A4                     000007A4    3152+          LFPC  FPCINIT            initialize FPC
                                                    3153+*          LFPC  =XL4'08000000'          set trap exception
00003CA4  E320 500C 0014                00003C1C    3154+          LGF   R2,V2_51           get v2
00003CAA  E762 0000 0806                00000000    3155+          VL    V22,0(R2)
00003CB0  E666 0000 1C5D                            3156+          VCFN  V22,V22,1,0        test instruction (dest is source)
00003CB6  B29C 5040                     00003C50    3157+          STFPC FPC_R_51           save FPC
00003CBA  E760 5028 080E                00003C38    3158+          VST   V22,V1O51          save instruction result
00003CC0  07FB                                      3159+          BR    R11                return
00003CC4                                            3160+RE51      DS    0F                 expected 16 byte result
00003CC4                                            3161+          DROP  R5
00003CC4  00000000 00000000                         3162           DC    XL16'000000000000000000000000000F000'
00003CCC  00000000 0000F000
00003CD4  0A000B00 00000000                         3163           DC    XL16'0A000B000000000000000000000D800'
00003CDC  00000000 0000D800
                                                    3164
                                                    3165 * +infinity, -Infinity
                                                    3166           VRR_A VCFN,1,0,80,21,S                    skip xc - invalid
00003CE8                                            3167+          DS    0FD
00003CE8                        00003CE8            3168+          USING *,R5               base for test data and test routine
00003CE8  00003D78                                  3169+T52       DC    A(X52)             address of test routine
00003CEC  0034                                      3170+          DC    H'52'              test number
00003CEE  00                                        3171+          DC    X'00'
00003CEF  E2                                        3172+          DC    CL1'S'             Y = skip cross check
00003CF0  01                                        3173+          DC    HL1'1'             m3
00003CF1  00                                        3174+          DC    HL1'0'             m4
00003CF2  80                                        3175+FLG52     DC    X'80'              expected FPC flags
00003CF3  21                                        3176+VXC52     DC    X'21'              expected VXC
00003CF4  00003DAC                                  3177+V2_52     DC    A(RE52+16)         address of v2: 16-byte packed decimal
00003CF8  E5C3C6D5 40404040                         3178+          DC    CL8'VCFN'          instruction name
00003D00  00000010                                  3179+          DC    A(16)              result length
00003D04  00003D9C                                  3180+          DC    A(RE52)            address of expected resul
00003D08  00000000 00000000                         3181+          DS    FD                 gap
00003D10  00000000 00000000                         3182+V1O52     DS    XL16               V1 output
00003D18  00000000 00000000
00003D20  00000000 00000000                         3183+          DS    FD                    gap
00003D28  00000000                                  3184+FPC_R_52  DS    F                  FPC after instruction
00003D30  00000000 00000000                         3185+          DS    FD                    gap
00003D38  40404040 40404040                         3186+          DC    CL8' '             was cross check skipped?
00003D40  00000000 00000000                         3187+          DS    FD                    gap
00003D48  00000000 00000000                         3188+XCO52     DS    XL16               Cross check Output
00003D50  00000000 00000000
00003D58  00000000 00000000                         3189+          DS    FD                    gap
00003D60  00000000                                  3190+FPC_XC_52 DS    F                  FPC after cross check
00003D68  00000000 00000000                         3191+          DS    FD                    gap
00003D70  00000000                                  3192+          DS    F                  debug area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00003D74  00000000                                3193+         DS    F
                                                  3194+*
00003D78                                          3195+X52      DS    0F
00003D78  B29D 85A4                     000007A4  3196+         LFPC  FPCINIT           initialize FPC
                                                  3197+*         LFPC  =XL4'08000000'         set trap exception
00003D7C  E320 500C 0014                00003CF4  3198+         LGF   R2,V2_52          get v2
00003D82  E762 0000 0806                00000000  3199+         VL    V22,0(R2)
00003D88  E666 0000 1C5D                          3200+         VCFN  V22,V22,1,0       test instruction (dest is source)
00003D8E  B29C 5040                     00003D28  3201+         STFPC FPC_R_52          save FPC
00003D92  E760 5028 080E                00003D10  3202+         VST   V22,V1O52         save instruction result
00003D98  07FB                                    3203+         BR    R11               return
00003D9C                                          3204+RE52     DS    0F                expected 16 byte result
00003D9C                                          3205+         DROP  R5
00003D9C  7E000000 FE000000                       3206          DC    XL16'7E000000FE00000000000000000F000'
00003DA4  00000000 0000F000
00003DAC  7FFF0000 FFFF0000                       3207          DC    XL16'7FFF0000FFFF000000000000000D800'
00003DB4  00000000 0000D800
                                                  3208
                                                  3209 * inexact - bad m3
                                                  3210          VRR_A VCFN,5,0,08,05,S                skip xc - inexact
00003DC0                                          3211+         DS    0FD
00003DC0                        00003DC0          3212+         USING *,R5              base for test data and test routine
00003DC0  00003E50                                3213+T53      DC    A(X53)            address of test routine
00003DC4  0035                                    3214+         DC    H'53'             test number
00003DC6  00                                      3215+         DC    X'00'
00003DC7  E2                                      3216+         DC    CL1'S'            Y = skip cross check
00003DC8  05                                      3217+         DC    HL1'5'            m3
00003DC9  00                                      3218+         DC    HL1'0'            m4
00003DCA  08                                      3219+FLG53    DC    X'08'             expected FPC flags
00003DCB  05                                      3220+VXC53    DC    X'05'             expected VXC
00003DCC  00003E84                                3221+V2_53    DC    A(RE53+16)        address of v2: 16-byte packed decimal
00003DD0  E5C3C6D5 40404040                       3222+         DC    CL8'VCFN'         instruction name
00003DD8  00000010                                3223+         DC    A(16)             result length
00003DDC  00003E74                                3224+         DC    A(RE53)           address of expected resul
00003DE0  00000000 00000000                       3225+         DS    FD                gap
00003DE8  00000000 00000000                       3226+V1O53    DS    XL16              V1 output
00003DF0  00000000 00000000
00003DF8  00000000 00000000                       3227+         DS    FD                   gap
00003E00  00000000                                3228+FPC_R_53 DS    F                 FPC after instruction
00003E08  00000000 00000000                       3229+         DS    FD                   gap
00003E10  40404040 40404040                       3230+         DC    CL8' '            was cross check skipped?
00003E18  00000000 00000000                       3231+         DS    FD                   gap
00003E20  00000000 00000000                       3232+XCO53    DS    XL16              Cross check Output
00003E28  00000000 00000000
00003E30  00000000 00000000                       3233+         DS    FD                   gap
00003E38  00000000                                3234+FPC_XC_53 DS   F                 FPC after cross check
00003E40  00000000 00000000                       3235+         DS    FD                   gap
00003E48  00000000                                3236+         DS    F                 debug area
00003E4C  00000000                                3237+         DS    F
                                                  3238+*
00003E50                                          3239+X53      DS    0F
00003E50  B29D 85A4                     000007A4  3240+         LFPC  FPCINIT           initialize FPC
                                                  3241+*         LFPC  =XL4'08000000'         set trap exception
00003E54  E320 500C 0014                00003DCC  3242+         LGF   R2,V2_53          get v2
00003E5A  E762 0000 0806                00000000  3243+         VL    V22,0(R2)
00003E60  E666 0000 5C5D                          3244+         VCFN  V22,V22,5,0       test instruction (dest is source)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00003E66  B29C 5040                     00003E00  3245+         STFPC FPC_R_53          save FPC
00003E6A  E760 5028 080E                00003DE8  3246+         VST   V22,V1O53         save instruction result
00003E70  07FB                                    3247+         BR    R11               return
00003E74                                          3248+RE53     DS    0F                expected 16 byte result
00003E74                                          3249+         DROP  R5
00003E74  00000000 00000000                       3250          DC    XL16'00000000000000000000000000000000'
00003E7C  00000000 00000000
00003E84  00010000 00000000                       3251          DC    XL16'00010000000000000000000000000F000'
00003E8C  00000000 0000F000
                                                  3252
                                                  3253 * inexact - bad m4
                                                  3254          VRR_A VCFN,0,5,08,05,S                    skip xc - inexact
00003E98                                          3255+         DS    0FD
00003E98                        00003E98          3256+         USING *,R5              base for test data and test routine
00003E98  00003F28                                3257+T54      DC    A(X54)            address of test routine
00003E9C  0036                                    3258+         DC    H'54'             test number
00003E9E  00                                      3259+         DC    X'00'
00003E9F  E2                                      3260+         DC    CL1'S'            Y = skip cross check
00003EA0  00                                      3261+         DC    HL1'0'            m3
00003EA1  05                                      3262+         DC    HL1'5'            m4
00003EA2  08                                      3263+FLG54    DC    X'08'             expected FPC flags
00003EA3  05                                      3264+VXC54    DC    X'05'             expected VXC
00003EA4  00003F5C                                3265+V2_54    DC    A(RE54+16)        address of v2: 16-byte packed decimal
00003EA8  E5C3C6D5 40404040                       3266+         DC    CL8'VCFN'         instruction name
00003EB0  00000010                                3267+         DC    A(16)             result length
00003EB4  00003F4C                                3268+         DC    A(RE54)           address of expected resul
00003EB8  00000000 00000000                       3269+         DS    FD                gap
00003EC0  00000000 00000000                       3270+V1O54    DS    XL16              V1 output
00003EC8  00000000 00000000
00003ED0  00000000 00000000                       3271+         DS    FD                   gap
00003ED8  00000000                                3272+FPC_R_54 DS    F                 FPC after instruction
00003EE0  00000000 00000000                       3273+         DS    FD                   gap
00003EE8  40404040 40404040                       3274+         DC    CL8' '            was cross check skipped?
00003EF0  00000000 00000000                       3275+         DS    FD                   gap
00003EF8  00000000 00000000                       3276+XCO54    DS    XL16              Cross check Output
00003F00  00000000 00000000
00003F08  00000000 00000000                       3277+         DS    FD                   gap
00003F10  00000000                                3278+FPC_XC_54 DS   F                 FPC after cross check
00003F18  00000000 00000000                       3279+         DS    FD                   gap
00003F20  00000000                                3280+         DS    F                 debug area
00003F24  00000000                                3281+         DS    F
                                                  3282+*
00003F28                                          3283+X54      DS    0F
00003F28  B29D 85A4                     000007A4  3284+         LFPC  FPCINIT           initialize FPC
                                                  3285+*         LFPC  =XL4'08000000'          set trap exception
00003F2C  E320 500C 0014                00003EA4  3286+         LGF   R2,V2_54          get v2
00003F32  E762 0000 0806                00000000  3287+         VL    V22,0(R2)
00003F38  E666 0005 0C5D                          3288+         VCFN  V22,V22,0,5       test instruction (dest is source)
00003F3E  B29C 5040                     00003ED8  3289+         STFPC FPC_R_54          save FPC
00003F42  E760 5028 080E                00003EC0  3290+         VST   V22,V1O54         save instruction result
00003F48  07FB                                    3291+         BR    R11               return
00003F4C                                          3292+RE54     DS    0F                expected 16 byte result
00003F4C                                          3293+         DROP  R5
00003F4C  00000000 00000000                       3294          DC    XL16'00000000000000000000000000000000'
00003F54  00000000 00000000
00003F5C  00010000 00000000                       3295          DC    XL16'00010000000000000000000000000F000'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00003F64  00000000 0000F000
                                                  3296
                                                  3297 * more tests
                                                  3298 * +3.140625, -3.140625
                                                  3299          VRR_A VCFN,1,0,00,00,N
00003F70                                          3300+         DS    0FD
00003F70                      00003F70            3301+         USING *,R5              base for test data and test routine
00003F70  00004000                                3302+T55      DC    A(X55)            address of test routine
00003F74  0037                                    3303+         DC    H'55'             test number
00003F76  00                                      3304+         DC    X'00'
00003F77  D5                                      3305+         DC    CL1'N'            Y = skip cross check
00003F78  01                                      3306+         DC    HL1'1'            m3
00003F79  00                                      3307+         DC    HL1'0'            m4
00003F7A  00                                      3308+FLG55    DC    X'00'             expected FPC flags
00003F7B  00                                      3309+VXC55    DC    X'00'             expected VXC
00003F7C  00004034                                3310+V2_55    DC    A(RE55+16)        address of v2: 16-byte packed decimal
00003F80  E5C3C6D5 40404040                       3311+         DC    CL8'VCFN'         instruction name
00003F88  00000010                                3312+         DC    A(16)             result length
00003F8C  00004024                                3313+         DC    A(RE55)           address of expected resul
00003F90  00000000 00000000                       3314+         DS    FD                gap
00003F98  00000000 00000000                       3315+V1O55    DS    XL16              V1 output
00003FA0  00000000 00000000
00003FA8  00000000 00000000                       3316+         DS    FD                   gap
00003FB0  00000000                                3317+FPC_R_55 DS    F                 FPC after instruction
00003FB8  00000000 00000000                       3318+         DS    FD                   gap
00003FC0  40404040 40404040                       3319+         DC    CL8' '            was cross check skipped?
00003FC8  00000000 00000000                       3320+         DS    FD                   gap
00003FD0  00000000 00000000                       3321+XCO55    DS    XL16              Cross check Output
00003FD8  00000000 00000000
00003FE0  00000000 00000000                       3322+         DS    FD                   gap
00003FE8  00000000                                3323+FPC_XC_55 DS   F                 FPC after cross check
00003FF0  00000000 00000000                       3324+         DS    FD                   gap
00003FF8  00000000                                3325+         DS    F                 debug area
00003FFC  00000000                                3326+         DS    F
                                                  3327+*
00004000                                          3328+X55      DS    0F
00004000  B29D 85A4                     000007A4  3329+         LFPC  FPCINIT           initialize FPC
                                                  3330+*         LFPC  =XL4'08000000'         set trap exception
00004004  E320 500C 0014                00003F7C  3331+         LGF   R2,V2_55          get v2
0000400A  E762 0000 0806                00000000  3332+         VL    V22,0(R2)
00004010  E666 0000 1C5D                          3333+         VCFN  V22,V22,1,0       test instruction (dest is source)
00004016  B29C 5040                     00003FB0  3334+         STFPC FPC_R_55          save FPC
0000401A  E760 5028 080E                00003F98  3335+         VST   V22,V1O55         save instruction result
00004020  07FB                                    3336+         BR    R11               return
00004024                                          3337+RE55     DS    0F                expected 16 byte result
00004024                                          3338+         DROP  R5
00004024  44480000 C4480000                       3339          DC    XL16'44480000C44800000000000000000000'
0000402C  00000000 00000000
00004034  42240000 C2240000                       3340          DC    XL16'42240000C22400000000000000000000'
0000403C  00000000 00000000
                                                  3341
                                                  3342
                                                  3343 * +27.15625, -27.15625
                                                  3344          VRR_A VCFN,1,0,00,00,N
00004048                                          3345+         DS    0FD
00004048                      00004048            3346+         USING *,R5              base for test data and test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004048  000040D8                                 3347+T56      DC    A(X56)            address of test routine
0000404C  0038                                     3348+         DC    H'56'             test number
0000404E  00                                       3349+         DC    X'00'
0000404F  D5                                       3350+         DC    CL1'N'            Y = skip cross check
00004050  01                                       3351+         DC    HL1'1'            m3
00004051  00                                       3352+         DC    HL1'0'            m4
00004052  00                                       3353+FLG56    DC    X'00'             expected FPC flags
00004053  00                                       3354+VXC56    DC    X'00'             expected VXC
00004054  0000410C                                 3355+V2_56    DC    A(RE56+16)        address of v2: 16-byte packed decimal
00004058  E5C3C6D5 40404040                        3356+         DC    CL8'VCFN'         instruction name
00004060  00000010                                 3357+         DC    A(16)             result length
00004064  000040FC                                 3358+         DC    A(RE56)           address of expected resul
00004068  00000000 00000000                        3359+         DS    FD                gap
00004070  00000000 00000000                        3360+V1O56    DS    XL16              V1 output
00004078  00000000 00000000
00004080  00000000 00000000                        3361+         DS    FD                   gap
00004088  00000000                                 3362+FPC_R_56 DS    F                 FPC after instruction
00004090  00000000 00000000                        3363+         DS    FD                   gap
00004098  40404040 40404040                        3364+         DC    CL8' '            was cross check skipped?
000040A0  00000000 00000000                        3365+         DS    FD                   gap
000040A8  00000000 00000000                        3366+XCO56    DS    XL16              Cross check Output
000040B0  00000000 00000000
000040B8  00000000 00000000                        3367+         DS    FD                   gap
000040C0  00000000                                 3368+FPC_XC_56 DS   F                 FPC after cross check
000040C8  00000000 00000000                        3369+         DS    FD                   gap
000040D0  00000000                                 3370+         DS    F                 debug area
000040D4  00000000                                 3371+         DS    F
                                                   3372+*
000040D8                                           3373+X56      DS    0F
000040D8  B29D 85A4                     000007A4   3374+         LFPC  FPCINIT           initialize FPC
                                                   3375+*         LFPC  =XL4'08000000'         set trap exception
000040DC  E320 500C 0014                00004054   3376+         LGF   R2,V2_56          get v2
000040E2  E762 0000 0806                00000000   3377+         VL    V22,0(R2)
000040E8  E666 0000 1C5D                           3378+         VCFN  V22,V22,1,0       test instruction (dest is source)
000040EE  B29C 5040                     00004088   3379+         STFPC FPC_R_56          save FPC
000040F2  E760 5028 080E                00004070   3380+         VST   V22,V1O56         save instruction result
000040F8  07FB                                     3381+         BR    R11               return
000040FC                                           3382+RE56     DS    0F                expected 16 byte result
000040FC                                           3383+         DROP  R5
000040FC  1ECA0000 9ECA0000                        3384          DC    XL16'1ECA00009ECA00000000000000000000'
00004104  00000000 00000000
0000410C  2F650000 AF650000                        3385          DC    XL16'2F650000AF650000000000000000000'
00004114  00000000 00000000
                                                   3386
                                                   3387 * +65536, -65536 (overflow)
                                                   3388          VRR_A VCFN,1,0,20,23,S
00004120                                           3389+         DS    0FD
00004120                        00004120           3390+         USING *,R5              base for test data and test routine
00004120  000041B0                                 3391+T57      DC    A(X57)            address of test routine
00004124  0039                                     3392+         DC    H'57'             test number
00004126  00                                       3393+         DC    X'00'
00004127  E2                                       3394+         DC    CL1'S'            Y = skip cross check
00004128  01                                       3395+         DC    HL1'1'            m3
00004129  00                                       3396+         DC    HL1'0'            m4
0000412A  20                                       3397+FLG57    DC    X'20'             expected FPC flags
0000412B  23                                       3398+VXC57    DC    X'23'             expected VXC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000412C  000041E4                                3399+V2_57    DC    A(RE57+16)        address of v2: 16-byte packed decimal
00004130  E5C3C6D5 40404040                       3400+         DC    CL8'VCFN'         instruction name
00004138  00000010                                3401+         DC    A(16)             result length
0000413C  000041D4                                3402+         DC    A(RE57)           address of expected resul
00004140  00000000 00000000                       3403+         DS    FD                gap
00004148  00000000 00000000                       3404+V1O57    DS    XL16              V1 output
00004150  00000000 00000000
00004158  00000000 00000000                       3405+         DS    FD                   gap
00004160  00000000                                3406+FPC_R_57 DS    F                 FPC after instruction
00004168  00000000 00000000                       3407+         DS    FD                   gap
00004170  40404040 40404040                       3408+         DC    CL8' '            was cross check skipped?
00004178  00000000 00000000                       3409+         DS    FD                   gap
00004180  00000000 00000000                       3410+XCO57    DS    XL16              Cross check Output
00004188  00000000 00000000
00004190  00000000 00000000                       3411+         DS    FD                   gap
00004198  00000000                                3412+FPC_XC_57 DS   F                 FPC after cross check
000041A0  00000000 00000000                       3413+         DS    FD                   gap
000041A8  00000000                                3414+         DS    F                 debug area
000041AC  00000000                                3415+         DS    F
                                                  3416+*
000041B0                                          3417+X57      DS    0F
000041B0  B29D 85A4                     000007A4  3418+         LFPC  FPCINIT           initialize FPC
                                                  3419+*         LFPC  =XL4'08000000'         set trap exception
000041B4  E320 500C 0014                0000412C  3420+         LGF   R2,V2_57          get v2
000041BA  E762 0000 0806                00000000  3421+         VL    V22,0(R2)
000041C0  E666 0000 1C5D                          3422+         VCFN  V22,V22,1,0       test instruction (dest is source)
000041C6  B29C 5040                     00004160  3423+         STFPC FPC_R_57          save FPC
000041CA  E760 5028 080E                00004148  3424+         VST   V22,V1O57         save instruction result
000041D0  07FB                                    3425+         BR    R11               return
000041D4                                          3426+RE57     DS    0F                expected 16 byte result
000041D4                                          3427+         DROP  R5
000041D4  7C000000 FC000000                       3428          DC    XL16'7C000000FC00000000000000000000'
000041DC  00000000 00000000
000041E4  5E000000 DE000000                       3429          DC    XL16'5E000000DE00000000000000000000'
000041EC  00000000 00000000
                                                  3430
                                                  3431 * +Normal, -Normal (2.5)
                                                  3432          VRR_A VCFN,1,0,00,00,N
000041F8                                          3433+         DS    0FD
000041F8                        000041F8          3434+         USING *,R5              base for test data and test routine
000041F8  00004288                                3435+T58      DC    A(X58)            address of test routine
000041FC  003A                                    3436+         DC    H'58'             test number
000041FE  00                                      3437+         DC    X'00'
000041FF  D5                                      3438+         DC    CL1'N'            Y = skip cross check
00004200  01                                      3439+         DC    HL1'1'            m3
00004201  00                                      3440+         DC    HL1'0'            m4
00004202  00                                      3441+FLG58    DC    X'00'             expected FPC flags
00004203  00                                      3442+VXC58    DC    X'00'             expected VXC
00004204  000042BC                                3443+V2_58    DC    A(RE58+16)        address of v2: 16-byte packed decimal
00004208  E5C3C6D5 40404040                       3444+         DC    CL8'VCFN'         instruction name
00004210  00000010                                3445+         DC    A(16)             result length
00004214  000042AC                                3446+         DC    A(RE58)           address of expected resul
00004218  00000000 00000000                       3447+         DS    FD                gap
00004220  00000000 00000000                       3448+V1O58    DS    XL16              V1 output
00004228  00000000 00000000
00004230  00000000 00000000                       3449+         DS    FD                   gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00004238  00000000                                3450+FPC_R_58 DS    F                 FPC after instruction
00004240  00000000 00000000                       3451+         DS    FD                   gap
00004248  40404040 40404040                       3452+         DC    CL8' '            was cross check skipped?
00004250  00000000 00000000                       3453+         DS    FD                   gap
00004258  00000000 00000000                       3454+XCO58    DS    XL16              Cross check Output
00004260  00000000 00000000
00004268  00000000 00000000                       3455+         DS    FD                   gap
00004270  00000000                                3456+FPC_XC_58 DS   F                 FPC after cross check
00004278  00000000 00000000                       3457+         DS    FD                   gap
00004280  00000000                                3458+         DS    F                 debug area
00004284  00000000                                3459+         DS    F
                                                  3460+*
00004288                                          3461+X58      DS    0F
00004288  B29D 85A4                    000007A4   3462+         LFPC  FPCINIT           initialize FPC
                                                  3463+*         LFPC  =XL4'08000000'         set trap exception
0000428C  E320 500C 0014               00004204   3464+         LGF   R2,V2_58          get v2
00004292  E762 0000 0806               00000000   3465+         VL    V22,0(R2)
00004298  E666 0000 1C5D                          3466+         VCFN  V22,V22,1,0       test instruction (dest is source)
0000429E  B29C 5040                    00004238   3467+         STFPC FPC_R_58          save FPC
000042A2  E760 5028 080E               00004220   3468+         VST   V22,V1O58         save instruction result
000042A8  07FB                                    3469+         BR    R11               return
000042AC                                          3470+RE58     DS    0F                expected 16 byte result
000042AC                                          3471+         DROP  R5
000042AC  41000000 C1000000                       3472          DC    XL16'41000000C1000000000000000000000'
000042B4  00000000 00000000
000042BC  40800000 C0800000                       3473          DC    XL16'40800000C0800000000000000000000'
000042C4  00000000 00000000
                                                  3474
                                                  3475 * +0.00006097, -0.00006097 (about)
                                                  3476          VRR_A VCFN,1,0,00,00,N
000042D0                                          3477+         DS    0FD
000042D0                       000042D0           3478+         USING *,R5              base for test data and test routine
000042D0  00004360                                3479+T59      DC    A(X59)            address of test routine
000042D4  003B                                    3480+         DC    H'59'             test number
000042D6  00                                      3481+         DC    X'00'
000042D7  D5                                      3482+         DC    CL1'N'            Y = skip cross check
000042D8  01                                      3483+         DC    HL1'1'            m3
000042D9  00                                      3484+         DC    HL1'0'            m4
000042DA  00                                      3485+FLG59    DC    X'00'             expected FPC flags
000042DB  00                                      3486+VXC59    DC    X'00'             expected VXC
000042DC  00004394                                3487+V2_59    DC    A(RE59+16)        address of v2: 16-byte packed decimal
000042E0  E5C3C6D5 40404040                       3488+         DC    CL8'VCFN'         instruction name
000042E8  00000010                                3489+         DC    A(16)             result length
000042EC  00004384                                3490+         DC    A(RE59)           address of expected resul
000042F0  00000000 00000000                       3491+         DS    FD                gap
000042F8  00000000 00000000                       3492+V1O59    DS    XL16              V1 output
00004300  00000000 00000000
00004308  00000000 00000000                       3493+         DS    FD                   gap
00004310  00000000                                3494+FPC_R_59 DS    F                 FPC after instruction
00004318  00000000 00000000                       3495+         DS    FD                   gap
00004320  40404040 40404040                       3496+         DC    CL8' '            was cross check skipped?
00004328  00000000 00000000                       3497+         DS    FD                   gap
00004330  00000000 00000000                       3498+XCO59    DS    XL16              Cross check Output
00004338  00000000 00000000
00004340  00000000 00000000                       3499+         DS    FD                   gap
00004348  00000000                                3500+FPC_XC_59 DS   F                 FPC after cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00004350  00000000 00000000                       3501+         DS    FD                   gap
00004358  00000000                                3502+         DS    F                  debug area
0000435C  00000000                                3503+         DS    F
                                                  3504+*
00004360                                          3505+X59      DS    0F
00004360  B29D 85A4                     000007A4  3506+         LFPC  FPCINIT            initialize FPC
                                                  3507+*         LFPC  =XL4'08000000'         set trap exception
00004364  E320 500C 0014                000042DC  3508+         LGF   R2,V2_59           get v2
0000436A  E762 0000 0806                00000000  3509+         VL    V22,0(R2)
00004370  E666 0000 1C5D                          3510+         VCFN  V22,V22,1,0        test instruction (dest is source)
00004376  B29C 5040                     00004310  3511+         STFPC FPC_R_59           save FPC
0000437A  E760 5028 080E                000042F8  3512+         VST   V22,V1O59          save instruction result
00004380  07FB                                    3513+         BR    R11                return
00004384                                          3514+RE59     DS    0F                 expected 16 byte result
00004384                                          3515+         DROP  R5
00004384  03FF0000 83FF0000                       3516          DC    XL16'03FF000083FF00000000000000000000'
0000438C  00000000 00000000
00004394  21FF0000 A1FF0000                       3517          DC    XL16'21FF0000A1FF00000000000000000000'
0000439C  00000000 00000000
                                                  3518
                                                  3519 * multiple exception types
                                                  3520 *  +Infinity, overflow
                                                  3521          VRR_A VCFN,1,0,A0,23,S                     skip xc - infinity
000043A8                                          3522+         DS    0FD
000043A8                        000043A8          3523+         USING *,R5               base for test data and test routine
000043A8  00004438                                3524+T60      DC    A(X60)             address of test routine
000043AC  003C                                    3525+         DC    H'60'              test number
000043AE  00                                      3526+         DC    X'00'
000043AF  E2                                      3527+         DC    CL1'S'             Y = skip cross check
000043B0  01                                      3528+         DC    HL1'1'             m3
000043B1  00                                      3529+         DC    HL1'0'             m4
000043B2  A0                                      3530+FLG60    DC    X'A0'              expected FPC flags
000043B3  23                                      3531+VXC60    DC    X'23'              expected VXC
000043B4  0000446C                                3532+V2_60    DC    A(RE60+16)         address of v2: 16-byte packed decimal
000043B8  E5C3C6D5 40404040                       3533+         DC    CL8'VCFN'          instruction name
000043C0  00000010                                3534+         DC    A(16)              result length
000043C4  0000445C                                3535+         DC    A(RE60)            address of expected resul
000043C8  00000000 00000000                       3536+         DS    FD                 gap
000043D0  00000000 00000000                       3537+V1O60    DS    XL16               V1 output
000043D8  00000000 00000000
000043E0  00000000 00000000                       3538+         DS    FD                   gap
000043E8  00000000                                3539+FPC_R_60 DS    F                  FPC after instruction
000043F0  00000000 00000000                       3540+         DS    FD                   gap
000043F8  40404040 40404040                       3541+         DC    CL8' '             was cross check skipped?
00004400  00000000 00000000                       3542+         DS    FD                   gap
00004408  00000000 00000000                       3543+XCO60    DS    XL16               Cross check Output
00004410  00000000 00000000
00004418  00000000 00000000                       3544+         DS    FD                   gap
00004420  00000000                                3545+FPC_XC_60 DS   F                  FPC after cross check
00004428  00000000 00000000                       3546+         DS    FD                   gap
00004430  00000000                                3547+         DS    F                  debug area
00004434  00000000                                3548+         DS    F
                                                  3549+*
00004438                                          3550+X60      DS    0F
00004438  B29D 85A4                     000007A4  3551+         LFPC  FPCINIT            initialize FPC
                                                  3552+*         LFPC  =XL4'08000000'         set trap exception
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000443C  E320 500C 0014                000043B4  3553+         LGF   R2,V2_60          get v2
00004442  E762 0000 0806                00000000  3554+         VL    V22,0(R2)
00004448  E666 0000 1C5D                          3555+         VCFN  V22,V22,1,0       test instruction (dest is source)
0000444E  B29C 5040                     000043E8  3556+         STFPC FPC_R_60          save FPC
00004452  E760 5028 080E                000043D0  3557+         VST   V22,V1O60         save instruction result
00004458  07FB                                    3558+         BR    R11               return
0000445C                                          3559+RE60     DS    0F                expected 16 byte result
0000445C                                          3560+         DROP  R5
0000445C  7E000000 7C000000                       3561          DC    XL16'7E0000007C00000000000000000000'
00004464  00000000 00000000
0000446C  7FFF0000 5E000000                       3562          DC    XL16'7FFF00005E00000000000000000000'
00004474  00000000 00000000
                                                  3563
                                                  3564 * Underflow,  -65536 (overflow)              skip xc - dropped digits
                                                  3565          VRR_A VCFN,1,0,30,23,S
00004480                                          3566+         DS    0FD
00004480                        00004480          3567+         USING *,R5              base for test data and test routine
00004480  00004510                                3568+T61      DC    A(X61)            address of test routine
00004484  003D                                    3569+         DC    H'61'             test number
00004486  00                                      3570+         DC    X'00'
00004487  E2                                      3571+         DC    CL1'S'            Y = skip cross check
00004488  01                                      3572+         DC    HL1'1'            m3
00004489  00                                      3573+         DC    HL1'0'            m4
0000448A  30                                      3574+FLG61    DC    X'30'             expected FPC flags
0000448B  23                                      3575+VXC61    DC    X'23'             expected VXC
0000448C  00004544                                3576+V2_61    DC    A(RE61+16)        address of v2: 16-byte packed decimal
00004490  E5C3C6D5 40404040                       3577+         DC    CL8'VCFN'         instruction name
00004498  00000010                                3578+         DC    A(16)             result length
0000449C  00004534                                3579+         DC    A(RE61)           address of expected resul
000044A0  00000000 00000000                       3580+         DS    FD                gap
000044A8  00000000 00000000                       3581+V1O61    DS    XL16              V1 output
000044B0  00000000 00000000
000044B8  00000000 00000000                       3582+         DS    FD                   gap
000044C0  00000000                                3583+FPC_R_61 DS    F                 FPC after instruction
000044C8  00000000 00000000                       3584+         DS    FD                   gap
000044D0  40404040 40404040                       3585+         DC    CL8' '            was cross check skipped?
000044D8  00000000 00000000                       3586+         DS    FD                   gap
000044E0  00000000 00000000                       3587+XCO61    DS    XL16              Cross check Output
000044E8  00000000 00000000
000044F0  00000000 00000000                       3588+         DS    FD                   gap
000044F8  00000000                                3589+FPC_XC_61 DS   F                 FPC after cross check
00004500  00000000 00000000                       3590+         DS    FD                   gap
00004508  00000000                                3591+         DS    F                 debug area
0000450C  00000000                                3592+         DS    F
                                                  3593+*
00004510                                          3594+X61      DS    0F
00004510  B29D 85A4                     000007A4  3595+         LFPC  FPCINIT           initialize FPC
                                                  3596+*         LFPC  =XL4'08000000'         set trap exception
00004514  E320 500C 0014                0000448C  3597+         LGF   R2,V2_61          get v2
0000451A  E762 0000 0806                00000000  3598+         VL    V22,0(R2)
00004520  E666 0000 1C5D                          3599+         VCFN  V22,V22,1,0       test instruction (dest is source)
00004526  B29C 5040                     000044C0  3600+         STFPC FPC_R_61          save FPC
0000452A  E760 5028 080E                000044A8  3601+         VST   V22,V1O61         save instruction result
00004530  07FB                                    3602+         BR    R11               return
00004534                                          3603+RE61     DS    0F                expected 16 byte result
00004534                                          3604+         DROP  R5
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004534  00000000 7C000000                        3605          DC    XL16'000000007C000000000000000000000'
0000453C  00000000 00000000
00004544  0A000000 5E000000                        3606          DC    XL16'0A0000005E000000000000000000000'
0000454C  00000000 00000000
                                                   3607
                                                   3608 * +Infinity, Underflow,  -65536 (overflow)          skip xc - infinity
                                                   3609          VRR_A VCFN,1,0,B0,43,S
00004558                                           3610+         DS    0FD
00004558                      00004558             3611+         USING *,R5              base for test data and test routine
00004558  000045E8                                 3612+T62      DC    A(X62)            address of test routine
0000455C  003E                                     3613+         DC    H'62'             test number
0000455E  00                                       3614+         DC    X'00'
0000455F  E2                                       3615+         DC    CL1'S'            Y = skip cross check
00004560  01                                       3616+         DC    HL1'1'            m3
00004561  00                                       3617+         DC    HL1'0'            m4
00004562  B0                                       3618+FLG62    DC    X'B0'             expected FPC flags
00004563  43                                       3619+VXC62    DC    X'43'             expected VXC
00004564  0000461C                                 3620+V2_62    DC    A(RE62+16)        address of v2: 16-byte packed decimal
00004568  E5C3C6D5 40404040                        3621+         DC    CL8'VCFN'         instruction name
00004570  00000010                                 3622+         DC    A(16)             result length
00004574  0000460C                                 3623+         DC    A(RE62)           address of expected resul
00004578  00000000 00000000                        3624+         DS    FD                gap
00004580  00000000 00000000                        3625+V1O62    DS    XL16              V1 output
00004588  00000000 00000000
00004590  00000000 00000000                        3626+         DS    FD                   gap
00004598  00000000                                 3627+FPC_R_62 DS    F                 FPC after instruction
000045A0  00000000 00000000                        3628+         DS    FD                   gap
000045A8  40404040 40404040                        3629+         DC    CL8' '            was cross check skipped?
000045B0  00000000 00000000                        3630+         DS    FD                   gap
000045B8  00000000 00000000                        3631+XCO62    DS    XL16              Cross check Output
000045C0  00000000 00000000
000045C8  00000000 00000000                        3632+         DS    FD                   gap
000045D0  00000000                                 3633+FPC_XC_62 DS   F                 FPC after cross check
000045D8  00000000 00000000                        3634+         DS    FD                   gap
000045E0  00000000                                 3635+         DS    F                 debug area
000045E4  00000000                                 3636+         DS    F
                                                   3637+*
000045E8                                           3638+X62      DS    0F
000045E8  B29D 85A4                    000007A4    3639+         LFPC  FPCINIT           initialize FPC
                                                   3640+*         LFPC  =XL4'08000000'         set trap exception
000045EC  E320 500C 0014               00004564    3641+         LGF   R2,V2_62          get v2
000045F2  E762 0000 0806               00000000    3642+         VL    V22,0(R2)
000045F8  E666 0000 1C5D                           3643+         VCFN  V22,V22,1,0       test instruction (dest is source)
000045FE  B29C 5040                    00004598    3644+         STFPC FPC_R_62          save FPC
00004602  E760 5028 080E               00004580    3645+         VST   V22,V1O62         save instruction result
00004608  07FB                                     3646+         BR    R11               return
0000460C                                           3647+RE62     DS    0F                expected 16 byte result
0000460C                                           3648+         DROP  R5
0000460C  7E000000 00000000                        3649          DC    XL16'7E000000000000007C00000000000000'
00004614  7C000000 00000000
0000461C  7FFF0000 0A000000                        3650          DC    XL16'7FFF00000A0000005E00000000000000'
00004624  5E000000 00000000
                                                   3651
                                                   3652 *-----------------------------------------------------------------------
                                                   3653 * VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                   3654 *-----------------------------------------------------------------------
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   3655 *  dlfloat -> short float (with cross check: short float -> dlfloat)
                                                   3656 *
                                                   3657
                                                   3658 * +0, -0     simple instruction and 'test' test
                                                   3659          VRR_A VCLFNL,2,0,00,00,N
00004630                                           3660+         DS    0FD
00004630                       00004630            3661+         USING *,R5              base for test data and test routine
00004630  000046C0                                 3662+T63      DC    A(X63)            address of test routine
00004634  003F                                     3663+         DC    H'63'             test number
00004636  00                                       3664+         DC    X'00'
00004637  D5                                       3665+         DC    CL1'N'            Y = skip cross check
00004638  02                                       3666+         DC    HL1'2'            m3
00004639  00                                       3667+         DC    HL1'0'            m4
0000463A  00                                       3668+FLG63    DC    X'00'             expected FPC flags
0000463B  00                                       3669+VXC63    DC    X'00'             expected VXC
0000463C  000046F4                                 3670+V2_63    DC    A(RE63+16)        address of v2: 16-byte packed decimal
00004640  E5C3D3C6 D5D34040                        3671+         DC    CL8'VCLFNL'       instruction name
00004648  00000010                                 3672+         DC    A(16)             result length
0000464C  000046E4                                 3673+         DC    A(RE63)           address of expected resul
00004650  00000000 00000000                        3674+         DS    FD                gap
00004658  00000000 00000000                        3675+V1O63    DS    XL16              V1 output
00004660  00000000 00000000
00004668  00000000 00000000                        3676+         DS    FD                   gap
00004670  00000000                                 3677+FPC_R_63 DS    F                 FPC after instruction
00004678  00000000 00000000                        3678+         DS    FD                   gap
00004680  40404040 40404040                        3679+         DC    CL8' '            was cross check skipped?
00004688  00000000 00000000                        3680+         DS    FD                   gap
00004690  00000000 00000000                        3681+XCO63    DS    XL16              Cross check Output
00004698  00000000 00000000
000046A0  00000000 00000000                        3682+         DS    FD                   gap
000046A8  00000000                                 3683+FPC_XC_63 DS   F                 FPC after cross check
000046B0  00000000 00000000                        3684+         DS    FD                   gap
000046B8  00000000                                 3685+         DS    F                 debug area
000046BC  00000000                                 3686+         DS    F
                                                   3687+*
000046C0                                           3688+X63      DS    0F
000046C0  B29D 85A4                     000007A4   3689+         LFPC  FPCINIT           initialize FPC
                                                   3690+*         LFPC  =XL4'08000000'         set trap exception
000046C4  E320 500C 0014                0000463C   3691+         LGF   R2,V2_63          get v2
000046CA  E762 0000 0806                00000000   3692+         VL    V22,0(R2)
000046D0  E666 0000 2C5E                           3693+         VCLFNL V22,V22,2,0      test instruction (dest is source)
000046D6  B29C 5040                     00004670   3694+         STFPC FPC_R_63          save FPC
000046DA  E760 5028 080E                00004658   3695+         VST   V22,V1O63         save instruction result
000046E0  07FB                                     3696+         BR    R11               return
000046E4                                           3697+RE63     DS    0F                expected 16 byte result
000046E4                                           3698+         DROP  R5
000046E4  00000000 80000000                        3699          DC    XL16'00000000800000000000000000000000'
000046EC  00000000 00000000
000046F4  00000000 00000000                        3700          DC    XL16'00000000000000000000800000000000'
000046FC  00008000 00000000
                                                   3701
                                                   3702 * +1, -1
                                                   3703          VRR_A VCLFNL,2,0,00,00,N
00004708                                           3704+         DS    0FD
00004708                       00004708            3705+         USING *,R5              base for test data and test routine
00004708  00004798                                 3706+T64      DC    A(X64)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000470C  0040                                     3707+          DC    H'64'              test number
0000470E  00                                       3708+          DC    X'00'
0000470F  D5                                       3709+          DC    CL1'N'             Y = skip cross check
00004710  02                                       3710+          DC    HL1'2'             m3
00004711  00                                       3711+          DC    HL1'0'             m4
00004712  00                                       3712+FLG64     DC    X'00'              expected FPC flags
00004713  00                                       3713+VXC64     DC    X'00'              expected VXC
00004714  000047CC                                 3714+V2_64     DC    A(RE64+16)         address of v2: 16-byte packed decimal
00004718  E5C3D3C6 D5D34040                        3715+          DC    CL8'VCLFNL'        instruction name
00004720  00000010                                 3716+          DC    A(16)              result length
00004724  000047BC                                 3717+          DC    A(RE64)            address of expected resul
00004728  00000000 00000000                        3718+          DS    FD                 gap
00004730  00000000 00000000                        3719+V1O64     DS    XL16               V1 output
00004738  00000000 00000000
00004740  00000000 00000000                        3720+          DS    FD                    gap
00004748  00000000                                 3721+FPC_R_64  DS    F                  FPC after instruction
00004750  00000000 00000000                        3722+          DS    FD                    gap
00004758  40404040 40404040                        3723+          DC    CL8' '             was cross check skipped?
00004760  00000000 00000000                        3724+          DS    FD                    gap
00004768  00000000 00000000                        3725+XCO64     DS    XL16               Cross check Output
00004770  00000000 00000000
00004778  00000000 00000000                        3726+          DS    FD                    gap
00004780  00000000                                 3727+FPC_XC_64 DS    F                  FPC after cross check
00004788  00000000 00000000                        3728+          DS    FD                    gap
00004790  00000000                                 3729+          DS    F                  debug area
00004794  00000000                                 3730+          DS    F
                                                   3731+*
00004798                                           3732+X64       DS    0F
00004798  B29D 85A4                     000007A4   3733+          LFPC  FPCINIT            initialize FPC
                                                   3734+*         LFPC  =XL4'08000000'          set trap exception
0000479C  E320 500C 0014                00004714   3735+          LGF   R2,V2_64           get v2
000047A2  E762 0000 0806                00000000   3736+          VL    V22,0(R2)
000047A8  E666 0000 2C5E                           3737+          VCLFNL V22,V22,2,0       test instruction (dest is source)
000047AE  B29C 5040                     00004748   3738+          STFPC FPC_R_64           save FPC
000047B2  E760 5028 080E                00004730   3739+          VST   V22,V1O64          save instruction result
000047B8  07FB                                     3740+          BR    R11                return
000047BC                                           3741+RE64      DS    0F                 expected 16 byte result
000047BC                                           3742+          DROP  R5
000047BC  3F800000 BF800000                        3743           DC    XL16'3F800000BF800000000000000000000'
000047C4  00000000 00000000
000047CC  00000000 00000000                        3744           DC    XL16'0000000000000000003E00BE0000000000'
000047D4  3E00BE00 00000000
                                                   3745
                                                   3746 * +0.5, -0.5
                                                   3747           VRR_A VCLFNL,2,0,00,00,N
000047E0                                           3748+          DS    0FD
000047E0                        000047E0           3749+          USING *,R5               base for test data and test routine
000047E0  00004870                                 3750+T65       DC    A(X65)             address of test routine
000047E4  0041                                     3751+          DC    H'65'              test number
000047E6  00                                       3752+          DC    X'00'
000047E7  D5                                       3753+          DC    CL1'N'             Y = skip cross check
000047E8  02                                       3754+          DC    HL1'2'             m3
000047E9  00                                       3755+          DC    HL1'0'             m4
000047EA  00                                       3756+FLG65     DC    X'00'              expected FPC flags
000047EB  00                                       3757+VXC65     DC    X'00'              expected VXC
000047EC  000048A4                                 3758+V2_65     DC    A(RE65+16)         address of v2: 16-byte packed decimal
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000047F0  E5C3D3C6 D5D34040                        3759+         DC    CL8'VCLFNL'       instruction name
000047F8  00000010                                 3760+         DC    A(16)             result length
000047FC  00004894                                 3761+         DC    A(RE65)           address of expected resul
00004800  00000000 00000000                        3762+         DS    FD                gap
00004808  00000000 00000000                        3763+V1O65    DS    XL16              V1 output
00004810  00000000 00000000
00004818  00000000 00000000                        3764+         DS    FD                   gap
00004820  00000000                                 3765+FPC_R_65 DS    F                 FPC after instruction
00004828  00000000 00000000                        3766+         DS    FD                   gap
00004830  40404040 40404040                        3767+         DC    CL8' '            was cross check skipped?
00004838  00000000 00000000                        3768+         DS    FD                   gap
00004840  00000000 00000000                        3769+XCO65    DS    XL16              Cross check Output
00004848  00000000 00000000
00004850  00000000 00000000                        3770+         DS    FD                   gap
00004858  00000000                                 3771+FPC_XC_65 DS   F                 FPC after cross check
00004860  00000000 00000000                        3772+         DS    FD                   gap
00004868  00000000                                 3773+         DS    F                 debug area
0000486C  00000000                                 3774+         DS    F
                                                   3775+*
00004870                                           3776+X65      DS    0F
00004870  B29D 85A4                     000007A4   3777+         LFPC  FPCINIT           initialize FPC
                                                   3778+*         LFPC  =XL4'08000000'         set trap exception
00004874  E320 500C 0014                000047EC   3779+         LGF   R2,V2_65          get v2
0000487A  E762 0000 0806                00000000   3780+         VL    V22,0(R2)
00004880  E666 0000 2C5E                           3781+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00004886  B29C 5040                     00004820   3782+         STFPC FPC_R_65          save FPC
0000488A  E760 5028 080E                00004808   3783+         VST   V22,V1O65         save instruction result
00004890  07FB                                     3784+         BR    R11               return
00004894                                           3785+RE65     DS    0F                expected 16 byte result
00004894                                           3786+         DROP  R5
00004894  3F000000 BF000000                        3787          DC    XL16'3F000000BF00000000000000000000'
0000489C  00000000 00000000
000048A4  00000000 00000000                        3788          DC    XL16'0000000000000000003C00BC0000000000'
000048AC  3C00BC00 00000000
                                                   3789
                                                   3790 * 1/64, -1/64
                                                   3791          VRR_A VCLFNL,2,0,00,00,N
000048B8                                           3792+         DS    0FD
000048B8                        000048B8           3793+         USING *,R5              base for test data and test routine
000048B8  00004948                                 3794+T66      DC    A(X66)            address of test routine
000048BC  0042                                     3795+         DC    H'66'             test number
000048BE  00                                       3796+         DC    X'00'
000048BF  D5                                       3797+         DC    CL1'N'            Y = skip cross check
000048C0  02                                       3798+         DC    HL1'2'            m3
000048C1  00                                       3799+         DC    HL1'0'            m4
000048C2  00                                       3800+FLG66    DC    X'00'             expected FPC flags
000048C3  00                                       3801+VXC66    DC    X'00'             expected VXC
000048C4  0000497C                                 3802+V2_66    DC    A(RE66+16)        address of v2: 16-byte packed decimal
000048C8  E5C3D3C6 D5D34040                        3803+         DC    CL8'VCLFNL'       instruction name
000048D0  00000010                                 3804+         DC    A(16)             result length
000048D4  0000496C                                 3805+         DC    A(RE66)           address of expected resul
000048D8  00000000 00000000                        3806+         DS    FD                gap
000048E0  00000000 00000000                        3807+V1O66    DS    XL16              V1 output
000048E8  00000000 00000000
000048F0  00000000 00000000                        3808+         DS    FD                   gap
000048F8  00000000                                 3809+FPC_R_66 DS    F                 FPC after instruction
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004900  00000000 00000000                        3810+          DS    FD                    gap
00004908  40404040 40404040                        3811+          DC    CL8' '             was cross check skipped?
00004910  00000000 00000000                        3812+          DS    FD                    gap
00004918  00000000 00000000                        3813+XCO66     DS    XL16               Cross check Output
00004920  00000000 00000000
00004928  00000000 00000000                        3814+          DS    FD                    gap
00004930  00000000                                 3815+FPC_XC_66 DS    F                  FPC after cross check
00004938  00000000 00000000                        3816+          DS    FD                    gap
00004940  00000000                                 3817+          DS    F                  debug area
00004944  00000000                                 3818+          DS    F
                                                   3819+*
00004948                                           3820+X66       DS    0F
00004948  B29D 85A4                     000007A4   3821+          LFPC  FPCINIT            initialize FPC
                                                   3822+*          LFPC  =XL4'08000000'          set trap exception
0000494C  E320 500C 0014                000048C4   3823+          LGF   R2,V2_66           get v2
00004952  E762 0000 0806                00000000   3824+          VL    V22,0(R2)
00004958  E666 0000 2C5E                           3825+          VCLFNL V22,V22,2,0       test instruction (dest is source)
0000495E  B29C 5040                     000048F8   3826+          STFPC FPC_R_66           save FPC
00004962  E760 5028 080E                000048E0   3827+          VST   V22,V1O66          save instruction result
00004968  07FB                                     3828+          BR    R11                return
0000496C                                           3829+RE66      DS    0F                 expected 16 byte result
0000496C                                           3830+          DROP  R5
0000496C  3C800000 BC800000                        3831           DC    XL16'3C800000BC80000000000000000000'
00004974  00000000 00000000
0000497C  00000000 00000000                        3832           DC    XL16'00000000000000003200B20000000000'
00004984  3200B200 00000000
                                                   3833
                                                   3834 * +15, -15
                                                   3835           VRR_A VCLFNL,2,0,00,00,N
00004990                                           3836+          DS    0FD
00004990                        00004990           3837+          USING *,R5               base for test data and test routine
00004990  00004A20                                 3838+T67       DC    A(X67)             address of test routine
00004994  0043                                     3839+          DC    H'67'              test number
00004996  00                                       3840+          DC    X'00'
00004997  D5                                       3841+          DC    CL1'N'             Y = skip cross check
00004998  02                                       3842+          DC    HL1'2'             m3
00004999  00                                       3843+          DC    HL1'0'             m4
0000499A  00                                       3844+FLG67     DC    X'00'              expected FPC flags
0000499B  00                                       3845+VXC67     DC    X'00'              expected VXC
0000499C  00004A54                                 3846+V2_67     DC    A(RE67+16)         address of v2: 16-byte packed decimal
000049A0  E5C3D3C6 D5D34040                        3847+          DC    CL8'VCLFNL'        instruction name
000049A8  00000010                                 3848+          DC    A(16)              result length
000049AC  00004A44                                 3849+          DC    A(RE67)            address of expected resul
000049B0  00000000 00000000                        3850+          DS    FD                 gap
000049B8  00000000 00000000                        3851+V1O67     DS    XL16               V1 output
000049C0  00000000 00000000
000049C8  00000000 00000000                        3852+          DS    FD                    gap
000049D0  00000000                                 3853+FPC_R_67  DS    F                  FPC after instruction
000049D8  00000000 00000000                        3854+          DS    FD                    gap
000049E0  40404040 40404040                        3855+          DC    CL8' '             was cross check skipped?
000049E8  00000000 00000000                        3856+          DS    FD                    gap
000049F0  00000000 00000000                        3857+XCO67     DS    XL16               Cross check Output
000049F8  00000000 00000000
00004A00  00000000 00000000                        3858+          DS    FD                    gap
00004A08  00000000                                 3859+FPC_XC_67 DS    F                  FPC after cross check
00004A10  00000000 00000000                        3860+          DS    FD                    gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00004A18  00000000                                3861+         DS    F                 debug area
00004A1C  00000000                                3862+         DS    F
                                                  3863+*
00004A20                                          3864+X67      DS    0F
00004A20  B29D 85A4                     000007A4  3865+         LFPC  FPCINIT           initialize FPC
                                                  3866+*         LFPC  =XL4'08000000'         set trap exception
00004A24  E320 500C 0014                0000499C  3867+         LGF   R2,V2_67          get v2
00004A2A  E762 0000 0806                00000000  3868+         VL    V22,0(R2)
00004A30  E666 0000 2C5E                          3869+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00004A36  B29C 5040                     000049D0  3870+         STFPC FPC_R_67          save FPC
00004A3A  E760 5028 080E                000049B8  3871+         VST   V22,V1O67         save instruction result
00004A40  07FB                                    3872+         BR    R11               return
00004A44                                          3873+RE67     DS    0F                expected 16 byte result
00004A44                                          3874+         DROP  R5
00004A44  41700000 C1700000                       3875          DC    XL16'41700000C17000000000000000000000'
00004A4C  00000000 00000000
00004A54  00000000 00000000                       3876          DC    XL16'00000000000000045C0C5C000000000'
00004A5C  45C0C5C0 00000000
                                                  3877
                                                  3878 * +20/7, -20/7 (about)
                                                  3879          VRR_A VCLFNL,2,0,00,00,N
00004A68                                          3880+         DS    0FD
00004A68                        00004A68          3881+         USING *,R5              base for test data and test routine
00004A68  00004AF8                                3882+T68      DC    A(X68)            address of test routine
00004A6C  0044                                    3883+         DC    H'68'             test number
00004A6E  00                                      3884+         DC    X'00'
00004A6F  D5                                      3885+         DC    CL1'N'            Y = skip cross check
00004A70  02                                      3886+         DC    HL1'2'            m3
00004A71  00                                      3887+         DC    HL1'0'            m4
00004A72  00                                      3888+FLG68    DC    X'00'             expected FPC flags
00004A73  00                                      3889+VXC68    DC    X'00'             expected VXC
00004A74  00004B2C                                3890+V2_68    DC    A(RE68+16)        address of v2: 16-byte packed decimal
00004A78  E5C3D3C6 D5D34040                       3891+         DC    CL8'VCLFNL'       instruction name
00004A80  00000010                                3892+         DC    A(16)             result length
00004A84  00004B1C                                3893+         DC    A(RE68)           address of expected resul
00004A88  00000000 00000000                       3894+         DS    FD                gap
00004A90  00000000 00000000                       3895+V1O68    DS    XL16              V1 output
00004A98  00000000 00000000
00004AA0  00000000 00000000                       3896+         DS    FD                   gap
00004AA8  00000000                                3897+FPC_R_68 DS    F                 FPC after instruction
00004AB0  00000000 00000000                       3898+         DS    FD                   gap
00004AB8  40404040 40404040                       3899+         DC    CL8' '            was cross check skipped?
00004AC0  00000000 00000000                       3900+         DS    FD                   gap
00004AC8  00000000 00000000                       3901+XCO68    DS    XL16              Cross check Output
00004AD0  00000000 00000000
00004AD8  00000000 00000000                       3902+         DS    FD                   gap
00004AE0  00000000                                3903+FPC_XC_68 DS   F                 FPC after cross check
00004AE8  00000000 00000000                       3904+         DS    FD                   gap
00004AF0  00000000                                3905+         DS    F                 debug area
00004AF4  00000000                                3906+         DS    F
                                                  3907+*
00004AF8                                          3908+X68      DS    0F
00004AF8  B29D 85A4                     000007A4  3909+         LFPC  FPCINIT           initialize FPC
                                                  3910+*         LFPC  =XL4'08000000'         set trap exception
00004AFC  E320 500C 0014                00004A74  3911+         LGF   R2,V2_68          get v2
00004B02  E762 0000 0806                00000000  3912+         VL    V22,0(R2)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00004B08  E666 0000 2C5E                          3913+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00004B0E  B29C 5040                     00004AA8  3914+         STFPC FPC_R_68          save FPC
00004B12  E760 5028 080E                00004A90  3915+         VST   V22,V1O68         save instruction result
00004B18  07FB                                    3916+         BR    R11               return
00004B1C                                          3917+RE68     DS    0F                expected 16 byte result
00004B1C                                          3918+         DROP  R5
00004B1C  4036C000 C036C000                       3919          DC    XL16'4036C000C036C000000000000000000'
00004B24  00000000 00000000
00004B2C  00000000 00000000                       3920          DC    XL16'00000000000000040DBC0DB00000000'
00004B34  40DBC0DB 00000000
                                                  3921
                                                  3922 * additional tests
                                                  3923 * max  tiny:  (1 - 2^-11) * 2^16 (65504)
                                                  3924          VRR_A VCLFNL,2,0,00,00,N
00004B40                                          3925+         DS    0FD
00004B40                        00004B40          3926+         USING *,R5              base for test data and test routine
00004B40  00004BD0                                3927+T69      DC    A(X69)            address of test routine
00004B44  0045                                    3928+         DC    H'69'             test number
00004B46  00                                      3929+         DC    X'00'
00004B47  D5                                      3930+         DC    CL1'N'            Y = skip cross check
00004B48  02                                      3931+         DC    HL1'2'            m3
00004B49  00                                      3932+         DC    HL1'0'            m4
00004B4A  00                                      3933+FLG69    DC    X'00'             expected FPC flags
00004B4B  00                                      3934+VXC69    DC    X'00'             expected VXC
00004B4C  00004C04                                3935+V2_69    DC    A(RE69+16)        address of v2: 16-byte packed decimal
00004B50  E5C3D3C6 D5D34040                       3936+         DC    CL8'VCLFNL'       instruction name
00004B58  00000010                                3937+         DC    A(16)             result length
00004B5C  00004BF4                                3938+         DC    A(RE69)           address of expected resul
00004B60  00000000 00000000                       3939+         DS    FD                gap
00004B68  00000000 00000000                       3940+V1O69    DS    XL16              V1 output
00004B70  00000000 00000000
00004B78  00000000 00000000                       3941+         DS    FD                   gap
00004B80  00000000                                3942+FPC_R_69 DS    F                 FPC after instruction
00004B88  00000000 00000000                       3943+         DS    FD                   gap
00004B90  40404040 40404040                       3944+         DC    CL8' '            was cross check skipped?
00004B98  00000000 00000000                       3945+         DS    FD                   gap
00004BA0  00000000 00000000                       3946+XCO69    DS    XL16              Cross check Output
00004BA8  00000000 00000000
00004BB0  00000000 00000000                       3947+         DS    FD                   gap
00004BB8  00000000                                3948+FPC_XC_69 DS   F                 FPC after cross check
00004BC0  00000000 00000000                       3949+         DS    FD                   gap
00004BC8  00000000                                3950+         DS    F                 debug area
00004BCC  00000000                                3951+         DS    F
                                                  3952+*
00004BD0                                          3953+X69      DS    0F
00004BD0  B29D 85A4                     000007A4  3954+         LFPC  FPCINIT           initialize FPC
                                                  3955+*         LFPC  =XL4'08000000'          set trap exception
00004BD4  E320 500C 0014                00004B4C  3956+         LGF   R2,V2_69          get v2
00004BDA  E762 0000 0806                00000000  3957+         VL    V22,0(R2)
00004BE0  E666 0000 2C5E                          3958+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00004BE6  B29C 5040                     00004B80  3959+         STFPC FPC_R_69          save FPC
00004BEA  E760 5028 080E                00004B68  3960+         VST   V22,V1O69         save instruction result
00004BF0  07FB                                    3961+         BR    R11               return
00004BF4                                          3962+RE69     DS    0F                expected 16 byte result
00004BF4                                          3963+         DROP  R5
00004BF4  47800000 00000000                       3964          DC    XL16'47800000000000000000000000000000'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004BFC  00000000 00000000
00004C04  00000000 00000000                         3965          DC    XL16'00000000000000005E00000000000000'
00004C0C  5E000000 00000000
                                                    3966
                                                    3967 * max  dlfloat:  2^(33)-2ulp
                                                    3968          VRR_A VCLFNL,2,0,00,00,N
00004C18                                            3969+         DS    0FD
00004C18                       00004C18             3970+         USING *,R5              base for test data and test routine
00004C18  00004CA8                                  3971+T70      DC    A(X70)            address of test routine
00004C1C  0046                                      3972+         DC    H'70'             test number
00004C1E  00                                        3973+         DC    X'00'
00004C1F  D5                                        3974+         DC    CL1'N'            Y = skip cross check
00004C20  02                                        3975+         DC    HL1'2'            m3
00004C21  00                                        3976+         DC    HL1'0'            m4
00004C22  00                                        3977+FLG70    DC    X'00'             expected FPC flags
00004C23  00                                        3978+VXC70    DC    X'00'             expected VXC
00004C24  00004CDC                                  3979+V2_70    DC    A(RE70+16)        address of v2: 16-byte packed decimal
00004C28  E5C3D3C6 D5D34040                         3980+         DC    CL8'VCLFNL'       instruction name
00004C30  00000010                                  3981+         DC    A(16)             result length
00004C34  00004CCC                                  3982+         DC    A(RE70)           address of expected resul
00004C38  00000000 00000000                         3983+         DS    FD                gap
00004C40  00000000 00000000                         3984+V1O70    DS    XL16              V1 output
00004C48  00000000 00000000
00004C50  00000000 00000000                         3985+         DS    FD                   gap
00004C58  00000000                                  3986+FPC_R_70 DS    F                 FPC after instruction
00004C60  00000000 00000000                         3987+         DS    FD                   gap
00004C68  40404040 40404040                         3988+         DC    CL8' '            was cross check skipped?
00004C70  00000000 00000000                         3989+         DS    FD                   gap
00004C78  00000000 00000000                         3990+XCO70    DS    XL16              Cross check Output
00004C80  00000000 00000000
00004C88  00000000 00000000                         3991+         DS    FD                   gap
00004C90  00000000                                  3992+FPC_XC_70 DS   F                 FPC after cross check
00004C98  00000000 00000000                         3993+         DS    FD                   gap
00004CA0  00000000                                  3994+         DS    F                 debug area
00004CA4  00000000                                  3995+         DS    F
                                                    3996+*
00004CA8                                            3997+X70      DS    0F
00004CA8  B29D 85A4                     000007A4    3998+         LFPC  FPCINIT           initialize FPC
                                                    3999+*         LFPC  =XL4'08000000'         set trap exception
00004CAC  E320 500C 0014                00004C24    4000+         LGF   R2,V2_70          get v2
00004CB2  E762 0000 0806                00000000    4001+         VL    V22,0(R2)
00004CB8  E666 0000 2C5E                            4002+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00004CBE  B29C 5040                     00004C58    4003+         STFPC FPC_R_70          save FPC
00004CC2  E760 5028 080E                00004C40    4004+         VST   V22,V1O70         save instruction result
00004CC8  07FB                                      4005+         BR    R11               return
00004CCC                                            4006+RE70     DS    0F                expected 16 byte result
00004CCC                                            4007+         DROP  R5
00004CCC  4FFF8000 00000000                         4008          DC    XL16'4FFF800000000000000000000000000'
00004CD4  00000000 00000000
00004CDC  00000000 00000000                         4009          DC    XL16'0000000000000007FFE000000000000'
00004CE4  7FFE0000 00000000
                                                    4010
                                                    4011 * min  dlfloat: 2^(-31)*+ulp
                                                    4012          VRR_A VCLFNL,2,0,00,00,N
00004CF0                                            4013+         DS    0FD
00004CF0                       00004CF0             4014+         USING *,R5              base for test data and test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004CF0  00004D80                                 4015+T71      DC    A(X71)            address of test routine
00004CF4  0047                                     4016+         DC    H'71'             test number
00004CF6  00                                       4017+         DC    X'00'
00004CF7  D5                                       4018+         DC    CL1'N'            Y = skip cross check
00004CF8  02                                       4019+         DC    HL1'2'            m3
00004CF9  00                                       4020+         DC    HL1'0'            m4
00004CFA  00                                       4021+FLG71    DC    X'00'             expected FPC flags
00004CFB  00                                       4022+VXC71    DC    X'00'             expected VXC
00004CFC  00004DB4                                 4023+V2_71    DC    A(RE71+16)        address of v2: 16-byte packed decimal
00004D00  E5C3D3C6 D5D34040                        4024+         DC    CL8'VCLFNL'       instruction name
00004D08  00000010                                 4025+         DC    A(16)             result length
00004D0C  00004DA4                                 4026+         DC    A(RE71)           address of expected resul
00004D10  00000000 00000000                        4027+         DS    FD                gap
00004D18  00000000 00000000                        4028+V1O71    DS    XL16              V1 output
00004D20  00000000 00000000
00004D28  00000000 00000000                        4029+         DS    FD                   gap
00004D30  00000000                                 4030+FPC_R_71 DS    F                 FPC after instruction
00004D38  00000000 00000000                        4031+         DS    FD                   gap
00004D40  40404040 40404040                        4032+         DC    CL8' '            was cross check skipped?
00004D48  00000000 00000000                        4033+         DS    FD                   gap
00004D50  00000000 00000000                        4034+XCO71    DS    XL16              Cross check Output
00004D58  00000000 00000000
00004D60  00000000 00000000                        4035+         DS    FD                   gap
00004D68  00000000                                 4036+FPC_XC_71 DS   F                 FPC after cross check
00004D70  00000000 00000000                        4037+         DS    FD                   gap
00004D78  00000000                                 4038+         DS    F                 debug area
00004D7C  00000000                                 4039+         DS    F
                                                   4040+*
00004D80                                           4041+X71      DS    0F
00004D80  B29D 85A4                     000007A4   4042+         LFPC  FPCINIT           initialize FPC
                                                   4043+*         LFPC  =XL4'08000000'          set trap exception
00004D84  E320 500C 0014                00004CFC   4044+         LGF   R2,V2_71          get v2
00004D8A  E762 0000 0806                00000000   4045+         VL    V22,0(R2)
00004D90  E666 0000 2C5E                           4046+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00004D96  B29C 5040                     00004D30   4047+         STFPC FPC_R_71          save FPC
00004D9A  E760 5028 080E                00004D18   4048+         VST   V22,V1O71         save instruction result
00004DA0  07FB                                     4049+         BR    R11               return
00004DA4                                           4050+RE71     DS    0F                expected 16 byte result
00004DA4                                           4051+         DROP  R5
00004DA4  30004000 00000000                        4052          DC    XL16'30004000000000000000000000000000'
00004DAC  00000000 00000000
00004DB4  00000000 00000000                        4053          DC    XL16'00000000000000000001000000000000'
00004DBC  00010000 00000000
                                                   4054
                                                   4055 * +Infinity, -Infinity
                                                   4056          VRR_A VCLFNL,2,0,80,61,S          skip xcheck - includes NAN
00004DC8                                           4057+         DS    0FD
00004DC8                        00004DC8           4058+         USING *,R5              base for test data and test routine
00004DC8  00004E58                                 4059+T72      DC    A(X72)            address of test routine
00004DCC  0048                                     4060+         DC    H'72'             test number
00004DCE  00                                       4061+         DC    X'00'
00004DCF  E2                                       4062+         DC    CL1'S'            Y = skip cross check
00004DD0  02                                       4063+         DC    HL1'2'            m3
00004DD1  00                                       4064+         DC    HL1'0'            m4
00004DD2  80                                       4065+FLG72    DC    X'80'             expected FPC flags
00004DD3  61                                       4066+VXC72    DC    X'61'             expected VXC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004DD4  00004E8C                                 4067+V2_72    DC    A(RE72+16)        address of v2: 16-byte packed decimal
00004DD8  E5C3D3C6 D5D34040                        4068+         DC    CL8'VCLFNL'       instruction name
00004DE0  00000010                                 4069+         DC    A(16)             result length
00004DE4  00004E7C                                 4070+         DC    A(RE72)           address of expected resul
00004DE8  00000000 00000000                        4071+         DS    FD                gap
00004DF0  00000000 00000000                        4072+V1O72    DS    XL16              V1 output
00004DF8  00000000 00000000
00004E00  00000000 00000000                        4073+         DS    FD                   gap
00004E08  00000000                                 4074+FPC_R_72 DS    F                 FPC after instruction
00004E10  00000000 00000000                        4075+         DS    FD                   gap
00004E18  40404040 40404040                        4076+         DC    CL8' '            was cross check skipped?
00004E20  00000000 00000000                        4077+         DS    FD                   gap
00004E28  00000000 00000000                        4078+XCO72    DS    XL16              Cross check Output
00004E30  00000000 00000000
00004E38  00000000 00000000                        4079+         DS    FD                   gap
00004E40  00000000                                 4080+FPC_XC_72 DS   F                 FPC after cross check
00004E48  00000000 00000000                        4081+         DS    FD                   gap
00004E50  00000000                                 4082+         DS    F                 debug area
00004E54  00000000                                 4083+         DS    F
                                                   4084+*
00004E58                                           4085+X72      DS    0F
00004E58  B29D 85A4                     000007A4   4086+         LFPC  FPCINIT           initialize FPC
                                                   4087+*         LFPC  =XL4'08000000'         set trap exception
00004E5C  E320 500C 0014                00004DD4   4088+         LGF   R2,V2_72          get v2
00004E62  E762 0000 0806                00000000   4089+         VL    V22,0(R2)
00004E68  E666 0000 2C5E                           4090+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00004E6E  B29C 5040                     00004E08   4091+         STFPC FPC_R_72          save FPC
00004E72  E760 5028 080E                00004DF0   4092+         VST   V22,V1O72         save instruction result
00004E78  07FB                                     4093+         BR    R11               return
00004E7C                                           4094+RE72     DS    0F                expected 16 byte result
00004E7C                                           4095+         DROP  R5
00004E7C  7FC00000 00000000                        4096          DC    XL16'7FC0000000000000FFC0000000000000'
00004E84  FFC00000 00000000
00004E8C  00000000 00000000                        4097          DC    XL16'00000000000000007FFF0000FFFF0000'
00004E94  7FFF0000 FFFF0000
                                                   4098
                                                   4099 * inexact - bad m3
                                                   4100          VRR_A VCLFNL,5,0,08,05,S                    skip xc - inexact
00004EA0                                           4101+         DS    0FD
00004EA0                        00004EA0           4102+         USING *,R5              base for test data and test routine
00004EA0  00004F30                                 4103+T73      DC    A(X73)            address of test routine
00004EA4  0049                                     4104+         DC    H'73'             test number
00004EA6  00                                       4105+         DC    X'00'
00004EA7  E2                                       4106+         DC    CL1'S'            Y = skip cross check
00004EA8  05                                       4107+         DC    HL1'5'            m3
00004EA9  00                                       4108+         DC    HL1'0'            m4
00004EAA  08                                       4109+FLG73    DC    X'08'             expected FPC flags
00004EAB  05                                       4110+VXC73    DC    X'05'             expected VXC
00004EAC  00004F64                                 4111+V2_73    DC    A(RE73+16)        address of v2: 16-byte packed decimal
00004EB0  E5C3D3C6 D5D34040                        4112+         DC    CL8'VCLFNL'       instruction name
00004EB8  00000010                                 4113+         DC    A(16)             result length
00004EBC  00004F54                                 4114+         DC    A(RE73)           address of expected resul
00004EC0  00000000 00000000                        4115+         DS    FD                gap
00004EC8  00000000 00000000                        4116+V1O73    DS    XL16              V1 output
00004ED0  00000000 00000000
00004ED8  00000000 00000000                        4117+         DS    FD                   gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00004EE0  00000000                                4118+FPC_R_73 DS    F                 FPC after instruction
00004EE8  00000000 00000000                       4119+         DS    FD                   gap
00004EF0  40404040 40404040                       4120+         DC    CL8' '            was cross check skipped?
00004EF8  00000000 00000000                       4121+         DS    FD                   gap
00004F00  00000000 00000000                       4122+XCO73    DS    XL16              Cross check Output
00004F08  00000000 00000000
00004F10  00000000 00000000                       4123+         DS    FD                   gap
00004F18  00000000                                4124+FPC_XC_73 DS   F                 FPC after cross check
00004F20  00000000 00000000                       4125+         DS    FD                   gap
00004F28  00000000                                4126+         DS    F                 debug area
00004F2C  00000000                                4127+         DS    F
                                                  4128+*
00004F30                                          4129+X73      DS    0F
00004F30  B29D 85A4                    000007A4   4130+         LFPC  FPCINIT           initialize FPC
                                                  4131+*         LFPC  =XL4'08000000'         set trap exception
00004F34  E320 500C 0014               00004EAC   4132+         LGF   R2,V2_73          get v2
00004F3A  E762 0000 0806               00000000   4133+         VL    V22,0(R2)
00004F40  E666 0000 5C5E                          4134+         VCLFNL V22,V22,5,0      test instruction (dest is source)
00004F46  B29C 5040                    00004EE0   4135+         STFPC FPC_R_73          save FPC
00004F4A  E760 5028 080E               00004EC8   4136+         VST   V22,V1O73         save instruction result
00004F50  07FB                                    4137+         BR    R11               return
00004F54                                          4138+RE73     DS    0F                expected 16 byte result
00004F54                                          4139+         DROP  R5
00004F54  00000000 00000000                       4140          DC    XL16'00000000000000000000000000000000'
00004F5C  00000000 00000000
00004F64  00000000 0000F000                       4141          DC    XL16'000000000000F0000001000000000000'
00004F6C  00010000 00000000
                                                  4142
                                                  4143 * inexact - bad m4
                                                  4144          VRR_A VCLFNL,2,5,08,05,S                    skip xc - inexact
00004F78                                          4145+         DS    0FD
00004F78                       00004F78           4146+         USING *,R5              base for test data and test routine
00004F78  00005008                                4147+T74      DC    A(X74)            address of test routine
00004F7C  004A                                    4148+         DC    H'74'             test number
00004F7E  00                                      4149+         DC    X'00'
00004F7F  E2                                      4150+         DC    CL1'S'            Y = skip cross check
00004F80  02                                      4151+         DC    HL1'2'            m3
00004F81  05                                      4152+         DC    HL1'5'            m4
00004F82  08                                      4153+FLG74    DC    X'08'             expected FPC flags
00004F83  05                                      4154+VXC74    DC    X'05'             expected VXC
00004F84  0000503C                                4155+V2_74    DC    A(RE74+16)        address of v2: 16-byte packed decimal
00004F88  E5C3D3C6 D5D34040                       4156+         DC    CL8'VCLFNL'       instruction name
00004F90  00000010                                4157+         DC    A(16)             result length
00004F94  0000502C                                4158+         DC    A(RE74)           address of expected resul
00004F98  00000000 00000000                       4159+         DS    FD                gap
00004FA0  00000000 00000000                       4160+V1O74    DS    XL16              V1 output
00004FA8  00000000 00000000
00004FB0  00000000 00000000                       4161+         DS    FD                   gap
00004FB8  00000000                                4162+FPC_R_74 DS    F                 FPC after instruction
00004FC0  00000000 00000000                       4163+         DS    FD                   gap
00004FC8  40404040 40404040                       4164+         DC    CL8' '            was cross check skipped?
00004FD0  00000000 00000000                       4165+         DS    FD                   gap
00004FD8  00000000 00000000                       4166+XCO74    DS    XL16              Cross check Output
00004FE0  00000000 00000000
00004FE8  00000000 00000000                       4167+         DS    FD                   gap
00004FF0  00000000                                4168+FPC_XC_74 DS   F                 FPC after cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00004FF8  00000000 00000000                       4169+         DS    FD                   gap
00005000  00000000                                4170+         DS    F                 debug area
00005004  00000000                                4171+         DS    F
                                                  4172+*
00005008                                          4173+X74      DS    0F
00005008  B29D 85A4                     000007A4  4174+         LFPC  FPCINIT           initialize FPC
                                                  4175+*         LFPC  =XL4'08000000'         set trap exception
0000500C  E320 500C 0014                00004F84  4176+         LGF   R2,V2_74          get v2
00005012  E762 0000 0806                00000000  4177+         VL    V22,0(R2)
00005018  E666 0005 2C5E                          4178+         VCLFNL V22,V22,2,5      test instruction (dest is source)
0000501E  B29C 5040                     00004FB8  4179+         STFPC FPC_R_74          save FPC
00005022  E760 5028 080E                00004FA0  4180+         VST   V22,V1O74         save instruction result
00005028  07FB                                    4181+         BR    R11               return
0000502C                                          4182+RE74     DS    0F                expected 16 byte result
0000502C                                          4183+         DROP  R5
0000502C  00000000 00000000                       4184          DC    XL16'00000000000000000000000000000000'
00005034  00000000 00000000
0000503C  00000000 0000F000                       4185          DC    XL16'000000000000F000000100000000000'
00005044  00010000 00000000
                                                  4186
                                                  4187 * more tests
                                                  4188 * +3.140625, -3.140625
                                                  4189          VRR_A VCLFNL,2,0,00,00,N
00005050                                          4190+         DS    0FD
00005050                        00005050          4191+         USING *,R5              base for test data and test routine
00005050  000050E0                                4192+T75      DC    A(X75)            address of test routine
00005054  004B                                    4193+         DC    H'75'             test number
00005056  00                                      4194+         DC    X'00'
00005057  D5                                      4195+         DC    CL1'N'            Y = skip cross check
00005058  02                                      4196+         DC    HL1'2'            m3
00005059  00                                      4197+         DC    HL1'0'            m4
0000505A  00                                      4198+FLG75    DC    X'00'             expected FPC flags
0000505B  00                                      4199+VXC75    DC    X'00'             expected VXC
0000505C  00005114                                4200+V2_75    DC    A(RE75+16)        address of v2: 16-byte packed decimal
00005060  E5C3D3C6 D5D34040                       4201+         DC    CL8'VCLFNL'       instruction name
00005068  00000010                                4202+         DC    A(16)             result length
0000506C  00005104                                4203+         DC    A(RE75)           address of expected resul
00005070  00000000 00000000                       4204+         DS    FD                gap
00005078  00000000 00000000                       4205+V1O75    DS    XL16              V1 output
00005080  00000000 00000000
00005088  00000000 00000000                       4206+         DS    FD                   gap
00005090  00000000                                4207+FPC_R_75 DS    F                 FPC after instruction
00005098  00000000 00000000                       4208+         DS    FD                   gap
000050A0  40404040 40404040                       4209+         DC    CL8' '            was cross check skipped?
000050A8  00000000 00000000                       4210+         DS    FD                   gap
000050B0  00000000 00000000                       4211+XCO75    DS    XL16              Cross check Output
000050B8  00000000 00000000
000050C0  00000000 00000000                       4212+         DS    FD                   gap
000050C8  00000000                                4213+FPC_XC_75 DS   F                 FPC after cross check
000050D0  00000000 00000000                       4214+         DS    FD                   gap
000050D8  00000000                                4215+         DS    F                 debug area
000050DC  00000000                                4216+         DS    F
                                                  4217+*
000050E0                                          4218+X75      DS    0F
000050E0  B29D 85A4                     000007A4  4219+         LFPC  FPCINIT           initialize FPC
                                                  4220+*         LFPC  =XL4'08000000'         set trap exception
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000050E4  E320 500C 0014                0000505C  4221+         LGF   R2,V2_75          get v2
000050EA  E762 0000 0806                00000000  4222+         VL    V22,0(R2)
000050F0  E666 0000 2C5E                          4223+         VCLFNL V22,V22,2,0      test instruction (dest is source)
000050F6  B29C 5040                     00005090  4224+         STFPC FPC_R_75          save FPC
000050FA  E760 5028 080E                00005078  4225+         VST   V22,V1O75         save instruction result
00005100  07FB                                    4226+         BR    R11               return
00005104                                          4227+RE75     DS    0F                expected 16 byte result
00005104                                          4228+         DROP  R5
00005104  40890000 00000000                       4229          DC    XL16'4089000000000000C089000000000000'
0000510C  C0890000 00000000
00005114  00000000 00000000                       4230          DC    XL16'00000000000000042240000C2240000'
0000511C  42240000 C2240000
                                                  4231
                                                  4232
                                                  4233 * +27.15625, -27.15625
                                                  4234          VRR_A VCLFNL,2,0,00,00,N
00005128                                          4235+         DS    0FD
00005128                        00005128          4236+         USING *,R5              base for test data and test routine
00005128  000051B8                                4237+T76      DC    A(X76)            address of test routine
0000512C  004C                                    4238+         DC    H'76'             test number
0000512E  00                                      4239+         DC    X'00'
0000512F  D5                                      4240+         DC    CL1'N'            Y = skip cross check
00005130  02                                      4241+         DC    HL1'2'            m3
00005131  00                                      4242+         DC    HL1'0'            m4
00005132  00                                      4243+FLG76    DC    X'00'             expected FPC flags
00005133  00                                      4244+VXC76    DC    X'00'             expected VXC
00005134  000051EC                                4245+V2_76    DC    A(RE76+16)        address of v2: 16-byte packed decimal
00005138  E5C3D3C6 D5D34040                       4246+         DC    CL8'VCLFNL'       instruction name
00005140  00000010                                4247+         DC    A(16)             result length
00005144  000051DC                                4248+         DC    A(RE76)           address of expected resul
00005148  00000000 00000000                       4249+         DS    FD                gap
00005150  00000000 00000000                       4250+V1O76    DS    XL16              V1 output
00005158  00000000 00000000
00005160  00000000 00000000                       4251+         DS    FD                   gap
00005168  00000000                                4252+FPC_R_76 DS    F                 FPC after instruction
00005170  00000000 00000000                       4253+         DS    FD                   gap
00005178  40404040 40404040                       4254+         DC    CL8' '            was cross check skipped?
00005180  00000000 00000000                       4255+         DS    FD                   gap
00005188  00000000 00000000                       4256+XCO76    DS    XL16              Cross check Output
00005190  00000000 00000000
00005198  00000000 00000000                       4257+         DS    FD                   gap
000051A0  00000000                                4258+FPC_XC_76 DS   F                 FPC after cross check
000051A8  00000000 00000000                       4259+         DS    FD                   gap
000051B0  00000000                                4260+         DS    F                 debug area
000051B4  00000000                                4261+         DS    F
                                                  4262+*
000051B8                                          4263+X76      DS    0F
000051B8  B29D 85A4                     000007A4  4264+         LFPC  FPCINIT           initialize FPC
                                                  4265+*         LFPC  =XL4'08000000'          set trap exception
000051BC  E320 500C 0014                00005134  4266+         LGF   R2,V2_76          get v2
000051C2  E762 0000 0806                00000000  4267+         VL    V22,0(R2)
000051C8  E666 0000 2C5E                          4268+         VCLFNL V22,V22,2,0      test instruction (dest is source)
000051CE  B29C 5040                     00005168  4269+         STFPC FPC_R_76          save FPC
000051D2  E760 5028 080E                00005150  4270+         VST   V22,V1O76         save instruction result
000051D8  07FB                                    4271+         BR    R11               return
000051DC                                          4272+RE76     DS    0F                expected 16 byte result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000051DC                                           4273+         DROP  R5
000051DC  3BD94000 00000000                        4274          DC    XL16'3BD9400000000000BBD9400000000000'
000051E4  BBD94000 00000000
000051EC  00000000 00000000                        4275          DC    XL16'00000000000000002F650000AF650000'
000051F4  2F650000 AF650000
                                                   4276
                                                   4277 * +65504, -65504
                                                   4278          VRR_A VCLFNL,2,0,00,00,N
00005200                                           4279+         DS    0FD
00005200                        00005200           4280+         USING *,R5              base for test data and test routine
00005200  00005290                                 4281+T77      DC    A(X77)            address of test routine
00005204  004D                                     4282+         DC    H'77'             test number
00005206  00                                       4283+         DC    X'00'
00005207  D5                                       4284+         DC    CL1'N'            Y = skip cross check
00005208  02                                       4285+         DC    HL1'2'            m3
00005209  00                                       4286+         DC    HL1'0'            m4
0000520A  00                                       4287+FLG77    DC    X'00'             expected FPC flags
0000520B  00                                       4288+VXC77    DC    X'00'             expected VXC
0000520C  000052C4                                 4289+V2_77    DC    A(RE77+16)        address of v2: 16-byte packed decimal
00005210  E5C3D3C6 D5D34040                        4290+         DC    CL8'VCLFNL'       instruction name
00005218  00000010                                 4291+         DC    A(16)             result length
0000521C  000052B4                                 4292+         DC    A(RE77)           address of expected resul
00005220  00000000 00000000                        4293+         DS    FD                gap
00005228  00000000 00000000                        4294+V1O77    DS    XL16              V1 output
00005230  00000000 00000000
00005238  00000000 00000000                        4295+         DS    FD                   gap
00005240  00000000                                 4296+FPC_R_77 DS    F                 FPC after instruction
00005248  00000000 00000000                        4297+         DS    FD                   gap
00005250  40404040 40404040                        4298+         DC    CL8' '            was cross check skipped?
00005258  00000000 00000000                        4299+         DS    FD                   gap
00005260  00000000 00000000                        4300+XCO77    DS    XL16              Cross check Output
00005268  00000000 00000000
00005270  00000000 00000000                        4301+         DS    FD                   gap
00005278  00000000                                 4302+FPC_XC_77 DS   F                 FPC after cross check
00005280  00000000 00000000                        4303+         DS    FD                   gap
00005288  00000000                                 4304+         DS    F                 debug area
0000528C  00000000                                 4305+         DS    F
                                                   4306+*
00005290                                           4307+X77      DS    0F
00005290  B29D 85A4                     000007A4   4308+         LFPC  FPCINIT           initialize FPC
                                                   4309+*         LFPC  =XL4'08000000'          set trap exception
00005294  E320 500C 0014                0000520C   4310+         LGF   R2,V2_77          get v2
0000529A  E762 0000 0806                00000000   4311+         VL    V22,0(R2)
000052A0  E666 0000 2C5E                           4312+         VCLFNL V22,V22,2,0      test instruction (dest is source)
000052A6  B29C 5040                     00005240   4313+         STFPC FPC_R_77          save FPC
000052AA  E760 5028 080E                00005228   4314+         VST   V22,V1O77         save instruction result
000052B0  07FB                                     4315+         BR    R11               return
000052B4                                           4316+RE77     DS    0F                expected 16 byte result
000052B4                                           4317+         DROP  R5
000052B4  47800000 00000000                        4318          DC    XL16'4780000000000000C780000000000000'
000052BC  C7800000 00000000
000052C4  00000000 00000000                        4319          DC    XL16'00000000000000005E000000DE000000'
000052CC  5E000000 DE000000
                                                   4320
                                                   4321 * +Normal, -Normal (2.5)
                                                   4322          VRR_A VCLFNL,2,0,00,00,N
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000052D8                                           4323+         DS    0FD
000052D8                     000052D8              4324+         USING *,R5              base for test data and test routine
000052D8  00005368                                 4325+T78      DC    A(X78)            address of test routine
000052DC  004E                                     4326+         DC    H'78'             test number
000052DE  00                                       4327+         DC    X'00'
000052DF  D5                                       4328+         DC    CL1'N'            Y = skip cross check
000052E0  02                                       4329+         DC    HL1'2'            m3
000052E1  00                                       4330+         DC    HL1'0'            m4
000052E2  00                                       4331+FLG78    DC    X'00'             expected FPC flags
000052E3  00                                       4332+VXC78    DC    X'00'             expected VXC
000052E4  0000539C                                 4333+V2_78    DC    A(RE78+16)        address of v2: 16-byte packed decimal
000052E8  E5C3D3C6 D5D34040                        4334+         DC    CL8'VCLFNL'       instruction name
000052F0  00000010                                 4335+         DC    A(16)             result length
000052F4  0000538C                                 4336+         DC    A(RE78)           address of expected resul
000052F8  00000000 00000000                        4337+         DS    FD                gap
00005300  00000000 00000000                        4338+V1O78    DS    XL16              V1 output
00005308  00000000 00000000
00005310  00000000 00000000                        4339+         DS    FD                   gap
00005318  00000000                                 4340+FPC_R_78 DS    F                 FPC after instruction
00005320  00000000 00000000                        4341+         DS    FD                   gap
00005328  40404040 40404040                        4342+         DC    CL8' '            was cross check skipped?
00005330  00000000 00000000                        4343+         DS    FD                   gap
00005338  00000000 00000000                        4344+XCO78    DS    XL16              Cross check Output
00005340  00000000 00000000
00005348  00000000 00000000                        4345+         DS    FD                   gap
00005350  00000000                                 4346+FPC_XC_78 DS   F                 FPC after cross check
00005358  00000000 00000000                        4347+         DS    FD                   gap
00005360  00000000                                 4348+         DS    F                 debug area
00005364  00000000                                 4349+         DS    F
                                                   4350+*
00005368                                           4351+X78      DS    0F
00005368  B29D 85A4                     000007A4   4352+         LFPC  FPCINIT           initialize FPC
                                                   4353+*         LFPC  =XL4'08000000'          set trap exception
0000536C  E320 500C 0014                000052E4   4354+         LGF   R2,V2_78          get v2
00005372  E762 0000 0806                00000000   4355+         VL    V22,0(R2)
00005378  E666 0000 2C5E                           4356+         VCLFNL V22,V22,2,0      test instruction (dest is source)
0000537E  B29C 5040                     00005318   4357+         STFPC FPC_R_78          save FPC
00005382  E760 5028 080E                00005300   4358+         VST   V22,V1O78         save instruction result
00005388  07FB                                     4359+         BR    R11               return
0000538C                                           4360+RE78     DS    0F                expected 16 byte result
0000538C                                           4361+         DROP  R5
0000538C  40200000 00000000                        4362          DC    XL16'4020000000000000C020000000000000'
00005394  C0200000 00000000
0000539C  00000000 00000000                        4363          DC    XL16'00000000000000004080000C0800000'
000053A4  40800000 C0800000
                                                   4364
                                                   4365 * +0.00006097, -0.00006097 (about)
                                                   4366          VRR_A VCLFNL,2,0,00,00,N
000053B0                                           4367+         DS    0FD
000053B0                     000053B0              4368+         USING *,R5              base for test data and test routine
000053B0  00005440                                 4369+T79      DC    A(X79)            address of test routine
000053B4  004F                                     4370+         DC    H'79'             test number
000053B6  00                                       4371+         DC    X'00'
000053B7  D5                                       4372+         DC    CL1'N'            Y = skip cross check
000053B8  02                                       4373+         DC    HL1'2'            m3
000053B9  00                                       4374+         DC    HL1'0'            m4
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000053BA  00                                       4375+FLG79    DC    X'00'              expected FPC flags
000053BB  00                                       4376+VXC79    DC    X'00'              expected VXC
000053BC  00005474                                 4377+V2_79    DC    A(RE79+16)         address of v2: 16-byte packed decimal
000053C0  E5C3D3C6 D5D34040                        4378+         DC    CL8'VCLFNL'        instruction name
000053C8  00000010                                 4379+         DC    A(16)              result length
000053CC  00005464                                 4380+         DC    A(RE79)            address of expected resul
000053D0  00000000 00000000                        4381+         DS    FD                 gap
000053D8  00000000 00000000                        4382+V1O79    DS    XL16               V1 output
000053E0  00000000 00000000
000053E8  00000000 00000000                        4383+         DS    FD                    gap
000053F0  00000000                                 4384+FPC_R_79 DS    F                  FPC after instruction
000053F8  00000000 00000000                        4385+         DS    FD                    gap
00005400  40404040 40404040                        4386+         DC    CL8' '             was cross check skipped?
00005408  00000000 00000000                        4387+         DS    FD                    gap
00005410  00000000 00000000                        4388+XCO79    DS    XL16               Cross check Output
00005418  00000000 00000000
00005420  00000000 00000000                        4389+         DS    FD                    gap
00005428  00000000                                 4390+FPC_XC_79 DS   F                  FPC after cross check
00005430  00000000 00000000                        4391+         DS    FD                    gap
00005438  00000000                                 4392+         DS    F                  debug area
0000543C  00000000                                 4393+         DS    F
                                                   4394+*
00005440                                           4395+X79      DS    0F
00005440  B29D 85A4                     000007A4   4396+         LFPC  FPCINIT            initialize FPC
                                                   4397+*         LFPC  =XL4'08000000'          set trap exception
00005444  E320 500C 0014                000053BC   4398+         LGF   R2,V2_79           get v2
0000544A  E762 0000 0806                00000000   4399+         VL    V22,0(R2)
00005450  E666 0000 2C5E                           4400+         VCLFNL V22,V22,2,0       test instruction (dest is source)
00005456  B29C 5040                     000053F0   4401+         STFPC FPC_R_79           save FPC
0000545A  E760 5028 080E                000053D8   4402+         VST   V22,V1O79          save instruction result
00005460  07FB                                     4403+         BR    R11                return
00005464                                           4404+RE79     DS    0F                 expected 16 byte result
00005464                                           4405+         DROP  R5
00005464  387FC000 00000000                        4406          DC    XL16'387FC00000000000B87FC00000000000'
0000546C  B87FC000 00000000
00005474  00000000 00000000                        4407          DC    XL16'00000000000000000021FF0000A1FF0000'
0000547C  21FF0000 A1FF0000
                                                   4408
00005484  00000000                                 4409          DC    F'0'     END OF TABLE
00005488  00000000                                 4410          DC    F'0'
                                                   4411 *
                                                   4412 * table of pointers to individual tests
                                                   4413 *
0000548C                                           4414 E6TESTS  DS    0F
                                                   4415          PTTABLE
0000548C                                           4416+TTABLE   DS    0F
0000548C  000011E0                                 4417+         DC    A(T1)              TEST &CUR
00005490  000012B8                                 4418+         DC    A(T2)              TEST &CUR
00005494  00001390                                 4419+         DC    A(T3)              TEST &CUR
00005498  00001468                                 4420+         DC    A(T4)              TEST &CUR
0000549C  00001540                                 4421+         DC    A(T5)              TEST &CUR
000054A0  00001618                                 4422+         DC    A(T6)              TEST &CUR
000054A4  000016F0                                 4423+         DC    A(T7)              TEST &CUR
000054A8  000017C8                                 4424+         DC    A(T8)              TEST &CUR
000054AC  000018A0                                 4425+         DC    A(T9)              TEST &CUR
000054B0  00001978                                 4426+         DC    A(T10)             TEST &CUR
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000054B4  00001A50                                4427+         DC    A(T11)            TEST &CUR
000054B8  00001B28                                4428+         DC    A(T12)            TEST &CUR
000054BC  00001C00                                4429+         DC    A(T13)            TEST &CUR
000054C0  00001CD8                                4430+         DC    A(T14)            TEST &CUR
000054C4  00001DB0                                4431+         DC    A(T15)            TEST &CUR
000054C8  00001E88                                4432+         DC    A(T16)            TEST &CUR
000054CC  00001F60                                4433+         DC    A(T17)            TEST &CUR
000054D0  00002038                                4434+         DC    A(T18)            TEST &CUR
000054D4  00002110                                4435+         DC    A(T19)            TEST &CUR
000054D8  000021E8                                4436+         DC    A(T20)            TEST &CUR
000054DC  000022C0                                4437+         DC    A(T21)            TEST &CUR
000054E0  00002398                                4438+         DC    A(T22)            TEST &CUR
000054E4  00002470                                4439+         DC    A(T23)            TEST &CUR
000054E8  00002548                                4440+         DC    A(T24)            TEST &CUR
000054EC  00002620                                4441+         DC    A(T25)            TEST &CUR
000054F0  000026F8                                4442+         DC    A(T26)            TEST &CUR
000054F4  000027D0                                4443+         DC    A(T27)            TEST &CUR
000054F8  000028A8                                4444+         DC    A(T28)            TEST &CUR
000054FC  00002980                                4445+         DC    A(T29)            TEST &CUR
00005500  00002A58                                4446+         DC    A(T30)            TEST &CUR
00005504  00002B30                                4447+         DC    A(T31)            TEST &CUR
00005508  00002C08                                4448+         DC    A(T32)            TEST &CUR
0000550C  00002CE0                                4449+         DC    A(T33)            TEST &CUR
00005510  00002DB8                                4450+         DC    A(T34)            TEST &CUR
00005514  00002E90                                4451+         DC    A(T35)            TEST &CUR
00005518  00002F68                                4452+         DC    A(T36)            TEST &CUR
0000551C  00003040                                4453+         DC    A(T37)            TEST &CUR
00005520  00003118                                4454+         DC    A(T38)            TEST &CUR
00005524  000031F0                                4455+         DC    A(T39)            TEST &CUR
00005528  000032C8                                4456+         DC    A(T40)            TEST &CUR
0000552C  000033A0                                4457+         DC    A(T41)            TEST &CUR
00005530  00003478                                4458+         DC    A(T42)            TEST &CUR
00005534  00003550                                4459+         DC    A(T43)            TEST &CUR
00005538  00003628                                4460+         DC    A(T44)            TEST &CUR
0000553C  00003700                                4461+         DC    A(T45)            TEST &CUR
00005540  000037D8                                4462+         DC    A(T46)            TEST &CUR
00005544  000038B0                                4463+         DC    A(T47)            TEST &CUR
00005548  00003988                                4464+         DC    A(T48)            TEST &CUR
0000554C  00003A60                                4465+         DC    A(T49)            TEST &CUR
00005550  00003B38                                4466+         DC    A(T50)            TEST &CUR
00005554  00003C10                                4467+         DC    A(T51)            TEST &CUR
00005558  00003CE8                                4468+         DC    A(T52)            TEST &CUR
0000555C  00003DC0                                4469+         DC    A(T53)            TEST &CUR
00005560  00003E98                                4470+         DC    A(T54)            TEST &CUR
00005564  00003F70                                4471+         DC    A(T55)            TEST &CUR
00005568  00004048                                4472+         DC    A(T56)            TEST &CUR
0000556C  00004120                                4473+         DC    A(T57)            TEST &CUR
00005570  000041F8                                4474+         DC    A(T58)            TEST &CUR
00005574  000042D0                                4475+         DC    A(T59)            TEST &CUR
00005578  000043A8                                4476+         DC    A(T60)            TEST &CUR
0000557C  00004480                                4477+         DC    A(T61)            TEST &CUR
00005580  00004558                                4478+         DC    A(T62)            TEST &CUR
00005584  00004630                                4479+         DC    A(T63)            TEST &CUR
00005588  00004708                                4480+         DC    A(T64)            TEST &CUR
0000558C  000047E0                                4481+         DC    A(T65)            TEST &CUR
00005590  000048B8                                4482+         DC    A(T66)            TEST &CUR
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005594  00004990                                 4483+         DC    A(T67)            TEST &CUR
00005598  00004A68                                 4484+         DC    A(T68)            TEST &CUR
0000559C  00004B40                                 4485+         DC    A(T69)            TEST &CUR
000055A0  00004C18                                 4486+         DC    A(T70)            TEST &CUR
000055A4  00004CF0                                 4487+         DC    A(T71)            TEST &CUR
000055A8  00004DC8                                 4488+         DC    A(T72)            TEST &CUR
000055AC  00004EA0                                 4489+         DC    A(T73)            TEST &CUR
000055B0  00004F78                                 4490+         DC    A(T74)            TEST &CUR
000055B4  00005050                                 4491+         DC    A(T75)            TEST &CUR
000055B8  00005128                                 4492+         DC    A(T76)            TEST &CUR
000055BC  00005200                                 4493+         DC    A(T77)            TEST &CUR
000055C0  000052D8                                 4494+         DC    A(T78)            TEST &CUR
000055C4  000053B0                                 4495+         DC    A(T79)            TEST &CUR
                                                   4496+*
000055C8  00000000                                 4497+         DC    A(0)              END OF TABLE
000055CC  00000000                                 4498+         DC    A(0)
                                                   4499
000055D0  00000000                                 4500          DC    F'0'     END OF TABLE
000055D4  00000000                                 4501          DC    F'0'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                          4503 ************************************************************************
                                          4504 *        Register equates
                                          4505 ************************************************************************


                             00000000  00000001  4507 R0       EQU   0
                             00000001  00000001  4508 R1       EQU   1
                             00000002  00000001  4509 R2       EQU   2
                             00000003  00000001  4510 R3       EQU   3
                             00000004  00000001  4511 R4       EQU   4
                             00000005  00000001  4512 R5       EQU   5
                             00000006  00000001  4513 R6       EQU   6
                             00000007  00000001  4514 R7       EQU   7
                             00000008  00000001  4515 R8       EQU   8
                             00000009  00000001  4516 R9       EQU   9
                             0000000A  00000001  4517 R10      EQU   10
                             0000000B  00000001  4518 R11      EQU   11
                             0000000C  00000001  4519 R12      EQU   12
                             0000000D  00000001  4520 R13      EQU   13
                             0000000E  00000001  4521 R14      EQU   14
                             0000000F  00000001  4522 R15      EQU   15


                                          4524 ************************************************************************
                                          4525 *        Register equates
                                          4526 ************************************************************************


                             00000000  00000001  4528 FPR0     EQU   0
                             00000001  00000001  4529 FPR1     EQU   1
                             00000002  00000001  4530 FPR2     EQU   2
                             00000003  00000001  4531 FPR3     EQU   3
                             00000004  00000001  4532 FPR4     EQU   4
                             00000005  00000001  4533 FPR5     EQU   5
                             00000006  00000001  4534 FPR6     EQU   6
                             00000007  00000001  4535 FPR7     EQU   7
                             00000008  00000001  4536 FPR8     EQU   8
                             00000009  00000001  4537 FPR9     EQU   9
                             0000000A  00000001  4538 FPR10    EQU   10
                             0000000B  00000001  4539 FPR11    EQU   11
                             0000000C  00000001  4540 FPR12    EQU   12
                             0000000D  00000001  4541 FPR13    EQU   13
                             0000000E  00000001  4542 FPR14    EQU   14
                             0000000F  00000001  4543 FPR15    EQU   15


                                          4545 ************************************************************************
                                          4546 *        Register equates
                                          4547 ************************************************************************


                             00000000  00000001  4549 V0       EQU   0
                             00000001  00000001  4550 V1       EQU   1
                             00000002  00000001  4551 V2       EQU   2
                             00000003  00000001  4552 V3       EQU   3
                             00000004  00000001  4553 V4       EQU   4
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

                              00000005  00000001  4554 V5       EQU   5
                              00000006  00000001  4555 V6       EQU   6
                              00000007  00000001  4556 V7       EQU   7
                              00000008  00000001  4557 V8       EQU   8
                              00000009  00000001  4558 V9       EQU   9
                              0000000A  00000001  4559 V10      EQU   10
                              0000000B  00000001  4560 V11      EQU   11
                              0000000C  00000001  4561 V12      EQU   12
                              0000000D  00000001  4562 V13      EQU   13
                              0000000E  00000001  4563 V14      EQU   14
                              0000000F  00000001  4564 V15      EQU   15
                              00000010  00000001  4565 V16      EQU   16
                              00000011  00000001  4566 V17      EQU   17
                              00000012  00000001  4567 V18      EQU   18
                              00000013  00000001  4568 V19      EQU   19
                              00000014  00000001  4569 V20      EQU   20
                              00000015  00000001  4570 V21      EQU   21
                              00000016  00000001  4571 V22      EQU   22
                              00000017  00000001  4572 V23      EQU   23
                              00000018  00000001  4573 V24      EQU   24
                              00000019  00000001  4574 V25      EQU   25
                              0000001A  00000001  4575 V26      EQU   26
                              0000001B  00000001  4576 V27      EQU   27
                              0000001C  00000001  4577 V28      EQU   28
                              0000001D  00000001  4578 V29      EQU   29
                              0000001E  00000001  4579 V30      EQU   30
                              0000001F  00000001  4580 V31      EQU   31
                                                  4581
                                                  4582          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
BEGIN	I	00000200	2	177	141	173	174	175									
CHECKRES	U	00000324	1	257	254												
CHECKVXC	U	00000316	1	252	249												
CTLR0	F	0000079C	4	621	187	188	189	190									
DECNUM	C	00001190	16	743	380	382	389	391	396	398	427	429	436	438	443	445	463
					465	472	474	479	481	497	499	506	508	513	515		
DONEXT	U	00000334	1	271													
E6TEST	4	00000000	144	757	236												
E6TESTS	F	0000548C	4	4414	229												
EDIT	X	00001164	18	738	381	390	397	428	437	444	464	473	480	498	507	514	
ENDTEST	U	0000066C	1	535	234												
EOJ	I	00000780	4	611	222	538											
EOJPSW	D	00000770	8	609	611												
FAILCONT	U	0000065C	1	525													
FAILED	F	00001000	4	659	408	424	460	527	536								
FAILMSG	U	000005F4	1	495	269												
FAILPSW	D	00000788	8	613	615												
FAILTEST	I	00000798	4	615	539												
FB0001	F	00000298	8	206	210	211	213										
FLG	X	0000000A	1	764	248	435											
FLG1	X	000011EA	1	913													
FLG10	X	00001982	1	1309													
FLG11	X	00001A5A	1	1353													
FLG12	X	00001B32	1	1397													
FLG13	X	00001C0A	1	1441													
FLG14	X	00001CE2	1	1486													
FLG15	X	00001DBA	1	1530													
FLG16	X	00001E92	1	1574													
FLG17	X	00001F6A	1	1618													
FLG18	X	00002042	1	1662													
FLG19	X	0000211A	1	1706													
FLG2	X	000012C2	1	957													
FLG20	X	000021F2	1	1750													
FLG21	X	000022CA	1	1794													
FLG22	X	000023A2	1	1839													
FLG23	X	0000247A	1	1883													
FLG24	X	00002552	1	1933													
FLG25	X	0000262A	1	1977													
FLG26	X	00002702	1	2021													
FLG27	X	000027DA	1	2065													
FLG28	X	000028B2	1	2109													
FLG29	X	0000298A	1	2153													
FLG3	X	0000139A	1	1000													
FLG30	X	00002A62	1	2198													
FLG31	X	00002B3A	1	2242													
FLG32	X	00002C12	1	2286													
FLG33	X	00002CEA	1	2330													
FLG34	X	00002DC2	1	2374													
FLG35	X	00002E9A	1	2418													
FLG36	X	00002F72	1	2463													
FLG37	X	0000304A	1	2508													
FLG38	X	00003122	1	2552													
FLG39	X	000031FA	1	2596													
FLG4	X	00001472	1	1044													
FLG40	X	000032D2	1	2640													
FLG41	X	000033AA	1	2690													

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
FLG42	X	00003482	1	2734													
FLG43	X	0000355A	1	2778													
FLG44	X	00003632	1	2822													
FLG45	X	0000370A	1	2866													
FLG46	X	000037E2	1	2910													
FLG47	X	000038BA	1	2954													
FLG48	X	00003992	1	2999													
FLG49	X	00003A6A	1	3043													
FLG5	X	0000154A	1	1088													
FLG50	X	00003B42	1	3087													
FLG51	X	00003C1A	1	3131													
FLG52	X	00003CF2	1	3175													
FLG53	X	00003DCA	1	3219													
FLG54	X	00003EA2	1	3263													
FLG55	X	00003F7A	1	3308													
FLG56	X	00004052	1	3353													
FLG57	X	0000412A	1	3397													
FLG58	X	00004202	1	3441													
FLG59	X	000042DA	1	3485													
FLG6	X	00001622	1	1132													
FLG60	X	000043B2	1	3530													
FLG61	X	0000448A	1	3574													
FLG62	X	00004562	1	3618													
FLG63	X	0000463A	1	3668													
FLG64	X	00004712	1	3712													
FLG65	X	000047EA	1	3756													
FLG66	X	000048C2	1	3800													
FLG67	X	0000499A	1	3844													
FLG68	X	00004A72	1	3888													
FLG69	X	00004B4A	1	3933													
FLG7	X	000016FA	1	1176													
FLG70	X	00004C22	1	3977													
FLG71	X	00004CFA	1	4021													
FLG72	X	00004DD2	1	4065													
FLG73	X	00004EAA	1	4109													
FLG74	X	00004F82	1	4153													
FLG75	X	0000505A	1	4198													
FLG76	X	00005132	1	4243													
FLG77	X	0000520A	1	4287													
FLG78	X	000052E2	1	4331													
FLG79	X	000053BA	1	4375													
FLG8	X	000017D2	1	1221													
FLG9	X	000018AA	1	1265													
FPCINIT	X	000007A4	4	623	307	325	343	361	934	978	1021	1065	1109	1153	1197	1242	1286
					1330	1374	1418	1462	1507	1551	1595	1639	1683	1727	1771	1815	1860
					1904	1954	1998	2042	2086	2130	2174	2219	2263	2307	2351	2395	2439
					2484	2529	2573	2617	2661	2711	2755	2799	2843	2887	2931	2975	3020
					3064	3108	3152	3196	3240	3284	3329	3374	3418	3462	3506	3551	3595
					3639	3689	3733	3777	3821	3865	3909	3954	3998	4042	4086	4130	4174
					4219	4264	4308	4352	4396								
FPCMSG	U	00000510	1	422	250												
FPCPEXP	C	00001052	3	674	439												
FPCPGOT	C	00001067	3	677	446												
FPCPLINE	C	00001008	13	669	679	449											
FPCPLNG	U	00000063	1	679	448												
FPCPNAME	C	00001039	8	672	432												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
FPCPNUM	C	00001015	3	670	430			
FPC_R	F	00000040	4	773	248	253	283	442	478
FPC_R_1	F	00001220	4	922	939				
FPC_R_10	F	000019B8	4	1318	1335				
FPC_R_11	F	00001A90	4	1362	1379				
FPC_R_12	F	00001B68	4	1406	1423				
FPC_R_13	F	00001C40	4	1450	1467				
FPC_R_14	F	00001D18	4	1495	1512				
FPC_R_15	F	00001DF0	4	1539	1556				
FPC_R_16	F	00001EC8	4	1583	1600				
FPC_R_17	F	00001FA0	4	1627	1644				
FPC_R_18	F	00002078	4	1671	1688				
FPC_R_19	F	00002150	4	1715	1732				
FPC_R_2	F	000012F8	4	966	983				
FPC_R_20	F	00002228	4	1759	1776				
FPC_R_21	F	00002300	4	1803	1820				
FPC_R_22	F	000023D8	4	1848	1865				
FPC_R_23	F	000024B0	4	1892	1909				
FPC_R_24	F	00002588	4	1942	1959				
FPC_R_25	F	00002660	4	1986	2003				
FPC_R_26	F	00002738	4	2030	2047				
FPC_R_27	F	00002810	4	2074	2091				
FPC_R_28	F	000028E8	4	2118	2135				
FPC_R_29	F	000029C0	4	2162	2179				
FPC_R_3	F	000013D0	4	1009	1026				
FPC_R_30	F	00002A98	4	2207	2224				
FPC_R_31	F	00002B70	4	2251	2268				
FPC_R_32	F	00002C48	4	2295	2312				
FPC_R_33	F	00002D20	4	2339	2356				
FPC_R_34	F	00002DF8	4	2383	2400				
FPC_R_35	F	00002ED0	4	2427	2444				
FPC_R_36	F	00002FA8	4	2472	2489				
FPC_R_37	F	00003080	4	2517	2534				
FPC_R_38	F	00003158	4	2561	2578				
FPC_R_39	F	00003230	4	2605	2622				
FPC_R_4	F	000014A8	4	1053	1070				
FPC_R_40	F	00003308	4	2649	2666				
FPC_R_41	F	000033E0	4	2699	2716				
FPC_R_42	F	000034B8	4	2743	2760				
FPC_R_43	F	00003590	4	2787	2804				
FPC_R_44	F	00003668	4	2831	2848				
FPC_R_45	F	00003740	4	2875	2892				
FPC_R_46	F	00003818	4	2919	2936				
FPC_R_47	F	000038F0	4	2963	2980				
FPC_R_48	F	000039C8	4	3008	3025				
FPC_R_49	F	00003AA0	4	3052	3069				
FPC_R_5	F	00001580	4	1097	1114				
FPC_R_50	F	00003B78	4	3096	3113				
FPC_R_51	F	00003C50	4	3140	3157				
FPC_R_52	F	00003D28	4	3184	3201				
FPC_R_53	F	00003E00	4	3228	3245				
FPC_R_54	F	00003ED8	4	3272	3289				
FPC_R_55	F	00003FB0	4	3317	3334				
FPC_R_56	F	00004088	4	3362	3379				
FPC_R_57	F	00004160	4	3406	3423				
FPC_R_58	F	00004238	4	3450	3467				

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
FPC_R_59	F	00004310	4	3494	3511
FPC_R_6	F	00001658	4	1141	1158
FPC_R_60	F	000043E8	4	3539	3556
FPC_R_61	F	000044C0	4	3583	3600
FPC_R_62	F	00004598	4	3627	3644
FPC_R_63	F	00004670	4	3677	3694
FPC_R_64	F	00004748	4	3721	3738
FPC_R_65	F	00004820	4	3765	3782
FPC_R_66	F	000048F8	4	3809	3826
FPC_R_67	F	000049D0	4	3853	3870
FPC_R_68	F	00004AA8	4	3897	3914
FPC_R_69	F	00004B80	4	3942	3959
FPC_R_7	F	00001730	4	1185	1202
FPC_R_70	F	00004C58	4	3986	4003
FPC_R_71	F	00004D30	4	4030	4047
FPC_R_72	F	00004E08	4	4074	4091
FPC_R_73	F	00004EE0	4	4118	4135
FPC_R_74	F	00004FB8	4	4162	4179
FPC_R_75	F	00005090	4	4207	4224
FPC_R_76	F	00005168	4	4252	4269
FPC_R_77	F	00005240	4	4296	4313
FPC_R_78	F	00005318	4	4340	4357
FPC_R_79	F	000053F0	4	4384	4401
FPC_R_8	F	00001808	4	1230	1247
FPC_R_9	F	000018E0	4	1274	1291
FPC_XC	F	00000078	4	779	311 314 329 332 347 350 365 368
FPC_XC_1	F	00001258	4	928	
FPC_XC_10	F	000019F0	4	1324	
FPC_XC_11	F	00001AC8	4	1368	
FPC_XC_12	F	00001BA0	4	1412	
FPC_XC_13	F	00001C78	4	1456	
FPC_XC_14	F	00001D50	4	1501	
FPC_XC_15	F	00001E28	4	1545	
FPC_XC_16	F	00001F00	4	1589	
FPC_XC_17	F	00001FD8	4	1633	
FPC_XC_18	F	000020B0	4	1677	
FPC_XC_19	F	00002188	4	1721	
FPC_XC_2	F	00001330	4	972	
FPC_XC_20	F	00002260	4	1765	
FPC_XC_21	F	00002338	4	1809	
FPC_XC_22	F	00002410	4	1854	
FPC_XC_23	F	000024E8	4	1898	
FPC_XC_24	F	000025C0	4	1948	
FPC_XC_25	F	00002698	4	1992	
FPC_XC_26	F	00002770	4	2036	
FPC_XC_27	F	00002848	4	2080	
FPC_XC_28	F	00002920	4	2124	
FPC_XC_29	F	000029F8	4	2168	
FPC_XC_3	F	00001408	4	1015	
FPC_XC_30	F	00002AD0	4	2213	
FPC_XC_31	F	00002BA8	4	2257	
FPC_XC_32	F	00002C80	4	2301	
FPC_XC_33	F	00002D58	4	2345	
FPC_XC_34	F	00002E30	4	2389	
FPC_XC_35	F	00002F08	4	2433	
FPC_XC_36	F	00002FE0	4	2478	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
FPC_XC_37	F	000030B8	4	2523	
FPC_XC_38	F	00003190	4	2567	
FPC_XC_39	F	00003268	4	2611	
FPC_XC_4	F	000014E0	4	1059	
FPC_XC_40	F	00003340	4	2655	
FPC_XC_41	F	00003418	4	2705	
FPC_XC_42	F	000034F0	4	2749	
FPC_XC_43	F	000035C8	4	2793	
FPC_XC_44	F	000036A0	4	2837	
FPC_XC_45	F	00003778	4	2881	
FPC_XC_46	F	00003850	4	2925	
FPC_XC_47	F	00003928	4	2969	
FPC_XC_48	F	00003A00	4	3014	
FPC_XC_49	F	00003AD8	4	3058	
FPC_XC_5	F	000015B8	4	1103	
FPC_XC_50	F	00003BB0	4	3102	
FPC_XC_51	F	00003C88	4	3146	
FPC_XC_52	F	00003D60	4	3190	
FPC_XC_53	F	00003E38	4	3234	
FPC_XC_54	F	00003F10	4	3278	
FPC_XC_55	F	00003FE8	4	3323	
FPC_XC_56	F	000040C0	4	3368	
FPC_XC_57	F	00004198	4	3412	
FPC_XC_58	F	00004270	4	3456	
FPC_XC_59	F	00004348	4	3500	
FPC_XC_6	F	00001690	4	1147	
FPC_XC_60	F	00004420	4	3545	
FPC_XC_61	F	000044F8	4	3589	
FPC_XC_62	F	000045D0	4	3633	
FPC_XC_63	F	000046A8	4	3683	
FPC_XC_64	F	00004780	4	3727	
FPC_XC_65	F	00004858	4	3771	
FPC_XC_66	F	00004930	4	3815	
FPC_XC_67	F	00004A08	4	3859	
FPC_XC_68	F	00004AE0	4	3903	
FPC_XC_69	F	00004BB8	4	3948	
FPC_XC_7	F	00001768	4	1191	
FPC_XC_70	F	00004C90	4	3992	
FPC_XC_71	F	00004D68	4	4036	
FPC_XC_72	F	00004E40	4	4080	
FPC_XC_73	F	00004F18	4	4124	
FPC_XC_74	F	00004FF0	4	4168	
FPC_XC_75	F	000050C8	4	4213	
FPC_XC_76	F	000051A0	4	4258	
FPC_XC_77	F	00005278	4	4302	
FPC_XC_78	F	00005350	4	4346	
FPC_XC_79	F	00005428	4	4390	
FPC_XC_8	F	00001840	4	1236	
FPC_XC_9	F	00001918	4	1280	
FPR0	U	00000000	1	4528	
FPR1	U	00000001	1	4529	
FPR10	U	0000000A	1	4538	
FPR11	U	0000000B	1	4539	
FPR12	U	0000000C	1	4540	
FPR13	U	0000000D	1	4541	
FPR14	U	0000000E	1	4542	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
FPR15	U	0000000F	1	4543													
FPR2	U	00000002	1	4530													
FPR3	U	00000003	1	4531													
FPR4	U	00000004	1	4532													
FPR5	U	00000005	1	4533													
FPR6	U	00000006	1	4534													
FPR7	U	00000007	1	4535													
FPR8	U	00000008	1	4536													
FPR9	U	00000009	1	4537													
IMAGE	1	00000000	21976	0													
K	U	00000400	1	642	643	644	645										
K64	U	00010000	1	644													
M3	U	00000008	1	762	388	505											
M4	U	00000009	1	763	395	512											
MB	U	00100000	1	645													
MSG	I	000006B0	4	571	221	554											
MSGCMD	C	000006FE	9	601	584	585											
MSGMSG	C	00000707	100	602	578	599	576										
MSGMVC	I	000006F8	6	599	582												
MSGOK	I	000006C6	2	580	577												
MSGRET	I	000006E6	4	595	588	591											
MSGSAVE	F	000006EC	4	598	574	595											
NEXTE6	U	000002EC	1	231	273	530											
OPNAME	C	00000010	8	767	289	292	295	298	385	432	468	502					
PAGE	U	00001000	1	643													
PRT3	C	0000117A	18	741	381	382	383	390	391	392	397	398	399	428	429	430	437
					438	439	444	445	446	464	465	466	473	474	475	480	481
					482	498	499	500	507	508	509	514	515	516			
PRTLINE	C	000010CE	13	706	716	519											
PRTLNG	U	00000048	1	716	518												
PRTM3	C	00001107	2	711	509												
PRTM4	C	00001113	2	714	516												
PRTNAME	C	000010F6	8	709	502												
PRTNUM	C	000010DB	3	707	500												
R0	U	00000000	1	4507	135	187	190	210	212	213	214	219	238	239	402	407	408
					423	424	448	459	460	484	518	526	527	553	555	571	574
					576	578	580	595									
R1	U	00000001	1	4508	220	267	268	317	318	335	336	353	354	371	372	403	449
					485	519	536	537	585	599							
R10	U	0000000A	1	4517	175	184	185										
R11	U	0000000B	1	4518	241	242	941	985	1028	1072	1116	1160	1204	1249	1293	1337	1381
					1425	1469	1514	1558	1602	1646	1690	1734	1778	1822	1867	1911	1961
					2005	2049	2093	2137	2181	2226	2270	2314	2358	2402	2446	2491	2536
					2580	2624	2668	2718	2762	2806	2850	2894	2938	2982	3027	3071	3115
					3159	3203	3247	3291	3336	3381	3425	3469	3513	3558	3602	3646	3696
					3740	3784	3828	3872	3916	3961	4005	4049	4093	4137	4181	4226	4271
					4315	4359	4403										
R12	U	0000000C	1	4519	229	232	272	529									
R13	U	0000000D	1	4520													
R14	U	0000000E	1	4521													
R15	U	0000000F	1	4522	244	282	284	302	315	320	333	338	351	356	369	374	401
					404	405	409	450	486	520	548	558	559				
R2	U	00000002	1	4509	221	379	380	387	388	389	394	395	396	426	427	434	435
					436	441	442	443	462	463	470	471	472	477	478	479	496
					497	504	505	506	511	512	513	553	554	555	572	574	580
					581	582	584	590	595	596	936	937	980	981	1023	1024	1067

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					1068	1111	1112	1155	1156	1199	1200	1244	1245	1288	1289	1332	1333
					1376	1377	1420	1421	1464	1465	1509	1510	1553	1554	1597	1598	1641
					1642	1685	1686	1729	1730	1773	1774	1817	1818	1862	1863	1906	1907
					1956	1957	2000	2001	2044	2045	2088	2089	2132	2133	2176	2177	2221
					2222	2265	2266	2309	2310	2353	2354	2397	2398	2441	2442	2486	2487
					2531	2532	2575	2576	2619	2620	2663	2664	2713	2714	2757	2758	2801
					2802	2845	2846	2889	2890	2933	2934	2977	2978	3022	3023	3066	3067
					3110	3111	3154	3155	3198	3199	3242	3243	3286	3287	3331	3332	3376
					3377	3420	3421	3464	3465	3508	3509	3553	3554	3597	3598	3641	3642
					3691	3692	3735	3736	3779	3780	3823	3824	3867	3868	3911	3912	3956
					3957	4000	4001	4044	4045	4088	4089	4132	4133	4176	4177	4221	4222
					4266	4267	4310	4311	4354	4355	4398	4399					
R3	U	00000003	1	4510													
R4	U	00000004	1	4511													
R5	U	00000005	1	4512	232	233	236	549	557	906	943	950	987	993	1030	1037	1074
					1081	1118	1125	1162	1169	1206	1214	1251	1258	1295	1302	1339	1346
					1383	1390	1427	1434	1471	1479	1516	1523	1560	1567	1604	1611	1648
					1655	1692	1699	1736	1743	1780	1787	1824	1832	1869	1876	1913	1926
					1963	1970	2007	2014	2051	2058	2095	2102	2139	2146	2183	2191	2228
					2235	2272	2279	2316	2323	2360	2367	2404	2411	2448	2456	2493	2501
					2538	2545	2582	2589	2626	2633	2670	2683	2720	2727	2764	2771	2808
					2815	2852	2859	2896	2903	2940	2947	2984	2992	3029	3036	3073	3080
					3117	3124	3161	3168	3205	3212	3249	3256	3293	3301	3338	3346	3383
					3390	3427	3434	3471	3478	3515	3523	3560	3567	3604	3611	3648	3661
					3698	3705	3742	3749	3786	3793	3830	3837	3874	3881	3918	3926	3963
					3970	4007	4014	4051	4058	4095	4102	4139	4146	4183	4191	4228	4236
					4273	4280	4317	4324	4361	4368	4405						
R6	U	00000006	1	4513													
R7	U	00000007	1	4514	250	255	451	487									
R8	U	00000008	1	4515	173	177	178	179	181								
R9	U	00000009	1	4516	174	181	182	184									
RE1	F	00001294	4	942	915	918											
RE10	F	00001A2C	4	1338	1311	1314											
RE11	F	00001B04	4	1382	1355	1358											
RE12	F	00001BDC	4	1426	1399	1402											
RE13	F	00001CB4	4	1470	1443	1446											
RE14	F	00001D8C	4	1515	1488	1491											
RE15	F	00001E64	4	1559	1532	1535											
RE16	F	00001F3C	4	1603	1576	1579											
RE17	F	00002014	4	1647	1620	1623											
RE18	F	000020EC	4	1691	1664	1667											
RE19	F	000021C4	4	1735	1708	1711											
RE2	F	0000136C	4	986	959	962											
RE20	F	0000229C	4	1779	1752	1755											
RE21	F	00002374	4	1823	1796	1799											
RE22	F	0000244C	4	1868	1841	1844											
RE23	F	00002524	4	1912	1885	1888											
RE24	F	000025FC	4	1962	1935	1938											
RE25	F	000026D4	4	2006	1979	1982											
RE26	F	000027AC	4	2050	2023	2026											
RE27	F	00002884	4	2094	2067	2070											
RE28	F	0000295C	4	2138	2111	2114											
RE29	F	00002A34	4	2182	2155	2158											
RE3	F	00001444	4	1029	1002	1005											
RE30	F	00002B0C	4	2227	2200	2203											
RE31	F	00002BE4	4	2271	2244	2247											

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
RE32	F	00002CBC	4	2315	2288	2291
RE33	F	00002D94	4	2359	2332	2335
RE34	F	00002E6C	4	2403	2376	2379
RE35	F	00002F44	4	2447	2420	2423
RE36	F	0000301C	4	2492	2465	2468
RE37	F	000030F4	4	2537	2510	2513
RE38	F	000031CC	4	2581	2554	2557
RE39	F	000032A4	4	2625	2598	2601
RE4	F	0000151C	4	1073	1046	1049
RE40	F	0000337C	4	2669	2642	2645
RE41	F	00003454	4	2719	2692	2695
RE42	F	0000352C	4	2763	2736	2739
RE43	F	00003604	4	2807	2780	2783
RE44	F	000036DC	4	2851	2824	2827
RE45	F	000037B4	4	2895	2868	2871
RE46	F	0000388C	4	2939	2912	2915
RE47	F	00003964	4	2983	2956	2959
RE48	F	00003A3C	4	3028	3001	3004
RE49	F	00003B14	4	3072	3045	3048
RE5	F	000015F4	4	1117	1090	1093
RE50	F	00003BEC	4	3116	3089	3092
RE51	F	00003CC4	4	3160	3133	3136
RE52	F	00003D9C	4	3204	3177	3180
RE53	F	00003E74	4	3248	3221	3224
RE54	F	00003F4C	4	3292	3265	3268
RE55	F	00004024	4	3337	3310	3313
RE56	F	000040FC	4	3382	3355	3358
RE57	F	000041D4	4	3426	3399	3402
RE58	F	000042AC	4	3470	3443	3446
RE59	F	00004384	4	3514	3487	3490
RE6	F	000016CC	4	1161	1134	1137
RE60	F	0000445C	4	3559	3532	3535
RE61	F	00004534	4	3603	3576	3579
RE62	F	0000460C	4	3647	3620	3623
RE63	F	000046E4	4	3697	3670	3673
RE64	F	000047BC	4	3741	3714	3717
RE65	F	00004894	4	3785	3758	3761
RE66	F	0000496C	4	3829	3802	3805
RE67	F	00004A44	4	3873	3846	3849
RE68	F	00004B1C	4	3917	3890	3893
RE69	F	00004BF4	4	3962	3935	3938
RE7	F	000017A4	4	1205	1178	1181
RE70	F	00004CCC	4	4006	3979	3982
RE71	F	00004DA4	4	4050	4023	4026
RE72	F	00004E7C	4	4094	4067	4070
RE73	F	00004F54	4	4138	4111	4114
RE74	F	0000502C	4	4182	4155	4158
RE75	F	00005104	4	4227	4200	4203
RE76	F	000051DC	4	4272	4245	4248
RE77	F	000052B4	4	4316	4289	4292
RE78	F	0000538C	4	4360	4333	4336
RE79	F	00005464	4	4404	4377	4380
RE8	F	0000187C	4	1250	1223	1226
RE9	F	00001954	4	1294	1267	1270
READDR	A	0000001C	4	769	267	
REG2LOW	U	000000DD	1	649		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
REG2PATT	U	AABBCCDD	1	648				
RELEN	A	00000018	4	768				
RPTDWSAV	D	000006A0	8	564	553	555		
RPTERROR	I	0000067A	4	548	404	450	486	520
RPTSAVE	F	00000698	4	561	548	558		
RPTSVR5	F	0000069C	4	562	549	557		
SKIPXC	C	00000050	8	775	280	288	301	
SKL0001	U	0000005F	1	203	219			
SKT0001	C	0000022A	26	200	203	220		
SVOLDPSW	U	00000140	0	137				
T1	A	000011E0	4	907	4417			
T10	A	00001978	4	1303	4426			
T11	A	00001A50	4	1347	4427			
T12	A	00001B28	4	1391	4428			
T13	A	00001C00	4	1435	4429			
T14	A	00001CD8	4	1480	4430			
T15	A	00001DB0	4	1524	4431			
T16	A	00001E88	4	1568	4432			
T17	A	00001F60	4	1612	4433			
T18	A	00002038	4	1656	4434			
T19	A	00002110	4	1700	4435			
T2	A	000012B8	4	951	4418			
T20	A	000021E8	4	1744	4436			
T21	A	000022C0	4	1788	4437			
T22	A	00002398	4	1833	4438			
T23	A	00002470	4	1877	4439			
T24	A	00002548	4	1927	4440			
T25	A	00002620	4	1971	4441			
T26	A	000026F8	4	2015	4442			
T27	A	000027D0	4	2059	4443			
T28	A	000028A8	4	2103	4444			
T29	A	00002980	4	2147	4445			
T3	A	00001390	4	994	4419			
T30	A	00002A58	4	2192	4446			
T31	A	00002B30	4	2236	4447			
T32	A	00002C08	4	2280	4448			
T33	A	00002CE0	4	2324	4449			
T34	A	00002DB8	4	2368	4450			
T35	A	00002E90	4	2412	4451			
T36	A	00002F68	4	2457	4452			
T37	A	00003040	4	2502	4453			
T38	A	00003118	4	2546	4454			
T39	A	000031F0	4	2590	4455			
T4	A	00001468	4	1038	4420			
T40	A	000032C8	4	2634	4456			
T41	A	000033A0	4	2684	4457			
T42	A	00003478	4	2728	4458			
T43	A	00003550	4	2772	4459			
T44	A	00003628	4	2816	4460			
T45	A	00003700	4	2860	4461			
T46	A	000037D8	4	2904	4462			
T47	A	000038B0	4	2948	4463			
T48	A	00003988	4	2993	4464			
T49	A	00003A60	4	3037	4465			
T5	A	00001540	4	1082	4421			
T50	A	00003B38	4	3081	4466			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES							
T51	A	00003C10	4	3125	4467							
T52	A	00003CE8	4	3169	4468							
T53	A	00003DC0	4	3213	4469							
T54	A	00003E98	4	3257	4470							
T55	A	00003F70	4	3302	4471							
T56	A	00004048	4	3347	4472							
T57	A	00004120	4	3391	4473							
T58	A	000041F8	4	3435	4474							
T59	A	000042D0	4	3479	4475							
T6	A	00001618	4	1126	4422							
T60	A	000043A8	4	3524	4476							
T61	A	00004480	4	3568	4477							
T62	A	00004558	4	3612	4478							
T63	A	00004630	4	3662	4479							
T64	A	00004708	4	3706	4480							
T65	A	000047E0	4	3750	4481							
T66	A	000048B8	4	3794	4482							
T67	A	00004990	4	3838	4483							
T68	A	00004A68	4	3882	4484							
T69	A	00004B40	4	3927	4485							
T7	A	000016F0	4	1170	4423							
T70	A	00004C18	4	3971	4486							
T71	A	00004CF0	4	4015	4487							
T72	A	00004DC8	4	4059	4488							
T73	A	00004EA0	4	4103	4489							
T74	A	00004F78	4	4147	4490							
T75	A	00005050	4	4192	4491							
T76	A	00005128	4	4237	4492							
T77	A	00005200	4	4281	4493							
T78	A	000052D8	4	4325	4494							
T79	A	000053B0	4	4369	4495							
T8	A	000017C8	4	1215	4424							
T9	A	000018A0	4	1259	4425							
TESTING	F	00001004	4	660	239							
TNUM	H	00000004	2	759	238	379	426	462	496			
TSUB	A	00000000	4	758	241							
TTABLE	F	0000548C	4	4416								
V0	U	00000000	1	4549								
V1	U	00000001	1	4550								
V10	U	0000000A	1	4559								
V11	U	0000000B	1	4560								
V12	U	0000000C	1	4561								
V13	U	0000000D	1	4562								
V14	U	0000000E	1	4563								
V15	U	0000000F	1	4564	310	312	328	330	346	348	364	366
V16	U	00000010	1	4565	309	310	327	328	345	346	363	364
V17	U	00000011	1	4566								
V18	U	00000012	1	4567								
V19	U	00000013	1	4568								
V1FUDGE	X	000011B0	16	749								
V1INPUT	X	000011C0	16	750								
V1O1	X	00001208	16	920	940							
V1O10	X	000019A0	16	1316	1336							
V1O11	X	00001A78	16	1360	1380							
V1O12	X	00001B50	16	1404	1424							
V1O13	X	00001C28	16	1448	1468							

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1014	X	00001D00	16	1493	1513
V1015	X	00001DD8	16	1537	1557
V1016	X	00001EB0	16	1581	1601
V1017	X	00001F88	16	1625	1645
V1018	X	00002060	16	1669	1689
V1019	X	00002138	16	1713	1733
V102	X	000012E0	16	964	984
V1020	X	00002210	16	1757	1777
V1021	X	000022E8	16	1801	1821
V1022	X	000023C0	16	1846	1866
V1023	X	00002498	16	1890	1910
V1024	X	00002570	16	1940	1960
V1025	X	00002648	16	1984	2004
V1026	X	00002720	16	2028	2048
V1027	X	000027F8	16	2072	2092
V1028	X	000028D0	16	2116	2136
V1029	X	000029A8	16	2160	2180
V103	X	000013B8	16	1007	1027
V1030	X	00002A80	16	2205	2225
V1031	X	00002B58	16	2249	2269
V1032	X	00002C30	16	2293	2313
V1033	X	00002D08	16	2337	2357
V1034	X	00002DE0	16	2381	2401
V1035	X	00002EB8	16	2425	2445
V1036	X	00002F90	16	2470	2490
V1037	X	00003068	16	2515	2535
V1038	X	00003140	16	2559	2579
V1039	X	00003218	16	2603	2623
V104	X	00001490	16	1051	1071
V1040	X	000032F0	16	2647	2667
V1041	X	000033C8	16	2697	2717
V1042	X	000034A0	16	2741	2761
V1043	X	00003578	16	2785	2805
V1044	X	00003650	16	2829	2849
V1045	X	00003728	16	2873	2893
V1046	X	00003800	16	2917	2937
V1047	X	000038D8	16	2961	2981
V1048	X	000039B0	16	3006	3026
V1049	X	00003A88	16	3050	3070
V105	X	00001568	16	1095	1115
V1050	X	00003B60	16	3094	3114
V1051	X	00003C38	16	3138	3158
V1052	X	00003D10	16	3182	3202
V1053	X	00003DE8	16	3226	3246
V1054	X	00003EC0	16	3270	3290
V1055	X	00003F98	16	3315	3335
V1056	X	00004070	16	3360	3380
V1057	X	00004148	16	3404	3424
V1058	X	00004220	16	3448	3468
V1059	X	000042F8	16	3492	3512
V106	X	00001640	16	1139	1159
V1060	X	000043D0	16	3537	3557
V1061	X	000044A8	16	3581	3601
V1062	X	00004580	16	3625	3645
V1063	X	00004658	16	3675	3695
V1064	X	00004730	16	3719	3739

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1O65	X	00004808	16	3763	3783
V1O66	X	000048E0	16	3807	3827
V1O67	X	000049B8	16	3851	3871
V1O68	X	00004A90	16	3895	3915
V1O69	X	00004B68	16	3940	3960
V1O7	X	00001718	16	1183	1203
V1O70	X	00004C40	16	3984	4004
V1O71	X	00004D18	16	4028	4048
V1O72	X	00004DF0	16	4072	4092
V1O73	X	00004EC8	16	4116	4136
V1O74	X	00004FA0	16	4160	4180
V1O75	X	00005078	16	4205	4225
V1O76	X	00005150	16	4250	4270
V1O77	X	00005228	16	4294	4314
V1O78	X	00005300	16	4338	4358
V1O79	X	000053D8	16	4382	4402
V1O8	X	000017F0	16	1228	1248
V1O9	X	000018C8	16	1272	1292
V1OUTPUT	X	00000028	16	771	268 309 327 345 363
V2	U	00000002	1	4551	
V20	U	00000014	1	4569	
V21	U	00000015	1	4570	
V22	U	00000016	1	4571	937 938 940 981 982 984 1024 1025 1027 1068 1069 1071 1112 1113 1115 1156 1157 1159 1200 1201 1203 1245 1246 1248 1289 1290 1292 1333 1334 1336 1377 1378 1380 1421 1422 1424 1465 1466 1468 1510 1511 1513 1554 1555 1557 1598 1599 1601 1642 1643 1645 1686 1687 1689 1730 1731 1733 1774 1775 1777 1818 1819 1821 1863 1864 1866 1907 1908 1910 1957 1958 1960 2001 2002 2004 2045 2046 2048 2089 2090 2092 2133 2134 2136 2177 2178 2180 2222 2223 2225 2266 2267 2269 2310 2311 2313 2354 2355 2357 2398 2399 2401 2442 2443 2445 2487 2488 2490 2532 2533 2535 2576 2577 2579 2620 2621 2623 2664 2665 2667 2714 2715 2717 2758 2759 2761 2802 2803 2805 2846 2847 2849 2890 2891 2893 2934 2935 2937 2978 2979 2981 3023 3024 3026 3067 3068 3070 3111 3112 3114 3155 3156 3158 3199 3200 3202 3243 3244 3246 3287 3288 3290 3332 3333 3335 3377 3378 3380 3421 3422 3424 3465 3466 3468 3509 3510 3512 3554 3555 3557 3598 3599 3601 3642 3643 3645 3692 3693 3695 3736 3737 3739 3780 3781 3783 3824 3825 3827 3868 3869 3871 3912 3913 3915 3957 3958 3960 4001 4002 4004 4045 4046 4048 4089 4090 4092 4133 4134 4136 4177 4178 4180 4222 4223 4225 4267 4268 4270 4311 4312 4314 4355 4356 4358 4399 4400 4402
V23	U	00000017	1	4572	
V24	U	00000018	1	4573	
V25	U	00000019	1	4574	
V26	U	0000001A	1	4575	
V27	U	0000001B	1	4576	
V28	U	0000001C	1	4577	
V29	U	0000001D	1	4578	
V2ADDR	A	0000000C	4	766	317 335 353 371
V2_1	A	000011EC	4	915	936
V2_10	A	00001984	4	1311	1332
V2_11	A	00001A5C	4	1355	1376
V2_12	A	00001B34	4	1399	1420
V2_13	A	00001C0C	4	1443	1464
V2_14	A	00001CE4	4	1488	1509
V2_15	A	00001DBC	4	1532	1553

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V2_16	A	00001E94	4	1576	1597
V2_17	A	00001F6C	4	1620	1641
V2_18	A	00002044	4	1664	1685
V2_19	A	0000211C	4	1708	1729
V2_2	A	000012C4	4	959	980
V2_20	A	000021F4	4	1752	1773
V2_21	A	000022CC	4	1796	1817
V2_22	A	000023A4	4	1841	1862
V2_23	A	0000247C	4	1885	1906
V2_24	A	00002554	4	1935	1956
V2_25	A	0000262C	4	1979	2000
V2_26	A	00002704	4	2023	2044
V2_27	A	000027DC	4	2067	2088
V2_28	A	000028B4	4	2111	2132
V2_29	A	0000298C	4	2155	2176
V2_3	A	0000139C	4	1002	1023
V2_30	A	00002A64	4	2200	2221
V2_31	A	00002B3C	4	2244	2265
V2_32	A	00002C14	4	2288	2309
V2_33	A	00002CEC	4	2332	2353
V2_34	A	00002DC4	4	2376	2397
V2_35	A	00002E9C	4	2420	2441
V2_36	A	00002F74	4	2465	2486
V2_37	A	0000304C	4	2510	2531
V2_38	A	00003124	4	2554	2575
V2_39	A	000031FC	4	2598	2619
V2_4	A	00001474	4	1046	1067
V2_40	A	000032D4	4	2642	2663
V2_41	A	000033AC	4	2692	2713
V2_42	A	00003484	4	2736	2757
V2_43	A	0000355C	4	2780	2801
V2_44	A	00003634	4	2824	2845
V2_45	A	0000370C	4	2868	2889
V2_46	A	000037E4	4	2912	2933
V2_47	A	000038BC	4	2956	2977
V2_48	A	00003994	4	3001	3022
V2_49	A	00003A6C	4	3045	3066
V2_5	A	0000154C	4	1090	1111
V2_50	A	00003B44	4	3089	3110
V2_51	A	00003C1C	4	3133	3154
V2_52	A	00003CF4	4	3177	3198
V2_53	A	00003DCC	4	3221	3242
V2_54	A	00003EA4	4	3265	3286
V2_55	A	00003F7C	4	3310	3331
V2_56	A	00004054	4	3355	3376
V2_57	A	0000412C	4	3399	3420
V2_58	A	00004204	4	3443	3464
V2_59	A	000042DC	4	3487	3508
V2_6	A	00001624	4	1134	1155
V2_60	A	000043B4	4	3532	3553
V2_61	A	0000448C	4	3576	3597
V2_62	A	00004564	4	3620	3641
V2_63	A	0000463C	4	3670	3691
V2_64	A	00004714	4	3714	3735
V2_65	A	000047EC	4	3758	3779
V2_66	A	000048C4	4	3802	3823

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V2_67	A	0000499C	4	3846	3867
V2_68	A	00004A74	4	3890	3911
V2_69	A	00004B4C	4	3935	3956
V2_7	A	000016FC	4	1178	1199
V2_70	A	00004C24	4	3979	4000
V2_71	A	00004CFC	4	4023	4044
V2_72	A	00004DD4	4	4067	4088
V2_73	A	00004EAC	4	4111	4132
V2_74	A	00004F84	4	4155	4176
V2_75	A	0000505C	4	4200	4221
V2_76	A	00005134	4	4245	4266
V2_77	A	0000520C	4	4289	4310
V2_78	A	000052E4	4	4333	4354
V2_79	A	000053BC	4	4377	4398
V2_8	A	000017D4	4	1223	1244
V2_9	A	000018AC	4	1267	1288
V3	U	00000003	1	4552	
V30	U	0000001E	1	4579	
V31	U	0000001F	1	4580	
V4	U	00000004	1	4553	
V5	U	00000005	1	4554	
V6	U	00000006	1	4555	
V7	U	00000007	1	4556	
V8	U	00000008	1	4557	
V9	U	00000009	1	4558	
VXC	X	0000000B	1	765	253 471
VXC1	X	000011EB	1	914	
VXC10	X	00001983	1	1310	
VXC11	X	00001A5B	1	1354	
VXC12	X	00001B33	1	1398	
VXC13	X	00001C0B	1	1442	
VXC14	X	00001CE3	1	1487	
VXC15	X	00001DBB	1	1531	
VXC16	X	00001E93	1	1575	
VXC17	X	00001F6B	1	1619	
VXC18	X	00002043	1	1663	
VXC19	X	0000211B	1	1707	
VXC2	X	000012C3	1	958	
VXC20	X	000021F3	1	1751	
VXC21	X	000022CB	1	1795	
VXC22	X	000023A3	1	1840	
VXC23	X	0000247B	1	1884	
VXC24	X	00002553	1	1934	
VXC25	X	0000262B	1	1978	
VXC26	X	00002703	1	2022	
VXC27	X	000027DB	1	2066	
VXC28	X	000028B3	1	2110	
VXC29	X	0000298B	1	2154	
VXC3	X	0000139B	1	1001	
VXC30	X	00002A63	1	2199	
VXC31	X	00002B3B	1	2243	
VXC32	X	00002C13	1	2287	
VXC33	X	00002CEB	1	2331	
VXC34	X	00002DC3	1	2375	
VXC35	X	00002E9B	1	2419	
VXC36	X	00002F73	1	2464	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
VXC37	X	0000304B	1	2509	
VXC38	X	00003123	1	2553	
VXC39	X	000031FB	1	2597	
VXC4	X	00001473	1	1045	
VXC40	X	000032D3	1	2641	
VXC41	X	000033AB	1	2691	
VXC42	X	00003483	1	2735	
VXC43	X	0000355B	1	2779	
VXC44	X	00003633	1	2823	
VXC45	X	0000370B	1	2867	
VXC46	X	000037E3	1	2911	
VXC47	X	000038BB	1	2955	
VXC48	X	00003993	1	3000	
VXC49	X	00003A6B	1	3044	
VXC5	X	0000154B	1	1089	
VXC50	X	00003B43	1	3088	
VXC51	X	00003C1B	1	3132	
VXC52	X	00003CF3	1	3176	
VXC53	X	00003DCB	1	3220	
VXC54	X	00003EA3	1	3264	
VXC55	X	00003F7B	1	3309	
VXC56	X	00004053	1	3354	
VXC57	X	0000412B	1	3398	
VXC58	X	00004203	1	3442	
VXC59	X	000042DB	1	3486	
VXC6	X	00001623	1	1133	
VXC60	X	000043B3	1	3531	
VXC61	X	0000448B	1	3575	
VXC62	X	00004563	1	3619	
VXC63	X	0000463B	1	3669	
VXC64	X	00004713	1	3713	
VXC65	X	000047EB	1	3757	
VXC66	X	000048C3	1	3801	
VXC67	X	0000499B	1	3845	
VXC68	X	00004A73	1	3889	
VXC69	X	00004B4B	1	3934	
VXC7	X	000016FB	1	1177	
VXC70	X	00004C23	1	3978	
VXC71	X	00004CFB	1	4022	
VXC72	X	00004DD3	1	4066	
VXC73	X	00004EAB	1	4110	
VXC74	X	00004F83	1	4154	
VXC75	X	0000505B	1	4199	
VXC76	X	00005133	1	4244	
VXC77	X	0000520B	1	4288	
VXC78	X	000052E3	1	4332	
VXC79	X	000053BB	1	4376	
VXC8	X	000017D3	1	1222	
VXC9	X	000018AB	1	1266	
VXCMSG	U	00000582	1	458	255
VXCPEXP	C	000010B5	3	693	475
VXCPGOT	C	000010CA	3	696	482
VXCPLINE	C	0000106B	13	688	698 485
VXCPLNG	U	00000063	1	698	484
VXCPNAME	C	0000109C	8	691	468
VXCPNUM	C	00001078	3	689	466

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
WK1	F	00000088	4	781		
WK2	F	0000008C	4	782		
X0001	U	000002C0	1	209	197	210
X1	F	00001270	4	933	907	
X10	F	00001A08	4	1329	1303	
X11	F	00001AE0	4	1373	1347	
X12	F	00001BB8	4	1417	1391	
X13	F	00001C90	4	1461	1435	
X14	F	00001D68	4	1506	1480	
X15	F	00001E40	4	1550	1524	
X16	F	00001F18	4	1594	1568	
X17	F	00001FF0	4	1638	1612	
X18	F	000020C8	4	1682	1656	
X19	F	000021A0	4	1726	1700	
X2	F	00001348	4	977	951	
X20	F	00002278	4	1770	1744	
X21	F	00002350	4	1814	1788	
X22	F	00002428	4	1859	1833	
X23	F	00002500	4	1903	1877	
X24	F	000025D8	4	1953	1927	
X25	F	000026B0	4	1997	1971	
X26	F	00002788	4	2041	2015	
X27	F	00002860	4	2085	2059	
X28	F	00002938	4	2129	2103	
X29	F	00002A10	4	2173	2147	
X3	F	00001420	4	1020	994	
X30	F	00002AE8	4	2218	2192	
X31	F	00002BC0	4	2262	2236	
X32	F	00002C98	4	2306	2280	
X33	F	00002D70	4	2350	2324	
X34	F	00002E48	4	2394	2368	
X35	F	00002F20	4	2438	2412	
X36	F	00002FF8	4	2483	2457	
X37	F	000030D0	4	2528	2502	
X38	F	000031A8	4	2572	2546	
X39	F	00003280	4	2616	2590	
X4	F	000014F8	4	1064	1038	
X40	F	00003358	4	2660	2634	
X41	F	00003430	4	2710	2684	
X42	F	00003508	4	2754	2728	
X43	F	000035E0	4	2798	2772	
X44	F	000036B8	4	2842	2816	
X45	F	00003790	4	2886	2860	
X46	F	00003868	4	2930	2904	
X47	F	00003940	4	2974	2948	
X48	F	00003A18	4	3019	2993	
X49	F	00003AF0	4	3063	3037	
X5	F	000015D0	4	1108	1082	
X50	F	00003BC8	4	3107	3081	
X51	F	00003CA0	4	3151	3125	
X52	F	00003D78	4	3195	3169	
X53	F	00003E50	4	3239	3213	
X54	F	00003F28	4	3283	3257	
X55	F	00004000	4	3328	3302	
X56	F	000040D8	4	3373	3347	
X57	F	000041B0	4	3417	3391	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
X58	F	00004288	4	3461	3435			
X59	F	00004360	4	3505	3479			
X6	F	000016A8	4	1152	1126			
X60	F	00004438	4	3550	3524			
X61	F	00004510	4	3594	3568			
X62	F	000045E8	4	3638	3612			
X63	F	000046C0	4	3688	3662			
X64	F	00004798	4	3732	3706			
X65	F	00004870	4	3776	3750			
X66	F	00004948	4	3820	3794			
X67	F	00004A20	4	3864	3838			
X68	F	00004AF8	4	3908	3882			
X69	F	00004BD0	4	3953	3927			
X7	F	00001780	4	1196	1170			
X70	F	00004CA8	4	3997	3971			
X71	F	00004D80	4	4041	4015			
X72	F	00004E58	4	4085	4059			
X73	F	00004F30	4	4129	4103			
X74	F	00005008	4	4173	4147			
X75	F	000050E0	4	4218	4192			
X76	F	000051B8	4	4263	4237			
X77	F	00005290	4	4307	4281			
X78	F	00005368	4	4351	4325			
X79	F	00005440	4	4395	4369			
X8	F	00001858	4	1241	1215			
X9	F	00001930	4	1285	1259			
XC0001	U	000002E8	1	223	215			
XCFAILMSG	H	0000045C	2	378	319	337	355	373
XCHECK	U	0000033C	1	279	244			
XCO1	X	00001240	16	926				
XCO10	X	000019D8	16	1322				
XCO11	X	00001AB0	16	1366				
XCO12	X	00001B88	16	1410				
XCO13	X	00001C60	16	1454				
XCO14	X	00001D38	16	1499				
XCO15	X	00001E10	16	1543				
XCO16	X	00001EE8	16	1587				
XCO17	X	00001FC0	16	1631				
XCO18	X	00002098	16	1675				
XCO19	X	00002170	16	1719				
XCO2	X	00001318	16	970				
XCO20	X	00002248	16	1763				
XCO21	X	00002320	16	1807				
XCO22	X	000023F8	16	1852				
XCO23	X	000024D0	16	1896				
XCO24	X	000025A8	16	1946				
XCO25	X	00002680	16	1990				
XCO26	X	00002758	16	2034				
XCO27	X	00002830	16	2078				
XCO28	X	00002908	16	2122				
XCO29	X	000029E0	16	2166				
XCO3	X	000013F0	16	1013				
XCO30	X	00002AB8	16	2211				
XCO31	X	00002B90	16	2255				
XCO32	X	00002C68	16	2299				
XCO33	X	00002D40	16	2343				

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES							
XCO34	X	00002E18	16	2387								
XCO35	X	00002EF0	16	2431								
XCO36	X	00002FC8	16	2476								
XCO37	X	000030A0	16	2521								
XCO38	X	00003178	16	2565								
XCO39	X	00003250	16	2609								
XCO4	X	000014C8	16	1057								
XCO40	X	00003328	16	2653								
XCO41	X	00003400	16	2703								
XCO42	X	000034D8	16	2747								
XCO43	X	000035B0	16	2791								
XCO44	X	00003688	16	2835								
XCO45	X	00003760	16	2879								
XCO46	X	00003838	16	2923								
XCO47	X	00003910	16	2967								
XCO48	X	000039E8	16	3012								
XCO49	X	00003AC0	16	3056								
XCO5	X	000015A0	16	1101								
XCO50	X	00003B98	16	3100								
XCO51	X	00003C70	16	3144								
XCO52	X	00003D48	16	3188								
XCO53	X	00003E20	16	3232								
XCO54	X	00003EF8	16	3276								
XCO55	X	00003FD0	16	3321								
XCO56	X	000040A8	16	3366								
XCO57	X	00004180	16	3410								
XCO58	X	00004258	16	3454								
XCO59	X	00004330	16	3498								
XCO6	X	00001678	16	1145								
XCO60	X	00004408	16	3543								
XCO61	X	000044E0	16	3587								
XCO62	X	000045B8	16	3631								
XCO63	X	00004690	16	3681								
XCO64	X	00004768	16	3725								
XCO65	X	00004840	16	3769								
XCO66	X	00004918	16	3813								
XCO67	X	000049F0	16	3857								
XCO68	X	00004AC8	16	3901								
XCO69	X	00004BA0	16	3946								
XCO7	X	00001750	16	1189								
XCO70	X	00004C78	16	3990								
XCO71	X	00004D50	16	4034								
XCO72	X	00004E28	16	4078								
XCO73	X	00004F00	16	4122								
XCO74	X	00004FD8	16	4166								
XCO75	X	000050B0	16	4211								
XCO76	X	00005188	16	4256								
XCO77	X	00005260	16	4300								
XCO78	X	00005338	16	4344								
XCO79	X	00005410	16	4388								
XCO8	X	00001828	16	1234								
XCO9	X	00001900	16	1278								
XCOUTPUT	X	00000060	16	777	312	318	330	336	348	354	366	372
XCPLINE	C	00001116	13	724	733	403						
XCPLNG	U	0000004E	1	733	402							
XCPM3	C	00001156	2	729	392							

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES					
XCPM4	C	00001161	2	731	399					
XCPNAME	C	00001145	8	727	385					
XCPTNUM	C	00001123	3	725	383					
XCR15	F	00000508	8	415	401	405				
XCRESULT	X	000004D8	16	412						
XCSKIP	C	00000007	1	761	281					
XCV1	X	000004E8	16	413						
XCV2	X	000004F8	16	414						
XCVCFN	F	000003F4	4	342	296					
XCVCLFNH	F	000003C0	4	324	293					
XCVCLFNL	F	00000428	4	360	299					
XCVCNF	F	0000038C	4	306	290					
ZVE6TST	J	00000000	21976	134	137	139	143	147	658	135
=A(E6TESTS)	A	000007DC	4	634	229					
=AL2(L'MSGMSG)	R	000007E6	2	637	576					
=CL1'S'	C	000007E8	1	638	281					
=CL8' '	C	000007B0	8	628	288					
=CL8'SKIP XC '	C	000007A8	8	627	280	301				
=CL8'VCFN'	C	000007C8	8	631	295					
=CL8'VCLFNH'	C	000007C0	8	630	292					
=CL8'VCLFNL'	C	000007D0	8	632	298					
=CL8'VCNF'	C	000007B8	8	629	289					
=F'1'	F	000007E0	4	635	407	423	459	526		
=F'4'	F	000007D8	4	633	214					
=H'0'	H	000007E4	2	636	571					

MACRO	DEFN	REFERENCES																
FCHECK	86	196																
PTTABLE	861	4415																
VRR_A	798	904	948	991	1035	1079	1123	1167	1212	1256	1300	1344	1388	1432	1477	1521	1565	1609
		1653	1697	1741	1785	1830	1874	1924	1968	2012	2056	2100	2144	2189	2233	2277	2321	2365
		2409	2454	2499	2543	2587	2631	2681	2725	2769	2813	2857	2901	2945	2990	3034	3078	3122
		3166	3210	3254	3299	3344	3388	3432	3476	3521	3565	3609	3659	3703	3747	3791	3835	3879
		3924	3968	4012	4056	4100	4144	4189	4234	4278	4322	4366						

```
   DESC     SYMBOL   SIZE     POS        ADDR

Entry: 0

Image      IMAGE    21976  0000-55D7  0000-55D7
  Region            21976  0000-55D7  0000-55D7
    CSECT  ZVE6TST  21976  0000-55D7  0000-55D7
```

```
   STMT                        FILE NAME
1     /devstor/sharedvfp/tests/zvector-e6-20-NNPconvert.asm

** NO ERRORS FOUND **
```