```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                     2 ************************************************************************
                                                     3 *
                                                     4 *        EXPERIMENTAL pending further PoP definition
                                                     5 *
                                                     6 *        Zvector E6 instruction tests for VRR-c encoded:
                                                     7 *
                                                     8 *        E675  VCRNF   - VECTOR FP CONVERT AND ROUND TO NNP
                                                     9 *
                                                    10 *        and partial testing of
                                                    11 *
                                                    12 *        E656 VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                    13 *        E65E VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                    14 *
                                                    15 *        during cross check tests for VCRNF
                                                    16 *
                                                    17 *        James Wekel August 2024
                                                    18 ************************************************************************


                                                    20 ************************************************************************
                                                    21 *
                                                    22 *        basic instruction tests
                                                    23 *
                                                    24 ************************************************************************
                                                    25 *  This program tests EXPERIMENTAL functioning of the z/arch E6 VRR-c
                                                    26 *  Neural-network-processing-assist facility vector instructions.
                                                    27 *  These test are EXPERIMENTAL pending further PoP definition of
                                                    28 *  NNP-data-type-1.
                                                    29 *
                                                    30 *  If requested and if VXC == 0 after test instruction execution,
                                                    31 *  a cross check test is performed. A cross check uses the result
                                                    32 *  of the instruction test to recreate the test source.
                                                    33 *
                                                    34 *  Exceptions (including trapable IEEE exceptions) are not tested.
                                                    35 *
                                                    36 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                    37 *  obvious coding errors.  None of the tests are thorough.  They are
                                                    38 *  NOT designed to test all aspects of any of the instructions.
                                                    39 *
                                                    40 ************************************************************************
                                                    41 *
                                                    42 *   *Testcase zvector-e6-21-VCRNF
                                                    43 *   *
                                                    44 *   *        EXPERIMENTAL pending further PoP definition
                                                    45 *   *
                                                    46 *   *        Zvector E6 instruction tests for VRR-c encoded:
                                                    47 *   *
                                                    48 *   *        E675 VCRNF   - VECTOR FP CONVERT AND ROUND TO NNP
                                                    49 *   *
                                                    50 *   *        # -------------------------------------------------------
                                                    51 *   *        #  This tests only the basic function of the instruction.
                                                    52 *   *        #  Exceptions are NOT tested.
                                                    53 *   *        # -------------------------------------------------------
                                                    54 *   *
                                                    55 *   mainsize    2
                                                    56 *   numcpu      1
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

                                                     57 *   sysclear
                                                     58 *   archlvl     z/Arch
                                                     59 *
                                                     60 *   loadcore    "$(testpath)/zvector-e6-21-VCRNF.core" 0x0
                                                     61 *
                                                     62 *   diag8cmd    enable    # (needed for messages to Hercules console)
                                                     63 *   runtest 5
                                                     64 *   diag8cmd    disable   # (reset back to default)
                                                     65 *
                                                     66 *   *Done
                                                     67 *
                                                     68 ******************************************************************************
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   70 ************************************************************************
                                                   71 *        FCHECK Macro - Is a Facility Bit set?
                                                   72 *
                                                   73 *        If the facility bit is NOT set, an message is issued and
                                                   74 *        the test is skipped.
                                                   75 *
                                                   76 *        Fcheck uses R0, R1 and R2
                                                   77 *
                                                   78 * eg.    FCHECK 134,'vector-packed-decimal'
                                                   79 ************************************************************************
                                                   80         MACRO
                                                   81         FCHECK &BITNO,&NOTSETMSG
                                                   82 .*                        &BITNO : facility bit number to check
                                                   83 .*                        &NOTSETMSG : 'facility name'
                                                   84         LCLA  &FBBYTE           Facility bit in Byte
                                                   85         LCLA  &FBBIT            Facility bit within Byte
                                                   86
                                                   87         LCLA  &L(8)
                                                   88 &L(1)   SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                   89
                                                   90 &FBBYTE SETA  &BITNO/8
                                                   91 &FBBIT  SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                   92 .*      MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                   93
                                                   94         B     X&SYSNDX
                                                   95 *                                       Fcheck data area
                                                   96 *                                       skip messgae
                                                   97 SKT&SYSNDX DC  C'          Skipping tests: '
                                                   98         DC    C&NOTSETMSG
                                                   99         DC    C' facility (bit &BITNO) is not installed.'
                                                  100 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                  101 *                                       facility bits
                                                  102         DS    FD                       gap
                                                  103 FB&SYSNDX DS   4FD
                                                  104         DS    FD                       gap
                                                  105 *
                                                  106 X&SYSNDX EQU *
                                                  107         LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                  108         STFLE FB&SYSNDX                get facility bits
                                                  109
                                                  110         XGR   R0,R0
                                                  111         IC    R0,FB&SYSNDX+&FBBYTE     get fbit byte
                                                  112         N     R0,=F'&FBBIT'            is bit set?
                                                  113         BNZ   XC&SYSNDX
                                                  114 *
                                                  115 * facility bit not set, issue message and exit
                                                  116 *
                                                  117         LA    R0,SKL&SYSNDX            message length
                                                  118         LA    R1,SKT&SYSNDX            message address
                                                  119         BAL   R2,MSG
                                                  120
                                                  121         B     EOJ
                                                  122 XC&SYSNDX EQU *
                                                  123         MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   125 ************************************************************************
                                                   126 *        Low core PSWs
                                                   127 ************************************************************************


                             00000000  00002D83   129 ZVE6TST  START 0
00000000                     00000000              130          USING ZVE6TST,R0            Low core addressability
                                                   131
                             00000140  00000000   132 SVOLDPSW EQU   ZVE6TST+X'140'        z/Arch Supervisor call old PSW


00000000                     00000000  000001A0   134          ORG   ZVE6TST+X'1A0'        z/Architecture RESTART PSW
000001A0  00000001 80000000                        135          DC    X'0000000180000000'
000001A8  00000000 00000200                        136          DC    AD(BEGIN)


000001B0                     000001B0  000001D0   138          ORG   ZVE6TST+X'1D0'        z/Architecture PROGRAM CHECK PSW
000001D0  00020001 80000000                        139          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                        140          DC    AD(X'DEAD')


000001E0                     000001E0  00000200   142          ORG   ZVE6TST+X'200'        Start of actual test program...
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    144
                                                    145 ************************************************************************
                                                    146 *                The actual "ZVE6TST" program itself...
                                                    147 ************************************************************************
                                                    148 *
                                                    149 *  Architecture Mode: z/Arch
                                                    150 *  Register Usage:
                                                    151 *
                                                    152 *   R0       (work)
                                                    153 *   R1-4     (work)
                                                    154 *   R5       Testing control table - current test base
                                                    155 *   R6       (work)
                                                    156 *   R7       msg return
                                                    157 *   R8       First base register
                                                    158 *   R9       Second base register
                                                    159 *   R10      Third base register
                                                    160 *   R11      E6TEST call return
                                                    161 *   R12      E6TESTS register
                                                    162 *   R13      (work)
                                                    163 *   R14      Subroutine call
                                                    164 *   R15      Secondary Subroutine call or work
                                                    165 *
                                                    166 ************************************************************************

00000200                       00000200             168          USING  BEGIN,R8               FIRST Base Register
00000200                       00001200             169          USING  BEGIN+4096,R9          SECOND Base Register
00000200                       00002200             170          USING  BEGIN+8192,R10         THIRD Base Register
                                                    171
00000200  0580                                      172 BEGIN    BALR   R8,0                   Initialize FIRST base register
00000202  0680                                      173          BCTR   R8,0                   Initialize FIRST base register
00000204  0680                                      174          BCTR   R8,0                   Initialize FIRST base register
                                                    175
00000206  4190 8800                     00000800    176          LA     R9,2048(,R8)           Initialize SECOND base register
0000020A  4190 9800                     00000800    177          LA     R9,2048(,R9)           Initialize SECOND base register
                                                    178
0000020E  41A0 9800                     00000800    179          LA     R10,2048(,R9)          Initialize THIRD base register
00000212  41A0 A800                     00000800    180          LA     R10,2048(,R10)         Initialize THIRD base register
                                                    181
00000216  B600 8524                     00000724    182          STCTL  R0,R0,CTLR0            Store CR0 to enable AFP
0000021A  9604 8525                     00000725    183          OI     CTLR0+1,X'04'          Turn on AFP bit
0000021E  9602 8525                     00000725    184          OI     CTLR0+1,X'02'          Turn on Vector bit
00000222  B700 8524                     00000724    185          LCTL   R0,R0,CTLR0            Reload updated CR0
                                                    186
                                                    187 ************************************************************************
                                                    188 * Is Neural-network-processing-assist facility 2 installed  (bit 165)
                                                    189 ************************************************************************
                                                    190
                                                    191          FCHECK 165,'Neural-network-processing-assist'
00000226  47F0 80C0                     000002C0    192+         B      X0001
                                                    193+*                                     Fcheck data area
                                                    194+*                                     skip messgae
0000022A  40404040 40404040                         195+SKT0001  DC     C'          Skipping tests: '
00000244  D585A499 81936095                         196+         DC     C'Neural-network-processing-assist'
00000264  40868183 899389A3                         197+         DC     C' facility (bit 165) is not installed.'
                               0000005F  00000001   198+SKL0001  EQU    *-SKT0001
                                                    199+*                                     facility bits
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00000290  00000000 00000000                        200+         DS    FD                      gap
00000298  00000000 00000000                        201+FB0001   DS    4FD
000002B8  00000000 00000000                        202+         DS    FD                      gap
                                                   203+*
                             000002C0  00000001    204+X0001    EQU   *
000002C0  4100 0004                    00000004    205+         LA    R0,((X0001-FB0001)/8)-1
000002C4  B2B0 8098                    00000298    206+         STFLE FB0001                  get facility bits
000002C8  B982 0000                                207+         XGR   R0,R0
000002CC  4300 80AC                    000002AC    208+         IC    R0,FB0001+20            get fbit byte
000002D0  5400 8548                    00000748    209+         N     R0,=F'4'                is bit set?
000002D4  4770 80E8                    000002E8    210+         BNZ   XC0001
                                                   211+*
                                                   212+* facility bit not set, issue message and exit
                                                   213+*
000002D8  4100 005F                    0000005F    214+         LA    R0,SKL0001              message length
000002DC  4110 802A                    0000022A    215+         LA    R1,SKT0001              message address
000002E0  4520 8438                    00000638    216+         BAL   R2,MSG
000002E4  47F0 8508                    00000708    217+         B     EOJ
                             000002E8  00000001    218+XC0001   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   220 ***********************************************************************
                                                   221 *               Do tests in the E6TESTS table
                                                   222 ***********************************************************************
                                                   223
000002E8  58C0 854C                      0000074C  224          L     R12,=A(E6TESTS)        get table of test addresses
                                                   225
                                 000002EC  00000001 226 NEXTE6   EQU   *
000002EC  5850 C000                      00000000  227          L     R5,0(0,R12)            get test address
000002F0  1255                                     228          LTR   R5,R5                     have a test?
000002F2  4780 83F4                      000005F4  229          BZ    ENDTEST                      done?
                                                   230
000002F6                         00000000          231          USING E6TEST,R5
                                                   232
000002F6  4800 5004                      00000004  233          LH    R0,TNUM                save current test number
000002FA  5000 8E04                      00001004  234          ST    R0,TESTING             for easy reference
                                                   235
000002FE  58B0 5000                      00000000  236          L     R11,TSUB               get address of test routine
00000302  05BB                                     237          BALR  R11,R11                do test
                                                   238
00000304  45F0 814E                      0000034E  239          BAL   R15,XCHECK
                                                   240 *
                                                   241 * validate FPC first
                                                   242 *
00000308  D500 500A 5041                 00000041  243          CLC   FLG(1),FPC_R+1          expected FPC flags?
0000030E  4780 8116                      00000316  244          BE    CHECKVXC
00000312  4570 8290                      00000490  245          BAL   R7,FPCMSG               no, issue failed message
                                                   246
                                 00000316  00000001 247 CHECKVXC EQU   *
00000316  D500 500B 5042                 00000042  248          CLC   VXC(1),FPC_R+2          expected VXC?
0000031C  4780 8124                      00000324  249          BE    CHECKRES
00000320  4570 8302                      00000502  250          BAL   R7,VXCMSG               no, issue failed message
                                                   251
                                 00000324  00000001 252 CHECKRES EQU   *
                                                   253
                                                   254 * then validate results, if not inexact
                                                   255
00000324  B982 0011                                256          XGR   R1,R1
00000328  4310 5041                      00000041  257          IC    R1,FPC_R+1             FPC flags
0000032C  5410 8550                      00000750  258          N     R1,=XL4'00000008'      check inexact flag
00000330  1211                                     259          LTR   R1,R1
00000332  4770 8146                      00000346  260          BNZ   DONEXT
                                                   261
00000336  E310 501C 0014                 0000001C  262          LGF   R1,READDR              expected result address
0000033C  D50F 5028 1000         00000028 00000000 263          CLC   V1OUTPUT,0(R1)
00000342  4770 8374                      00000574  264          BNE   FAILMSG                no, issue failed message
                                                   265
                                 00000346  00000001 266 DONEXT   EQU   *
00000346  41C0 C004                      00000004  267          LA    R12,4(0,R12)           next test address
0000034A  47F0 80EC                      000002EC  268          B     NEXTE6
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   270 *-----------------------------------------------------------------------
                                                   271 * cross check that the result can be converted back to the source
                                                   272 * where there were NO exceptions (DXC/VXC = 0)
                                                   273 *-----------------------------------------------------------------------
                                0000034E  00000001 274 XCHECK   EQU   *
0000034E  D207 5050 8530        00000050  00000730 275          MVC   SKIPXC,=CL8'SKIP XC '
00000354  D500 5007 855C        00000007  0000075C 276          CLC   XCSKIP,=CL1'S'          skip xcheck requested
0000035A  478F 0000                       00000000 277          BE    0(R15)                    skip = S, so exit
0000035E  9500 5042                       00000042 278          CLI   FPC_R+2,0               Only Xcheck no VXC error
00000362  477F 0000                       00000000 279          BNZ   0(R15)                    some VXC error , so exit
                                                   280 *
                                                   281 *        cross check depends on the instruction
                                                   282 *
00000366  D207 5050 8538        00000050  00000738 283          MVC   SKIPXC,=CL8'        '
0000036C  D507 5010 8540        00000010  00000740 284          CLC   OPNAME,=CL8'VCRNF'
00000372  4780 8180                       00000380 285          BE    XCVCRNF
                                                   286
                                                   287
00000376  D207 5050 8530        00000050  00000730 288          MVC   SKIPXC,=CL8'SKIP XC '
0000037C  07FF                                     289          BR    R15                     return from xcheck
                                                   290
                                                   291 * cross check: VCRNF   - VECTOR FP CONVERT AND ROUND TO NNP
                                                   292 *
00000380                                           293 XCVCRNF  DS    0F
00000380  B29D 852C                       0000072C 294          LFPC  FPCINIT                 initialize FPC
                                                   295
00000384  E700 5028 0806                  00000028 296          VL    V16,V1OUTPUT
0000038A  E6F0 0000 2456                           297          VCLFNH V15,V16,2,0
00000390  B29C 5088                       00000088 298          STFPC FPC_XC1                 save 1st FPC
00000394  E7F0 5060 000E                  00000060 299          VST   V15,XCOUTPUT
                                                   300
0000039A  B29D 852C                       0000072C 301          LFPC  FPCINIT                 initialize FPC
                                                   302
0000039E  E700 5028 0806                  00000028 303          VL    V16,V1OUTPUT
000003A4  E6F0 0000 245E                           304          VCLFNL V15,V16,2,0
000003AA  B29C 508C                       0000008C 305          STFPC FPC_XC2                 save 2nd FPC
000003AE  E7F0 5070 000E                  00000070 306          VST   V15,XCOUTPUT+16
                                                   307
000003B4  9500 508A                       0000008A 308          CLI   FPC_XC1+2,0             1st FPC
000003B8  477F 0000                       00000000 309          BNZ   0(R15)                  some VXC error , so exit
                                                   310
000003BC  9500 508E                       0000008E 311          CLI   FPC_XC2+2,0             2nd FPC
000003C0  477F 0000                       00000000 312          BNZ   0(R15)                  some VXC error , so exit
                                                   313
000003C4  E310 500C 0014                  0000000C 314          LGF   R1,V2ADDR               expected source address
000003CA  D51F 5060 1000                  00000000 315          CLC   XCOUTPUT(32),0(R1)
000003D0  4770 81D6                       000003D6 316          BNE   XCFAILMSG
000003D4  07FF                                     317          BR    R15                     return from xcheck
                                                   318
                                                   319
                                                   320 * xcheck failed message
000003D6                                           321 XCFAILMSG DS   0H
000003D6  5800 8554                       00000754 322          L     R0,=F'1'                set failed test indicator
000003DA  5000 8E00                       00001000 323          ST    R0,FAILED
                                                   324
000003DE  4820 5004                       00000004 325          LH    R2,TNUM                 get test number and convert
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000003E2  4E20 8F90                     00001190   326          CVD   R2,DECNUM
000003E6  D211 8F7A 8F64      0000117A  00001164   327          MVC   PRT3,EDIT
000003EC  DE11 8F7A 8F90      0000117A  00001190   328          ED    PRT3,DECNUM
000003F2  D202 8F23 8F87      00001123  00001187   329          MVC   XCPTNUM(3),PRT3+13     fill in message with test #
                                                   330
000003F8  D207 8F45 5010      00001145  00000010   331          MVC   XCPNAME,OPNAME         fill in message with instruction
                                                   332
000003FE  B982 0022                                333          XGR   R2,R2
00000402  4320 5008                     00000008   334          IC    R2,M4                  get m3 and convert
00000406  4E20 8F90                     00001190   335          CVD   R2,DECNUM
0000040A  D211 8F7A 8F64      0000117A  00001164   336          MVC   PRT3,EDIT
00000410  DE11 8F7A 8F90      0000117A  00001190   337          ED    PRT3,DECNUM
00000416  D201 8F56 8F88      00001156  00001188   338          MVC   XCPM4(2),PRT3+14       fill in message with m3 field
                                                   339 *
0000041C  B982 0022                                340          XGR   R2,R2
00000420  4320 5009                     00000009   341          IC    R2,M5                  get m4 and convert
00000424  4E20 8F90                     00001190   342          CVD   R2,DECNUM
00000428  D211 8F7A 8F64      0000117A  00001164   343          MVC   PRT3,EDIT
0000042E  DE11 8F7A 8F90      0000117A  00001190   344          ED    PRT3,DECNUM
00000434  D201 8F61 8F88      00001161  00001188   345          MVC   XCPM5(2),PRT3+14       fill in message with m4 field
                                                   346
0000043A  50F0 8288                     00000488   347          ST    R15,XCR15              save r15
0000043E  4100 004E                     0000004E   348          LA    R0,XCPLNG              message length
00000442  4110 8F16                     00001116   349          LA    R1,XCPLINE             message address
00000446  45F0 8402                     00000602   350          BAL   R15,RPTERROR
0000044A  58F0 8288                     00000488   351          L     R15,XCR15
                                                   352
0000044E  5800 8554                     00000754   353          L     R0,=F'1'               set failed test indicator
00000452  5000 8E00                     00001000   354          ST    R0,FAILED
00000456  07FF                                     355          BR    R15                    return from xcheck
                                                   356
00000458                                           357          DS    0FD
00000458  00000000 00000000                        358 XCRESULT DS    XL16
00000468  00000000 00000000                        359 XCV1     DS    XL16
00000478  00000000 00000000                        360 XCV2     DS    XL16
00000488  00000000 00000000                        361 XCR15    DS    FD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   363 ***********************************************************************
                                                   364 * FPC not as expected:
                                                   365 *        issue message with test number, instruction under test,
                                                   366 *              expected FPC and received FPC
                                                   367 ***********************************************************************
                                00000490  00000001  368 FPCMSG   EQU   *
00000490  5800 8554                         00000754  369          L     R0,=F'1'                 set failed test indicator
00000494  5000 8E00                         00001000  370          ST    R0,FAILED
                                                   371
00000498  4820 5004                         00000004  372          LH    R2,TNUM                  get test number and convert
0000049C  4E20 8F90                         00001190  373          CVD   R2,DECNUM
000004A0  D211 8F7A 8F64        0000117A    00001164  374          MVC   PRT3,EDIT
000004A6  DE11 8F7A 8F90        0000117A    00001190  375          ED    PRT3,DECNUM
000004AC  D202 8E15 8F87        00001015    00001187  376          MVC   FPCPNUM(3),PRT3+13       fill in message with test #
                                                   377
000004B2  D207 8E39 5010        00001039    00000010  378          MVC   FPCPNAME,OPNAME          fill in message with instruction
                                                   379 *
000004B8  B982 0022                                380          XGR   R2,R2
000004BC  4320 500A                         0000000A  381          IC    R2,FLG                   get expected flags and convert
000004C0  4E20 8F90                         00001190  382          CVD   R2,DECNUM
000004C4  D211 8F7A 8F64        0000117A    00001164  383          MVC   PRT3,EDIT
000004CA  DE11 8F7A 8F90        0000117A    00001190  384          ED    PRT3,DECNUM
000004D0  D202 8E52 8F87        00001052    00001187  385          MVC   FPCPEXP(3),PRT3+13       fill in message with m3 field
                                                   386 *
000004D6  B982 0022                                387          XGR   R2,R2
000004DA  4320 5041                         00000041  388          IC    R2,FPC_R+1               get received flags and convert
000004DE  4E20 8F90                         00001190  389          CVD   R2,DECNUM
000004E2  D211 8F7A 8F64        0000117A    00001164  390          MVC   PRT3,EDIT
000004E8  DE11 8F7A 8F90        0000117A    00001190  391          ED    PRT3,DECNUM
000004EE  D202 8E67 8F87        00001067    00001187  392          MVC   FPCPGOT(3),PRT3+13       fill in message with FPC got
                                                   393 *
000004F4  4100 0063                         00000063  394          LA    R0,FPCPLNG               message length
000004F8  4110 8E08                         00001008  395          LA    R1,FPCPLINE              message address
000004FC  45F0 8402                         00000602  396          BAL   R15,RPTERROR
00000500  07F7                                     397          BR    R7
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   399 ***********************************************************************
                                                   400 * VXC not as expected:
                                                   401 *        issue message with test number, instruction under test,
                                                   402 *               expected FPC and received FPC
                                                   403 ***********************************************************************
                                 00000502  00000001  404 VXCMSG   EQU   *
00000502  5800 8554                        00000754  405          L     R0,=F'1'                set failed test indicator
00000506  5000 8E00                        00001000  406          ST    R0,FAILED
                                                   407
0000050A  4820 5004                        00000004  408          LH    R2,TNUM                 get test number and convert
0000050E  4E20 8F90                        00001190  409          CVD   R2,DECNUM
00000512  D211 8F7A 8F64         0000117A  00001164  410          MVC   PRT3,EDIT
00000518  DE11 8F7A 8F90         0000117A  00001190  411          ED    PRT3,DECNUM
0000051E  D202 8E78 8F87         00001078  00001187  412          MVC   VXCPNUM(3),PRT3+13      fill in message with test #
                                                   413
00000524  D207 8E9C 5010         0000109C  00000010  414          MVC   VXCPNAME,OPNAME         fill in message with instruction
                                                   415 *
0000052A  B982 0022                                416          XGR   R2,R2
0000052E  4320 500B                        0000000B  417          IC    R2,VXC                  get expected flags and convert
00000532  4E20 8F90                        00001190  418          CVD   R2,DECNUM
00000536  D211 8F7A 8F64         0000117A  00001164  419          MVC   PRT3,EDIT
0000053C  DE11 8F7A 8F90         0000117A  00001190  420          ED    PRT3,DECNUM
00000542  D202 8EB5 8F87         000010B5  00001187  421          MVC   VXCPEXP(3),PRT3+13      fill in message with m3 field
                                                   422 *
00000548  B982 0022                                423          XGR   R2,R2
0000054C  4320 5042                        00000042  424          IC    R2,FPC_R+2              get received flags and convert
00000550  4E20 8F90                        00001190  425          CVD   R2,DECNUM
00000554  D211 8F7A 8F64         0000117A  00001164  426          MVC   PRT3,EDIT
0000055A  DE11 8F7A 8F90         0000117A  00001190  427          ED    PRT3,DECNUM
00000560  D202 8ECA 8F87         000010CA  00001187  428          MVC   VXCPGOT(3),PRT3+13      fill in message with FPC got
                                                   429 *
00000566  4100 0063                        00000063  430          LA    R0,VXCPLNG              message length
0000056A  4110 8E6B                        0000106B  431          LA    R1,VXCPLINE             message address
0000056E  45F0 8402                        00000602  432          BAL   R15,RPTERROR
00000572  07F7                                     433          BR    R7
                                                   434
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   436 ***********************************************************************
                                                   437 * result not as expected:
                                                   438 *        issue message with test number, instruction under test
                                                   439 *               and instruction m4
                                                   440 ***********************************************************************
                             00000574  00000001    441 FAILMSG  EQU   *
00000574  5800 8554                    00000754    442          L     R0,=F'1'                set failed test indicator
00000578  5000 8E00                    00001000    443          ST    R0,FAILED
                                                   444
0000057C  4820 5004                    00000004    445          LH    R2,TNUM                 get test number and convert
00000580  4E20 8F90                    00001190    446          CVD   R2,DECNUM
00000584  D211 8F7A 8F64               0000117A    447          MVC   PRT3,EDIT
0000058A  DE11 8F7A 8F90               0000117A    448          ED    PRT3,DECNUM
00000590  D202 8EDB 8F87               000010DB    449          MVC   PRTNUM(3),PRT3+13       fill in message with test #
                                                   450
00000596  D207 8EF6 5010               000010F6    451          MVC   PRTNAME,OPNAME          fill in message with instruction
                                                   452 *
0000059C  B982 0022                                453          XGR   R2,R2
000005A0  4320 5008                    00000008    454          IC    R2,M4                   get m3 and convert
000005A4  4E20 8F90                    00001190    455          CVD   R2,DECNUM
000005A8  D211 8F7A 8F64               0000117A    456          MVC   PRT3,EDIT
000005AE  DE11 8F7A 8F90               0000117A    457          ED    PRT3,DECNUM
000005B4  D201 8F07 8F88               00001107    458          MVC   PRTM4(2),PRT3+14        fill in message with m3 field
                                                   459 *
000005BA  B982 0022                                460          XGR   R2,R2
000005BE  4320 5009                    00000009    461          IC    R2,M5                   get m4 and convert
000005C2  4E20 8F90                    00001190    462          CVD   R2,DECNUM
000005C6  D211 8F7A 8F64               0000117A    463          MVC   PRT3,EDIT
000005CC  DE11 8F7A 8F90               0000117A    464          ED    PRT3,DECNUM
000005D2  D201 8F13 8F88               00001113    465          MVC   PRTM5(2),PRT3+14        fill in message with m4 field
                                                   466 *
000005D8  4100 0048                    00000048    467          LA    R0,PRTLNG               message length
000005DC  4110 8ECE                    000010CE    468          LA    R1,PRTLINE              message address
000005E0  45F0 8402                    00000602    469          BAL   R15,RPTERROR


                                                   471 ***********************************************************************
                                                   472 * continue after a failed test
                                                   473 ***********************************************************************
                             000005E4  00000001    474 FAILCONT EQU   *
000005E4  5800 8554                    00000754    475          L     R0,=F'1'                set failed test indicator
000005E8  5000 8E00                    00001000    476          ST    R0,FAILED
                                                   477
000005EC  41C0 C004                    00000004    478          LA    R12,4(0,R12)            next test address
000005F0  47F0 80EC                    000002EC    479          B     NEXTE6


                                                   481 ***********************************************************************
                                                   482 * end of testing; set ending psw
                                                   483 ***********************************************************************
                             000005F4  00000001    484 ENDTEST  EQU   *
000005F4  5810 8E00                    00001000    485          L     R1,FAILED               did a test fail?
000005F8  1211                                     486          LTR   R1,R1
000005FA  4780 8508                    00000708    487          BZ    EOJ                      No, exit
000005FE  47F0 8520                    00000720    488          B     FAILTEST                 Yes, exit with BAD PSW
                                                   489
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   491 ***********************************************************************
                                                   492 *        RPTERROR          Report instruction test in error
                                                   493 *                              R0 = MESSGAE LENGTH
                                                   494 *                              R1 = ADDRESS OF MESSAGE
                                                   495 ***********************************************************************

00000602  50F0 8420                     00000620   497 RPTERROR ST    R15,RPTSAVE            Save return address
00000606  5050 8424                     00000624   498          ST    R5,RPTSVR5             Save R5
                                                   499 *
                                                   500 *        Use Hercules Diagnose for Message to console
                                                   501 *
0000060A  9002 8428                     00000628   502          STM   R0,R2,RPTDWSAV         save regs used by MSG
0000060E  4520 8438                     00000638   503          BAL   R2,MSG                 call Hercules console MSG display
00000612  9802 8428                     00000628   504          LM    R0,R2,RPTDWSAV         restore regs


00000616  5850 8424                     00000624   506          L     R5,RPTSVR5             Restore R5
0000061A  58F0 8420                     00000620   507          L     R15,RPTSAVE            Restore return address
0000061E  07FF                                     508          BR    R15                    Return to caller

00000620  00000000                                 510 RPTSAVE  DC    F'0'                   R15 save area
00000624  00000000                                 511 RPTSVR5  DC    F'0'                   R5 save area

00000628  00000000 00000000                        513 RPTDWSAV DC    2D'0'                  R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   515 ************************************************************************
                                                   516 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                   517 *              R2 = return address
                                                   518 ************************************************************************

00000638  4900 8558                     00000758   520 MSG      CH    R0,=H'0'                Do we even HAVE a message?
0000063C  07D2                                     521          BNHR  R2                      No, ignore

0000063E  9002 8474                     00000674   523          STM   R0,R2,MSGSAVE           Save registers

00000642  4900 855A                     0000075A   525          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
00000646  47D0 844E                     0000064E   526          BNH   MSGOK                   Yes, continue
0000064A  4100 0064                     00000064   527          LA    R0,L'MSGMSG             No, set to maximum

0000064E  1820                                     529 MSGOK    LR    R2,R0                   Copy length to work register
00000650  0620                                     530          BCTR  R2,0                    Minus-1 for execute
00000652  4420 8480                     00000680   531          EX    R2,MSGMVC               Copy message to O/P buffer

00000656  4120 200A                     0000000A   533          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
0000065A  4110 8486                     00000686   534          LA    R1,MSGCMD               Point to true command

0000065E  83120008                                 536          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
00000662  4780 846E                     0000066E   537          BZ    MSGRET                  Return if successful
                                                   538
00000666  1222                                     539          LTR   R2,R2                   Is Diag8 Ry (R2) 0?
00000668  4780 846E                     0000066E   540          BZ    MSGRET                    an error occurred but coninue
                                                   541
0000066C  0000                                     542          DC    H'0'                    CRASH for debugging purposes

0000066E  9802 8474                     00000674   544 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
00000672  07F2                                     545          BR    R2                      Return to caller


00000674  00000000 00000000                        547 MSGSAVE  DC    3F'0'                   Registers save area
00000680  D200 848F 1000      0000068F  00000000   548 MSGMVC   MVC   MSGMSG(0),0(R1)          Executed instruction

00000686  D4E2C7D5 D6C8405C                        550 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
0000068F  40404040 40404040                        551 MSGMSG   DC    CL100' '                 The message text to be displayed
                                                   552
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   554 ************************************************************************
                                                   555 *        Normal completion or Abnormal termination PSWs
                                                   556 ************************************************************************


000006F8  00020001 80000000                        558 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000708  B2B2 84F8                     000006F8   560 EOJ      LPSWE EOJPSW                 Normal completion


00000710  00020001 80000000                        562 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

00000720  B2B2 8510                     00000710   564 FAILTEST LPSWE FAILPSW                Abnormal termination


                                                   566 ************************************************************************
                                                   567 *        Working Storage
                                                   568 ************************************************************************


00000724  00000000                                 570 CTLR0    DS    F                      CR0
00000728  00000000                                 571          DS    F
0000072C  00000000                                 572 FPCINIT  DC    XL4'00000000'          FPC before test


                                                   574
00000730                                           575          LTORG ,                Literals pool
00000730  E2D2C9D7 40E7C340                        576                =CL8'SKIP XC '
00000738  40404040 40404040                        577                =CL8'        '
00000740  E5C3D9D5 C6404040                        578                =CL8'VCRNF'
00000748  00000004                                 579                =F'4'
0000074C  00002D04                                 580                =A(E6TESTS)
00000750  00000008                                 581                =XL4'00000008'
00000754  00000001                                 582                =F'1'
00000758  0000                                     583                =H'0'
0000075A  0064                                     584                =AL2(L'MSGMSG)
0000075C  E2                                       585                =CL1'S'
                                                   586
                                                   587 *        some constants
                                                   588
                             00000400  00000001    589 K        EQU   1024             One KB
                             00001000  00000001    590 PAGE     EQU   (4*K)            Size of one page
                             00010000  00000001    591 K64      EQU   (64*K)           64 KB
                             00100000  00000001    592 MB       EQU   (K*K)             1 MB
                                                   593
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   594
                              AABBCCDD  00000001   595 REG2PATT EQU   X'AABBCCDD'    Polluted Register pattern
                              000000DD  00000001   596 REG2LOW  EQU         X'DD'    (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   598 *=====================================================================
                                                   599 *
                                                   600 *  NOTE: start data on an address that is easy to display
                                                   601 *        within Hercules
                                                   602 *
                                                   603 *=====================================================================
                                                   604
0000075D                      0000075D  00001000   605          ORG   ZVE6TST+X'1000'
00001000  00000000                                 606 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                 607 TESTING  DC    F'0'                    current test #


                                                   609
                                                   610 ************************************************************************
                                                   611 *        TEST failed : FPC message
                                                   612 ************************************************************************
                                                   613 *
                                                   614 *        failed message and associated editting
                                                   615 *
00001008  40404040 4040E385                        616 FPCPLINE DC    C'      Test # '
00001015  A7A7A7                                   617 FPCPNUM  DC    C'xxx'
00001018  40A69996 958740C6                        618          DC    c' wrong FPC flags for instruction '
00001039  A7A7A7A7 A7A7A7A7                        619 FPCPNAME DC    CL8'xxxxxxxx'
00001041  4085A797 8583A385                        620          DC    C' expected: flags='
00001052  A7A7A7                                   621 FPCPEXP  DC    C'xxx'
00001055  6B                                       622          DC    C','
00001056  40998583 8589A585                        623          DC    C' received: flags='
00001067  A7A7A7                                   624 FPCPGOT  DC    C'xxx'
0000106A  4B                                       625          DC    C'.'
                              00000063  00000001   626 FPCPLNG  EQU   *-FPCPLINE


                                                   628
                                                   629 ************************************************************************
                                                   630 *        TEST failed : VXC message
                                                   631 ************************************************************************
                                                   632 *
                                                   633 *        failed message and associated editting
                                                   634 *
0000106B  40404040 4040E385                        635 VXCPLINE DC    C'      Test # '
00001078  A7A7A7                                   636 VXCPNUM  DC    C'xxx'
0000107B  40A69996 958740C6                        637          DC    c' wrong FPC VXC   for instruction '
0000109C  A7A7A7A7 A7A7A7A7                        638 VXCPNAME DC    CL8'xxxxxxxx'
000010A4  4085A797 8583A385                        639          DC    C' expected:   VXC='
000010B5  A7A7A7                                   640 VXCPEXP  DC    C'xxx'
000010B8  6B                                       641          DC    C','
000010B9  40998583 8589A585                        642          DC    C' received:   VXC='
000010CA  A7A7A7                                   643 VXCPGOT  DC    C'xxx'
000010CD  4B                                       644          DC    C'.'
                              00000063  00000001   645 VXCPLNG  EQU   *-VXCPLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    647
                                                    648 ***********************************************************************
                                                    649 *        TEST failed : result messgae
                                                    650 ***********************************************************************
                                                    651 *
                                                    652 *        failed message and associated editting
                                                    653 *
000010CE  40404040 4040E385                         654 PRTLINE  DC    C'      Test # '
000010DB  A7A7A7                                    655 PRTNUM   DC    C'xxx'
000010DE  40868189 93858440                         656          DC    c' failed for instruction '
000010F6  A7A7A7A7 A7A7A7A7                         657 PRTNAME  DC    CL8'xxxxxxxx'
000010FE  40A689A3 884094F4                         658          DC    C' with m4='
00001107  A7A7                                      659 PRTM4    DC    C'xx'
00001109  6B                                        660          DC    C','
0000110A  40A689A3 884094F5                         661          DC    C' with m5='
00001113  A7A7                                      662 PRTM5    DC    C'xx'
00001115  4B                                        663          DC    C'.'
                            00000048  00000001      664 PRTLNG   EQU   *-PRTLINE


                                                    666 ***********************************************************************
                                                    667 *        TEST failed : XCHECK
                                                    668 ***********************************************************************
                                                    669 *
                                                    670 *        XCHECK failed message
                                                    671 *
00001116  40404040 4040E385                         672 XCPLINE  DC    C'      Test # '
00001123  A7A7A7                                    673 XCPTNUM  DC    C'xxx'
00001126  40E7C3C8 C5C3D240                         674          DC    c' XCHECK failed for instruction '
00001145  A7A7A7A7 A7A7A7A7                         675 XCPNAME  DC    CL8'xxxxxxxx'
0000114D  40A689A3 884094F4                         676          DC    C' with m4='
00001156  A7A7                                      677 XCPM4    DC    C'xx'
00001158  40A689A3 884094F5                         678          DC    C' with m5='
00001161  A7A7                                      679 XCPM5    DC    C'xx'
00001163  4B                                        680          DC    C'.'
                            0000004E  00000001      681 XCPLNG   EQU   *-XCPLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   683 ***********************************************************************
                                                   684 *        TEST failed : message working storge
                                                   685 ***********************************************************************
00001164  40212020 20202020                        686 EDIT     DC    XL18'402120202020202020202020202020202020'
                                                   687
00001176  7E7E7E6E                                 688          DC    C'===>'
0000117A  40404040 40404040                        689 PRT3     DC    CL18' '
0000118C  4C7E7E7E                                 690          DC    C'<===='
00001190  00000000 00000000                        691 DECNUM   DS    CL16


                                                   693 *
                                                   694 *        Vector instruction results, pollution and input
                                                   695 *
000011A0  00000000 00000000                        696          DS    XL16                                          gap
000011B0  FFFFFFFF FFFFFFFF                        697 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000011C0  12345678 90123456                        698 V1INPUT  DC    XL16'12345678901234567890123456789 01D'   V1 input
000011D0  00000000 00000000                        699          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    701 ************************************************************************
                                                    702 *        E6TEST DSECT
                                                    703 ************************************************************************


                                                    705 E6TEST   DSECT ,
00000000  00000000                                  706 TSUB     DC    A(0)              pointer  to test
00000004  0000                                      707 TNUM     DC    H'00'             Test Number
00000006  00                                        708          DC    X'00'
00000007  40                                        709 XCSKIP   DC    CL1' '            Y = skip cross check
00000008  00                                        710 M4       DC    HL1'00'           m4 used
00000009  00                                        711 M5       DC    HL1'00'           m5 used
0000000A  00                                        712 FLG      DC    X'00'             expected FPC flags
0000000B  00                                        713 VXC      DC    X'00'             VXC expected
0000000C  00000000                                  714 V2ADDR   DC    A(0)              address of v2: 16-byte packed decimal
00000010  40404040 40404040                         715 OPNAME   DC    CL8' '            E6 name
00000018  00000000                                  716 RELEN    DC    A(0)              result length
0000001C  00000000                                  717 READDR   DC    A(0)              expected result address
00000020  00000000 00000000                         718          DS    FD                   gap
00000028  00000000 00000000                         719 V1OUTPUT DS    XL16              V1 Output
00000038  00000000 00000000                         720          DS    FD                   gap
00000040  00000000                                  721 FPC_R    DS    F                 FPC after instruction
00000048  00000000 00000000                         722          DS    FD                   gap
00000050  40404040 40404040                         723 SKIPXC   DC    CL8' '            was cross check skipped?
00000058  00000000 00000000                         724          DS    FD                   gap
00000060  00000000 00000000                         725 XCOUTPUT DS    XL16              Cross check Output
00000070  00000000 00000000                         726          DS    XL16
00000080  00000000 00000000                         727          DS    FD                   gap
00000088  00000000                                  728 FPC_XC1  DS    F                 1st cross check FPC
0000008C  00000000                                  729 FPC_XC2  DS    F                 2nd cross check FPC
00000090  00000000 00000000                         730          DS    FD                   gap
00000098  00000000                                  731 WK1      DS    F                 debug area
0000009C  00000000                                  732 WK2      DS    F
000000A0                                            733          DS    0F
                                                    734 **
                                                    735 *        test routine will be here (from VRR-c macro)


                             00000000  00002D83     737 ZVE6TST  CSECT ,
000011E0                                            738          DS    0F


                                                    740 ************************************************************************
                                                    741 *     Macros to help build test tables
                                                    742 ************************************************************************


                                                    744 *
                                                    745 * macro to generate individual test
                                                    746 *
                                                    747          MACRO
                                                    748          VRR_C &INST,&M4,&M5,&FLAGS,&VXC,&SKIP
                                                    749 .*                             &INST  - VRR-c instruction under test
                                                    750 .*                             &m4    - m4 field
                                                    751 .*                             &m5    - m5 field
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                  .*                                &flags - expected FPC flags (HEX)
                                                  .*                                &VXC   - expected VXC (HEX)
                                                  .*                                &SKIP  - S = skip cross check
                                                           GBLA  &TNUM
                                                  &TNUM    SETA  &TNUM+1

                                                           DS    0FD
                                                           USING *,R5               base for test data and test routine

                                                  T&TNUM   DC    A(X&TNUM)         address of test routine
                                                           DC    H'&TNUM'          test number
                                                           DC    X'00'
                                                           DC    CL1'&SKIP'        Y = skip cross check
                                                           DC    HL1'&M4'          m4
                                                           DC    HL1'&M5'          m5
                                                  FLG&TNUM DC    X'&FLAGS'         expected FPC flags
                                                  VXC&TNUM DC    X'&VXC'           expected VXC
                                                  V2_&TNUM DC    A(RE&TNUM+16)     address of v2: 16-byte packed decimal
                                                           DC    CL8'&INST'        instruction name
                                                           DC    A(16)             result length
                                                           DC    A(RE&TNUM)        address of expected resul
                                                           DS    FD                gap
                                                  V1O&TNUM DS    XL16              V1 output
                                                           DS    FD                   gap
                                                  FPC_R_&TNUM DS F                 FPC after instruction
                                                           DS    FD                   gap
                                                           DC    CL8' '            was cross check skipped?
                                                           DS    FD                   gap
                                                  XCO&TNUM DS    XL16              Cross check Output
                                                           DS    XL16
                                                           DS    FD                   gap
                                                  FPC_XC_&TNUM DS F               1st cross check FPC
                                                           DS    F                2nd cross check FPC
                                                           DS    FD                   gap
                                                           DS    F                 debug area
                                                           DS    F
                                                  .*
                                                  *
                                                  X&TNUM   DS    0F
                                                           LFPC  FPCINIT           initialize FPC
                                                  *         LFPC  =XL4'08000000'         set trap exception

                                                           LGF   R2,V2_&TNUM       get v2
                                                           VLM   V22,V23,0(R2)

                                                           &INST V22,V22,V23,&M4,&M5   test instruction (dest is source)

                                                           STFPC FPC_R_&TNUM       save FPC
                                                           VST   V22,V1O&TNUM      save instruction result

                                                           BR    R11               return

                                                  RE&TNUM  DS    0F                expected 16 byte result
                                                           DROP  R5

                                                           MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   809 *
                                                   810 * macro to generate table of pointers to individual tests
                                                   811 *
                                                   812          MACRO
                                                   813          PTTABLE
                                                   814          GBLA  &TNUM
                                                   815          LCLA  &CUR
                                                   816 &CUR     SETA  1
                                                   817 .*
                                                   818 TTABLE   DS    0F
                                                   819 .LOOP    ANOP
                                                   820 .*
                                                   821          DC    A(T&CUR)          TEST &CUR
                                                   822 .*
                                                   823 &CUR     SETA  &CUR+1
                                                   824          AIF   (&CUR LE &TNUM).LOOP
                                                   825 *
                                                   826          DC    A(0)              END OF TABLE
                                                   827          DC    A(0)
                                                   828 .*
                                                   829          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   831 ************************************************************************
                                                   832 *        E6 VRR-c tests
                                                   833 ************************************************************************
                                                   834         PRINT DATA
                                                   835 *
                                                   836 *        E675  VCRNF   - VECTOR FP CONVERT AND ROUND TO NNP
                                                   837 *
                                                   838 *-----------------------------------------------------------------------
                                                   839 *   VRR-c   instruction, m4, m5, flags, VXC, SKIP
                                                   840 *              NOTE: flags and VXC are HEX values
                                                   841 *   followed by
                                                   842 *              v1 - 16 byte expected result
                                                   843 *              v2 - 16 byte source
                                                   844 *              v3 - 16 byte source
                                                   845 *-----------------------------------------------------------------------
                                                   846 * VCRNF   - VECTOR FP CONVERT AND ROUND TO NNP
                                                   847 *-----------------------------------------------------------------------
                                                   848 * Short Float -> dlfloat  (with cross check dlfloat -> short float)
                                                   849 *
                                                   850 * some of these tests use numbers from PoP SA22-7832-13,
                                                   851 * Figure 9-2. Examples of Floating-Point Numbers ( page 9-6 )
                                                   852 *
                                                   853 * +0     simple instruction test and 'test' test
                                                   854         VRR_C VCRNF,0,2,00,00,N
000011E0                                           855+        DS    0FD
000011E0                       000011E0            856+        USING *,R5              base for test data and test routine
000011E0  00001280                                 857+T1      DC    A(X1)             address of test routine
000011E4  0001                                     858+        DC    H'1'              test number
000011E6  00                                       859+        DC    X'00'
000011E7  D5                                       860+        DC    CL1'N'            Y = skip cross check
000011E8  00                                       861+        DC    HL1'0'            m4
000011E9  02                                       862+        DC    HL1'2'            m5
000011EA  00                                       863+FLG1    DC    X'00'             expected FPC flags
000011EB  00                                       864+VXC1    DC    X'00'             expected VXC
000011EC  000012B4                                 865+V2_1    DC    A(RE1+16)         address of v2: 16-byte packed decimal
000011F0  E5C3D9D5 C6404040                        866+        DC    CL8'VCRNF'        instruction name
000011F8  00000010                                 867+        DC    A(16)             result length
000011FC  000012A4                                 868+        DC    A(RE1)            address of expected resul
00001200  00000000 00000000                        869+        DS    FD                gap
00001208  00000000 00000000                        870+V1O1    DS    XL16              V1 output
00001210  00000000 00000000
00001218  00000000 00000000                        871+        DS    FD                   gap
00001220  00000000                                 872+FPC_R_1 DS    F                 FPC after instruction
00001228  00000000 00000000                        873+        DS    FD                   gap
00001230  40404040 40404040                        874+        DC    CL8' '            was cross check skipped?
00001238  00000000 00000000                        875+        DS    FD                   gap
00001240  00000000 00000000                        876+XCO1    DS    XL16              Cross check Output
00001248  00000000 00000000
00001250  00000000 00000000                        877+        DS    XL16
00001258  00000000 00000000
00001260  00000000 00000000                        878+        DS    FD                   gap
00001268  00000000                                 879+FPC_XC_1 DS   F                1st cross check FPC
0000126C  00000000                                 880+        DS    F                2nd cross check FPC
00001270  00000000 00000000                        881+        DS    FD                   gap
00001278  00000000                                 882+        DS    F                 debug area
0000127C  00000000                                 883+        DS    F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   884+*
00001280                                           885+X1       DS    0F
00001280  B29D 852C                     0000072C   886+         LFPC  FPCINIT           initialize FPC
                                                   887+*         LFPC  =XL4'08000000'          set trap exception
00001284  E320 500C 0014                000011EC   888+         LGF   R2,V2_1           get v2
0000128A  E767 2000 0C36                00000000   889+         VLM   V22,V23,0(R2)
00001290  E666 7002 0E75                           890+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
00001296  B29C 9020                     00001220   891+         STFPC FPC_R_1           save FPC
0000129A  E760 9008 080E                00001208   892+         VST   V22,V1O1          save instruction result
000012A0  07FB                                     893+         BR    R11               return
000012A4                                           894+RE1      DS    0F                expected 16 byte result
000012A4                                           895+         DROP  R5
000012A4  00000000 00000000                        896          DC    XL16'0000000000000000 0000000000000000'
000012AC  00000000 00000000
000012B4  00000000 00000000                        897          DC    XL16'0000000000000000 0000000000000000'
000012BC  00000000 00000000
000012C4  00000000 00000000                        898          DC    XL16'0000000000000000 0000000000000000'
000012CC  00000000 00000000
                                                   899
                                                   900 * +1, -1
                                                   901          VRR_C VCRNF,0,2,00,00,N
000012D8                                           902+         DS    0FD
000012D8                        000012D8           903+         USING *,R5              base for test data and test routine
000012D8  00001378                                 904+T2       DC    A(X2)             address of test routine
000012DC  0002                                     905+         DC    H'2'              test number
000012DE  00                                       906+         DC    X'00'
000012DF  D5                                       907+         DC    CL1'N'            Y = skip cross check
000012E0  00                                       908+         DC    HL1'0'            m4
000012E1  02                                       909+         DC    HL1'2'            m5
000012E2  00                                       910+FLG2     DC    X'00'             expected FPC flags
000012E3  00                                       911+VXC2     DC    X'00'             expected VXC
000012E4  000013AC                                 912+V2_2     DC    A(RE2+16)         address of v2: 16-byte packed decimal
000012E8  E5C3D9D5 C6404040                        913+         DC    CL8'VCRNF'        instruction name
000012F0  00000010                                 914+         DC    A(16)             result length
000012F4  0000139C                                 915+         DC    A(RE2)            address of expected resul
000012F8  00000000 00000000                        916+         DS    FD                gap
00001300  00000000 00000000                        917+V1O2     DS    XL16              V1 output
00001308  00000000 00000000
00001310  00000000 00000000                        918+         DS    FD                   gap
00001318  00000000                                 919+FPC_R_2  DS    F                 FPC after instruction
00001320  00000000 00000000                        920+         DS    FD                   gap
00001328  40404040 40404040                        921+         DC    CL8' '            was cross check skipped?
00001330  00000000 00000000                        922+         DS    FD                   gap
00001338  00000000 00000000                        923+XCO2     DS    XL16              Cross check Output
00001340  00000000 00000000
00001348  00000000 00000000                        924+         DS    XL16
00001350  00000000 00000000
00001358  00000000 00000000                        925+         DS    FD                   gap
00001360  00000000                                 926+FPC_XC_2 DS    F                1st cross check FPC
00001364  00000000                                 927+         DS    F                2nd cross check FPC
00001368  00000000 00000000                        928+         DS    FD                   gap
00001370  00000000                                 929+         DS    F                 debug area
00001374  00000000                                 930+         DS    F
                                                   931+*
00001378                                           932+X2       DS    0F
00001378  B29D 852C                     0000072C   933+         LFPC  FPCINIT           initialize FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  934+*         LFPC  =XL4'08000000'         set trap exception
0000137C  E320 500C 0014                 000012E4  935+         LGF   R2,V2_2            get v2
00001382  E767 2000 0C36                 00000000  936+         VLM   V22,V23,0(R2)
00001388  E666 7002 0E75                           937+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
0000138E  B29C 5040                      00001318  938+         STFPC FPC_R_2            save FPC
00001392  E760 5028 080E                 00001300  939+         VST   V22,V1O2           save instruction result
00001398  07FB                                     940+         BR    R11                return
0000139C                                           941+RE2      DS    0F                 expected 16 byte result
0000139C                                           942+         DROP  R5
0000139C  3E000000 00000000                        943          DC    XL16'3E00000000000000 BE00000000000000'
000013A4  BE000000 00000000
000013AC  3F800000 00000000                        944          DC    XL16'3F80000000000000 0000000000000000'
000013B4  00000000 00000000
000013BC  BF800000 00000000                        945          DC    XL16'BF80000000000000 0000000000000000'
000013C4  00000000 00000000
                                                   946
                                                   947 * +.5, -.5
                                                   948          VRR_C VCRNF,0,2,00,00,N
000013D0                                           949+         DS    0FD
000013D0                         000013D0          950+         USING *,R5               base for test data and test routine
000013D0  00001470                                 951+T3       DC    A(X3)              address of test routine
000013D4  0003                                     952+         DC    H'3'               test number
000013D6  00                                       953+         DC    X'00'
000013D7  D5                                       954+         DC    CL1'N'             Y = skip cross check
000013D8  00                                       955+         DC    HL1'0'             m4
000013D9  02                                       956+         DC    HL1'2'             m5
000013DA  00                                       957+FLG3     DC    X'00'              expected FPC flags
000013DB  00                                       958+VXC3     DC    X'00'              expected VXC
000013DC  000014A4                                 959+V2_3     DC    A(RE3+16)          address of v2: 16-byte packed decimal
000013E0  E5C3D9D5 C6404040                        960+         DC    CL8'VCRNF'         instruction name
000013E8  00000010                                 961+         DC    A(16)              result length
000013EC  00001494                                 962+         DC    A(RE3)             address of expected resul
000013F0  00000000 00000000                        963+         DS    FD                 gap
000013F8  00000000 00000000                        964+V1O3     DS    XL16               V1 output
00001400  00000000 00000000
00001408  00000000 00000000                        965+         DS    FD                    gap
00001410  00000000                                 966+FPC_R_3  DS    F                  FPC after instruction
00001418  00000000 00000000                        967+         DS    FD                    gap
00001420  40404040 40404040                        968+         DC    CL8' '             was cross check skipped?
00001428  00000000 00000000                        969+         DS    FD                    gap
00001430  00000000 00000000                        970+XCO3     DS    XL16               Cross check Output
00001438  00000000 00000000
00001440  00000000 00000000                        971+         DS    XL16
00001448  00000000 00000000
00001450  00000000 00000000                        972+         DS    FD                    gap
00001458  00000000                                 973+FPC_XC_3 DS    F                 1st cross check FPC
0000145C  00000000                                 974+         DS    F                 2nd cross check FPC
00001460  00000000 00000000                        975+         DS    FD                    gap
00001468  00000000                                 976+         DS    F                  debug area
0000146C  00000000                                 977+         DS    F
                                                   978+*
00001470                                           979+X3       DS    0F
00001470  B29D 852C                      0000072C  980+         LFPC  FPCINIT            initialize FPC
                                                   981+*         LFPC  =XL4'08000000'         set trap exception
00001474  E320 500C 0014                 000013DC  982+         LGF   R2,V2_3            get v2
0000147A  E767 2000 0C36                 00000000  983+         VLM   V22,V23,0(R2)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001480  E666 7002 0E75                          984+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
00001486  B29C 5040                     00001410  985+         STFPC FPC_R_3           save FPC
0000148A  E760 5028 080E                000013F8  986+         VST   V22,V1O3          save instruction result
00001490  07FB                                    987+         BR    R11               return
00001494                                          988+RE3      DS    0F                expected 16 byte result
00001494                                          989+         DROP  R5
00001494  3C000000 00000000                       990          DC    XL16'3C00000000000000 BC00000000000000'
0000149C  BC000000 00000000
000014A4  3F000000 00000000                       991          DC    XL16'3F00000000000000 0000000000000000'
000014AC  00000000 00000000
000014B4  BF000000 00000000                       992          DC    XL16'BF00000000000000 0000000000000000'
000014BC  00000000 00000000
                                                  993
                                                  994 * +1/64, -1/64
                                                  995          VRR_C VCRNF,0,2,00,00,N
000014C8                                          996+         DS    0FD
000014C8                        000014C8          997+         USING *,R5              base for test data and test routine
000014C8  00001568                                998+T4       DC    A(X4)             address of test routine
000014CC  0004                                    999+         DC    H'4'              test number
000014CE  00                                     1000+         DC    X'00'
000014CF  D5                                     1001+         DC    CL1'N'            Y = skip cross check
000014D0  00                                     1002+         DC    HL1'0'            m4
000014D1  02                                     1003+         DC    HL1'2'            m5
000014D2  00                                     1004+FLG4     DC    X'00'             expected FPC flags
000014D3  00                                     1005+VXC4     DC    X'00'             expected VXC
000014D4  0000159C                               1006+V2_4     DC    A(RE4+16)         address of v2: 16-byte packed decimal
000014D8  E5C3D9D5 C6404040                      1007+         DC    CL8'VCRNF'        instruction name
000014E0  00000010                               1008+         DC    A(16)             result length
000014E4  0000158C                               1009+         DC    A(RE4)            address of expected resul
000014E8  00000000 00000000                      1010+         DS    FD                gap
000014F0  00000000 00000000                      1011+V1O4     DS    XL16              V1 output
000014F8  00000000 00000000
00001500  00000000 00000000                      1012+         DS    FD                   gap
00001508  00000000                               1013+FPC_R_4  DS    F                 FPC after instruction
00001510  00000000 00000000                      1014+         DS    FD                   gap
00001518  40404040 40404040                      1015+         DC    CL8' '            was cross check skipped?
00001520  00000000 00000000                      1016+         DS    FD                   gap
00001528  00000000 00000000                      1017+XCO4     DS    XL16              Cross check Output
00001530  00000000 00000000
00001538  00000000 00000000                      1018+         DS    XL16
00001540  00000000 00000000
00001548  00000000 00000000                      1019+         DS    FD                   gap
00001550  00000000                               1020+FPC_XC_4 DS    F               1st cross check FPC
00001554  00000000                               1021+         DS    F               2nd cross check FPC
00001558  00000000 00000000                      1022+         DS    FD                   gap
00001560  00000000                               1023+         DS    F                 debug area
00001564  00000000                               1024+         DS    F
                                                 1025+*
00001568                                         1026+X4       DS    0F
00001568  B29D 852C                     0000072C 1027+         LFPC  FPCINIT           initialize FPC
                                                 1028+*         LFPC  =XL4'08000000'          set trap exception
0000156C  E320 500C 0014                000014D4 1029+         LGF   R2,V2_4           get v2
00001572  E767 2000 0C36                00000000 1030+         VLM   V22,V23,0(R2)
00001578  E666 7002 0E75                         1031+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
0000157E  B29C 5040                     00001508 1032+         STFPC FPC_R_4           save FPC
00001582  E760 5028 080E                000014F0 1033+         VST   V22,V1O4          save instruction result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001588  07FB                                     1034+         BR    R11                 return
0000158C                                           1035+RE4      DS    0F                  expected 16 byte result
0000158C                                           1036+         DROP  R5
0000158C  32000000 00000000                        1037          DC    XL16'320000000000000 B200000000000000'
00001594  B2000000 00000000
0000159C  3C800000 00000000                        1038          DC    XL16'3C80000000000000 0000000000000000'
000015A4  00000000 00000000
000015AC  BC800000 00000000                        1039          DC    XL16'BC80000000000000 0000000000000000'
000015B4  00000000 00000000
                                                   1040
                                                   1041 * +0, -0
                                                   1042          VRR_C VCRNF,0,2,00,00,N
000015C0                                           1043+         DS    0FD
000015C0                       000015C0            1044+         USING *,R5                base for test data and test routine
000015C0  00001660                                 1045+T5       DC    A(X5)               address of test routine
000015C4  0005                                     1046+         DC    H'5'                test number
000015C6  00                                       1047+         DC    X'00'
000015C7  D5                                       1048+         DC    CL1'N'              Y = skip cross check
000015C8  00                                       1049+         DC    HL1'0'              m4
000015C9  02                                       1050+         DC    HL1'2'              m5
000015CA  00                                       1051+FLG5     DC    X'00'               expected FPC flags
000015CB  00                                       1052+VXC5     DC    X'00'               expected VXC
000015CC  00001694                                 1053+V2_5     DC    A(RE5+16)           address of v2: 16-byte packed decimal
000015D0  E5C3D9D5 C6404040                        1054+         DC    CL8'VCRNF'          instruction name
000015D8  00000010                                 1055+         DC    A(16)               result length
000015DC  00001684                                 1056+         DC    A(RE5)              address of expected resul
000015E0  00000000 00000000                        1057+         DS    FD                     gap
000015E8  00000000 00000000                        1058+V1O5     DS    XL16                V1 output
000015F0  00000000 00000000
000015F8  00000000 00000000                        1059+         DS    FD                     gap
00001600  00000000                                 1060+FPC_R_5  DS    F                   FPC after instruction
00001608  00000000 00000000                        1061+         DS    FD                     gap
00001610  40404040 40404040                        1062+         DC    CL8' '              was cross check skipped?
00001618  00000000 00000000                        1063+         DS    FD                     gap
00001620  00000000 00000000                        1064+XCO5     DS    XL16                Cross check Output
00001628  00000000 00000000
00001630  00000000 00000000                        1065+         DS    XL16
00001638  00000000 00000000
00001640  00000000 00000000                        1066+         DS    FD                     gap
00001648  00000000                                 1067+FPC_XC_5 DS    F                 1st cross check FPC
0000164C  00000000                                 1068+         DS    F                 2nd cross check FPC
00001650  00000000 00000000                        1069+         DS    FD                     gap
00001658  00000000                                 1070+         DS    F                   debug area
0000165C  00000000                                 1071+         DS    F
                                                   1072+*
00001660                                           1073+X5       DS    0F
00001660  B29D 852C                     0000072C   1074+         LFPC  FPCINIT             initialize FPC
                                                   1075+*         LFPC  =XL4'08000000'          set trap exception
00001664  E320 500C 0014                000015CC   1076+         LGF   R2,V2_5             get v2
0000166A  E767 2000 0C36                00000000   1077+         VLM   V22,V23,0(R2)
00001670  E666 7002 0E75                           1078+         VCRNF V22,V22,V23,0,2         test instruction (dest is source)
00001676  B29C 5040                     00001600   1079+         STFPC FPC_R_5             save FPC
0000167A  E760 5028 080E                000015E8   1080+         VST   V22,V1O5            save instruction result
00001680  07FB                                     1081+         BR    R11                 return
00001684                                           1082+RE5      DS    0F                  expected 16 byte result
00001684                                           1083+         DROP  R5
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001684  00000000 00000000                        1084          DC    XL16'0000000000000000 8000000000000000'
0000168C  80000000 00000000
00001694  00000000 00000000                        1085          DC    XL16'0000000000000000 0000000000000000'
0000169C  00000000 00000000
000016A4  80000000 00000000                        1086          DC    XL16'8000000000000000 0000000000000000'
000016AC  00000000 00000000
                                                   1087
                                                   1088 * +15, -15
                                                   1089          VRR_C VCRNF,0,2,00,00,N
000016B8                                           1090+         DS    0FD
000016B8                       000016B8            1091+         USING *,R5              base for test data and test routine
000016B8  00001758                                 1092+T6       DC    A(X6)             address of test routine
000016BC  0006                                     1093+         DC    H'6'              test number
000016BE  00                                       1094+         DC    X'00'
000016BF  D5                                       1095+         DC    CL1'N'            Y = skip cross check
000016C0  00                                       1096+         DC    HL1'0'            m4
000016C1  02                                       1097+         DC    HL1'2'            m5
000016C2  00                                       1098+FLG6     DC    X'00'             expected FPC flags
000016C3  00                                       1099+VXC6     DC    X'00'             expected VXC
000016C4  0000178C                                 1100+V2_6     DC    A(RE6+16)         address of v2: 16-byte packed decimal
000016C8  E5C3D9D5 C6404040                        1101+         DC    CL8'VCRNF'        instruction name
000016D0  00000010                                 1102+         DC    A(16)             result length
000016D4  0000177C                                 1103+         DC    A(RE6)            address of expected resul
000016D8  00000000 00000000                        1104+         DS    FD                gap
000016E0  00000000 00000000                        1105+V1O6     DS    XL16              V1 output
000016E8  00000000 00000000
000016F0  00000000 00000000                        1106+         DS    FD                   gap
000016F8  00000000                                 1107+FPC_R_6  DS    F                 FPC after instruction
00001700  00000000 00000000                        1108+         DS    FD                   gap
00001708  40404040 40404040                        1109+         DC    CL8' '            was cross check skipped?
00001710  00000000 00000000                        1110+         DS    FD                   gap
00001718  00000000 00000000                        1111+XCO6     DS    XL16              Cross check Output
00001720  00000000 00000000
00001728  00000000 00000000                        1112+         DS    XL16
00001730  00000000 00000000
00001738  00000000 00000000                        1113+         DS    FD                   gap
00001740  00000000                                 1114+FPC_XC_6 DS    F                1st cross check FPC
00001744  00000000                                 1115+         DS    F                2nd cross check FPC
00001748  00000000 00000000                        1116+         DS    FD                   gap
00001750  00000000                                 1117+         DS    F                 debug area
00001754  00000000                                 1118+         DS    F
                                                   1119+*
00001758                                           1120+X6       DS    0F
00001758  B29D 852C                    0000072C    1121+         LFPC  FPCINIT           initialize FPC
                                                   1122+*         LFPC  =XL4'08000000'         set trap exception
0000175C  E320 500C 0014               000016C4    1123+         LGF   R2,V2_6           get v2
00001762  E767 2000 0C36               00000000    1124+         VLM   V22,V23,0(R2)
00001768  E666 7002 0E75                           1125+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
0000176E  B29C 5040                    000016F8    1126+         STFPC FPC_R_6           save FPC
00001772  E760 5028 080E               000016E0    1127+         VST   V22,V1O6          save instruction result
00001778  07FB                                     1128+         BR    R11               return
0000177C                                           1129+RE6      DS    0F                expected 16 byte result
0000177C                                           1130+         DROP  R5
0000177C  45C00000 00000000                        1131          DC    XL16'45C0000000000000 C5C0000000000000'
00001784  C5C00000 00000000
0000178C  41700000 00000000                        1132          DC    XL16'4170000000000000 0000000000000000'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001794  00000000 00000000
0000179C  C1700000 00000000                         1133          DC    XL16'C170000000000000 0000000000000000'
000017A4  00000000 00000000
                                                    1134
                                                    1135 * +20/7, - 20/7
                                                    1136          VRR_C VCRNF,0,2,00,00,S                 skip xc: lost digits
000017B0                                            1137+         DS    0FD
000017B0                       000017B0             1138+         USING *,R5              base for test data and test routine
000017B0  00001850                                  1139+T7       DC    A(X7)             address of test routine
000017B4  0007                                      1140+         DC    H'7'              test number
000017B6  00                                        1141+         DC    X'00'
000017B7  E2                                        1142+         DC    CL1'S'            Y = skip cross check
000017B8  00                                        1143+         DC    HL1'0'            m4
000017B9  02                                        1144+         DC    HL1'2'            m5
000017BA  00                                        1145+FLG7     DC    X'00'             expected FPC flags
000017BB  00                                        1146+VXC7     DC    X'00'             expected VXC
000017BC  00001884                                  1147+V2_7     DC    A(RE7+16)         address of v2: 16-byte packed decimal
000017C0  E5C3D9D5 C6404040                         1148+         DC    CL8'VCRNF'        instruction name
000017C8  00000010                                  1149+         DC    A(16)             result length
000017CC  00001874                                  1150+         DC    A(RE7)            address of expected resul
000017D0  00000000 00000000                         1151+         DS    FD                gap
000017D8  00000000 00000000                         1152+V1O7     DS    XL16              V1 output
000017E0  00000000 00000000
000017E8  00000000 00000000                         1153+         DS    FD                   gap
000017F0  00000000                                  1154+FPC_R_7  DS    F                 FPC after instruction
000017F8  00000000 00000000                         1155+         DS    FD                   gap
00001800  40404040 40404040                         1156+         DC    CL8' '            was cross check skipped?
00001808  00000000 00000000                         1157+         DS    FD                   gap
00001810  00000000 00000000                         1158+XCO7     DS    XL16              Cross check Output
00001818  00000000 00000000
00001820  00000000 00000000                         1159+         DS    XL16
00001828  00000000 00000000
00001830  00000000 00000000                         1160+         DS    FD                   gap
00001838  00000000                                  1161+FPC_XC_7 DS    F                1st cross check FPC
0000183C  00000000                                  1162+         DS    F                2nd cross check FPC
00001840  00000000 00000000                         1163+         DS    FD                   gap
00001848  00000000                                  1164+         DS    F                 debug area
0000184C  00000000                                  1165+         DS    F
                                                    1166+*
00001850                                            1167+X7       DS    0F
00001850  B29D 852C                     0000072C    1168+         LFPC  FPCINIT           initialize FPC
                                                    1169+*         LFPC  =XL4'08000000'         set trap exception
00001854  E320 500C 0014                000017BC    1170+         LGF   R2,V2_7           get v2
0000185A  E767 2000 0C36                00000000    1171+         VLM   V22,V23,0(R2)
00001860  E666 7002 0E75                            1172+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
00001866  B29C 5040                     000017F0    1173+         STFPC FPC_R_7           save FPC
0000186A  E760 5028 080E                000017D8    1174+         VST   V22,V1O7          save instruction result
00001870  07FB                                      1175+         BR    R11               return
00001874                                            1176+RE7      DS    0F                expected 16 byte result
00001874                                            1177+         DROP  R5
00001874  40DB0000 00000000                         1178          DC    XL16'40DB000000000000 C0DB000000000000'
0000187C  C0DB0000 00000000
00001884  4036DB6E 00000000                         1179          DC    XL16'4036DB6E00000000 0000000000000000'
0000188C  00000000 00000000
00001894  C036DB6E 00000000                         1180          DC    XL16'C036DB6E00000000 0000000000000000'
0000189C  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   1181
                                                   1182 * +2^(-126), -2^(-126)
                                                   1183          VRR_C VCRNF,0,2,10,44,S                skip xc: underflow
000018A8                                           1184+         DS    0FD
000018A8                       000018A8            1185+         USING *,R5              base for test data and test routine
000018A8  00001948                                 1186+T8       DC    A(X8)             address of test routine
000018AC  0008                                     1187+         DC    H'8'              test number
000018AE  00                                       1188+         DC    X'00'
000018AF  E2                                       1189+         DC    CL1'S'            Y = skip cross check
000018B0  00                                       1190+         DC    HL1'0'            m4
000018B1  02                                       1191+         DC    HL1'2'            m5
000018B2  10                                       1192+FLG8     DC    X'10'             expected FPC flags
000018B3  44                                       1193+VXC8     DC    X'44'             expected VXC
000018B4  0000197C                                 1194+V2_8     DC    A(RE8+16)         address of v2: 16-byte packed decimal
000018B8  E5C3D9D5 C6404040                        1195+         DC    CL8'VCRNF'        instruction name
000018C0  00000010                                 1196+         DC    A(16)             result length
000018C4  0000196C                                 1197+         DC    A(RE8)            address of expected resul
000018C8  00000000 00000000                        1198+         DS    FD                gap
000018D0  00000000 00000000                        1199+V1O8     DS    XL16              V1 output
000018D8  00000000 00000000
000018E0  00000000 00000000                        1200+         DS    FD                   gap
000018E8  00000000                                 1201+FPC_R_8  DS    F                 FPC after instruction
000018F0  00000000 00000000                        1202+         DS    FD                   gap
000018F8  40404040 40404040                        1203+         DC    CL8' '            was cross check skipped?
00001900  00000000 00000000                        1204+         DS    FD                   gap
00001908  00000000 00000000                        1205+XCO8     DS    XL16              Cross check Output
00001910  00000000 00000000
00001918  00000000 00000000                        1206+         DS    XL16
00001920  00000000 00000000
00001928  00000000 00000000                        1207+         DS    FD                   gap
00001930  00000000                                 1208+FPC_XC_8 DS    F                1st cross check FPC
00001934  00000000                                 1209+         DS    F                2nd cross check FPC
00001938  00000000 00000000                        1210+         DS    FD                   gap
00001940  00000000                                 1211+         DS    F                 debug area
00001944  00000000                                 1212+         DS    F
                                                   1213+*
00001948                                           1214+X8       DS    0F
00001948  B29D 852C                    0000072C    1215+         LFPC  FPCINIT           initialize FPC
                                                   1216+*         LFPC  =XL4'08000000'          set trap exception
0000194C  E320 500C 0014               000018B4    1217+         LGF   R2,V2_8           get v2
00001952  E767 2000 0C36               00000000    1218+         VLM   V22,V23,0(R2)
00001958  E666 7002 0E75                           1219+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
0000195E  B29C 5040                    000018E8    1220+         STFPC FPC_R_8           save FPC
00001962  E760 5028 080E               000018D0    1221+         VST   V22,V1O8          save instruction result
00001968  07FB                                     1222+         BR    R11               return
0000196C                                           1223+RE8      DS    0F                expected 16 byte result
0000196C                                           1224+         DROP  R5
0000196C  00000000 00000000                        1225          DC    XL16'0000000000000000 8000000000000000'
00001974  80000000 00000000
0000197C  00800000 00000000                        1226          DC    XL16'0080000000000000 0000000000000000'
00001984  00000000 00000000
0000198C  80800000 00000000                        1227          DC    XL16'8080000000000000 0000000000000000'
00001994  00000000 00000000
                                                   1228
                                                   1229 * +2^(-149), -2^(-149) - subnormal
                                                   1230          VRR_C VCRNF,0,2,10,44,S                skip xc: underflow
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000019A0                                           1231+         DS    0FD
000019A0                     000019A0              1232+         USING *,R5              base for test data and test routine
000019A0  00001A40                                 1233+T9       DC    A(X9)             address of test routine
000019A4  0009                                     1234+         DC    H'9'              test number
000019A6  00                                       1235+         DC    X'00'
000019A7  E2                                       1236+         DC    CL1'S'            Y = skip cross check
000019A8  00                                       1237+         DC    HL1'0'            m4
000019A9  02                                       1238+         DC    HL1'2'            m5
000019AA  10                                       1239+FLG9     DC    X'10'             expected FPC flags
000019AB  44                                       1240+VXC9     DC    X'44'             expected VXC
000019AC  00001A74                                 1241+V2_9     DC    A(RE9+16)         address of v2: 16-byte packed decimal
000019B0  E5C3D9D5 C6404040                        1242+         DC    CL8'VCRNF'        instruction name
000019B8  00000010                                 1243+         DC    A(16)             result length
000019BC  00001A64                                 1244+         DC    A(RE9)            address of expected resul
000019C0  00000000 00000000                        1245+         DS    FD                gap
000019C8  00000000 00000000                        1246+V1O9     DS    XL16              V1 output
000019D0  00000000 00000000
000019D8  00000000 00000000                        1247+         DS    FD                   gap
000019E0  00000000                                 1248+FPC_R_9  DS    F                 FPC after instruction
000019E8  00000000 00000000                        1249+         DS    FD                   gap
000019F0  40404040 40404040                        1250+         DC    CL8' '            was cross check skipped?
000019F8  00000000 00000000                        1251+         DS    FD                   gap
00001A00  00000000 00000000                        1252+XCO9     DS    XL16              Cross check Output
00001A08  00000000 00000000
00001A10  00000000 00000000                        1253+         DS    XL16
00001A18  00000000 00000000
00001A20  00000000 00000000                        1254+         DS    FD                   gap
00001A28  00000000                                 1255+FPC_XC_9 DS    F                1st cross check FPC
00001A2C  00000000                                 1256+         DS    F                2nd cross check FPC
00001A30  00000000 00000000                        1257+         DS    FD                   gap
00001A38  00000000                                 1258+         DS    F                 debug area
00001A3C  00000000                                 1259+         DS    F
                                                   1260+*
00001A40                                           1261+X9       DS    0F
00001A40  B29D 852C                     0000072C   1262+         LFPC  FPCINIT           initialize FPC
                                                   1263+*         LFPC  =XL4'08000000'         set trap exception
00001A44  E320 500C 0014                000019AC   1264+         LGF   R2,V2_9           get v2
00001A4A  E767 2000 0C36                00000000   1265+         VLM   V22,V23,0(R2)
00001A50  E666 7002 0E75                           1266+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
00001A56  B29C 5040                     000019E0   1267+         STFPC FPC_R_9           save FPC
00001A5A  E760 5028 080E                000019C8   1268+         VST   V22,V1O9          save instruction result
00001A60  07FB                                     1269+         BR    R11               return
00001A64                                           1270+RE9      DS    0F                expected 16 byte result
00001A64                                           1271+         DROP  R5
00001A64  00000000 00000000                        1272          DC    XL16'0000000000000000 8000000000000000'
00001A6C  80000000 00000000
00001A74  00000001 00000000                        1273          DC    XL16'0000000100000000 0000000000000000'
00001A7C  00000000 00000000
00001A84  80800001 00000000                        1274          DC    XL16'8080000100000000 0000000000000000'
00001A8C  00000000 00000000
                                                   1275
                                                   1276 * +2^(128) * (1 - 2^(-24)) , - +2^(128) * (1 - 2^(-24))
                                                   1277          VRR_C VCRNF,0,2,20,43,S                 skip xc: overflow
00001A98                                           1278+         DS    0FD
00001A98                     00001A98              1279+         USING *,R5              base for test data and test routine
00001A98  00001B38                                 1280+T10      DC    A(X10)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001A9C  000A                                     1281+         DC    H'10'              test number
00001A9E  00                                       1282+         DC    X'00'
00001A9F  E2                                       1283+         DC    CL1'S'             Y = skip cross check
00001AA0  00                                       1284+         DC    HL1'0'             m4
00001AA1  02                                       1285+         DC    HL1'2'             m5
00001AA2  20                                       1286+FLG10    DC    X'20'              expected FPC flags
00001AA3  43                                       1287+VXC10    DC    X'43'              expected VXC
00001AA4  00001B6C                                 1288+V2_10    DC    A(RE10+16)         address of v2: 16-byte packed decimal
00001AA8  E5C3D9D5 C6404040                        1289+         DC    CL8'VCRNF'         instruction name
00001AB0  00000010                                 1290+         DC    A(16)              result length
00001AB4  00001B5C                                 1291+         DC    A(RE10)            address of expected resul
00001AB8  00000000 00000000                        1292+         DS    FD                 gap
00001AC0  00000000 00000000                        1293+V1O10    DS    XL16               V1 output
00001AC8  00000000 00000000
00001AD0  00000000 00000000                        1294+         DS    FD                    gap
00001AD8  00000000                                 1295+FPC_R_10 DS    F                  FPC after instruction
00001AE0  00000000 00000000                        1296+         DS    FD                    gap
00001AE8  40404040 40404040                        1297+         DC    CL8' '             was cross check skipped?
00001AF0  00000000 00000000                        1298+         DS    FD                    gap
00001AF8  00000000 00000000                        1299+XCO10    DS    XL16               Cross check Output
00001B00  00000000 00000000
00001B08  00000000 00000000                        1300+         DS    XL16
00001B10  00000000 00000000
00001B18  00000000 00000000                        1301+         DS    FD                    gap
00001B20  00000000                                 1302+FPC_XC_10 DS   F                 1st cross check FPC
00001B24  00000000                                 1303+         DS    F                 2nd cross check FPC
00001B28  00000000 00000000                        1304+         DS    FD                    gap
00001B30  00000000                                 1305+         DS    F                  debug area
00001B34  00000000                                 1306+         DS    F
                                                   1307+*
00001B38                                           1308+X10      DS    0F
00001B38  B29D 852C                     0000072C   1309+         LFPC  FPCINITI           initialize FPC
                                                   1310+*         LFPC  =XL4'08000000'          set trap exception
00001B3C  E320 500C 0014                00001AA4   1311+         LGF   R2,V2_10           get v2
00001B42  E767 2000 0C36                00000000   1312+         VLM   V22,V23,0(R2)
00001B48  E666 7002 0E75                           1313+         VCRNF V22,V22,V23,0,2        test instruction (dest is source)
00001B4E  B29C 5040                     00001AD8   1314+         STFPC FPC_R_10           save FPC
00001B52  E760 5028 080E                00001AC0   1315+         VST   V22,V1O10          save instruction result
00001B58  07FB                                     1316+         BR    R11                return
00001B5C                                           1317+RE10     DS    0F                 expected 16 byte result
00001B5C                                           1318+         DROP  R5
00001B5C  7FFE0000 00000000                        1319          DC    XL16'7FFE000000000000 FFFE000000000000'
00001B64  FFFE0000 00000000
00001B6C  7F7FFFFF 00000000                        1320          DC    XL16'7F7FFFFF00000000 0000000000000000'
00001B74  00000000 00000000
00001B7C  FF7FFFFF 00000000                        1321          DC    XL16'FF7FFFFF00000000 0000000000000000'
00001B84  00000000 00000000
                                                   1322
                                                   1323 * NAN, -NAN
                                                   1324          VRR_C VCRNF,0,2,80,41,S                 skip xc: invalid on XC
00001B90                                           1325+         DS    0FD
00001B90                        00001B90           1326+         USING *,R5               base for test data and test routine
00001B90  00001C30                                 1327+T11      DC    A(X11)             address of test routine
00001B94  000B                                     1328+         DC    H'11'              test number
00001B96  00                                       1329+         DC    X'00'
00001B97  E2                                       1330+         DC    CL1'S'             Y = skip cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001B98  00                                       1331+         DC    HL1'0'            m4
00001B99  02                                       1332+         DC    HL1'2'            m5
00001B9A  80                                       1333+FLG11    DC    X'80'             expected FPC flags
00001B9B  41                                       1334+VXC11    DC    X'41'             expected VXC
00001B9C  00001C64                                 1335+V2_11    DC    A(RE11+16)        address of v2: 16-byte packed decimal
00001BA0  E5C3D9D5 C6404040                        1336+         DC    CL8'VCRNF'        instruction name
00001BA8  00000010                                 1337+         DC    A(16)             result length
00001BAC  00001C54                                 1338+         DC    A(RE11)           address of expected resul
00001BB0  00000000 00000000                        1339+         DS    FD                gap
00001BB8  00000000 00000000                        1340+V1O11    DS    XL16              V1 output
00001BC0  00000000 00000000
00001BC8  00000000 00000000                        1341+         DS    FD                   gap
00001BD0  00000000                                 1342+FPC_R_11 DS    F                 FPC after instruction
00001BD8  00000000 00000000                        1343+         DS    FD                   gap
00001BE0  40404040 40404040                        1344+         DC    CL8' '            was cross check skipped?
00001BE8  00000000 00000000                        1345+         DS    FD                   gap
00001BF0  00000000 00000000                        1346+XCO11    DS    XL16              Cross check Output
00001BF8  00000000 00000000
00001C00  00000000 00000000                        1347+         DS    XL16
00001C08  00000000 00000000
00001C10  00000000 00000000                        1348+         DS    FD                   gap
00001C18  00000000                                 1349+FPC_XC_11 DS   F                1st cross check FPC
00001C1C  00000000                                 1350+         DS    F                2nd cross check FPC
00001C20  00000000 00000000                        1351+         DS    FD                   gap
00001C28  00000000                                 1352+         DS    F                 debug area
00001C2C  00000000                                 1353+         DS    F
                                                   1354+*
00001C30                                           1355+X11      DS    0F
00001C30  B29D 852C                     0000072C   1356+         LFPC  FPCINIT           initialize FPC
                                                   1357+*         LFPC  =XL4'08000000'          set trap exception
00001C34  E320 500C 0014                00001B9C   1358+         LGF   R2,V2_11          get v2
00001C3A  E767 2000 0C36                00000000   1359+         VLM   V22,V23,0(R2)
00001C40  E666 7002 0E75                           1360+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
00001C46  B29C 5040                     00001BD0   1361+         STFPC FPC_R_11          save FPC
00001C4A  E760 5028 080E                00001BB8   1362+         VST   V22,V1O11         save instruction result
00001C50  07FB                                     1363+         BR    R11               return
00001C54                                           1364+RE11     DS    0F                expected 16 byte result
00001C54                                           1365+         DROP  R5
00001C54  7FFF0000 00000000                        1366          DC    XL16'7FFF000000000000 FFFF000000000000'
00001C5C  FFFF0000 00000000
00001C64  7FC00000 00000000                        1367          DC    XL16'7FC0000000000000 0000000000000000'
00001C6C  00000000 00000000
00001C74  FFC00000 00000000                        1368          DC    XL16'FFC0000000000000 0000000000000000'
00001C7C  00000000 00000000
                                                   1369
                                                   1370 * bad m4 - inexact
                                                   1371          VRR_C VCRNF,2,2,08,05,S                 skip xc: inexact
00001C88                                           1372+         DS    0FD
00001C88                        00001C88           1373+         USING *,R5              base for test data and test routine
00001C88  00001D28                                 1374+T12      DC    A(X12)            address of test routine
00001C8C  000C                                     1375+         DC    H'12'             test number
00001C8E  00                                       1376+         DC    X'00'
00001C8F  E2                                       1377+         DC    CL1'S'            Y = skip cross check
00001C90  02                                       1378+         DC    HL1'2'            m4
00001C91  02                                       1379+         DC    HL1'2'            m5
00001C92  08                                       1380+FLG12    DC    X'08'             expected FPC flags
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001C93  05                                       1381+VXC12    DC    X'05'              expected VXC
00001C94  00001D5C                                 1382+V2_12    DC    A(RE12+16)         address of v2: 16-byte packed decimal
00001C98  E5C3D9D5 C6404040                        1383+         DC    CL8'VCRNF'         instruction name
00001CA0  00000010                                 1384+         DC    A(16)              result length
00001CA4  00001D4C                                 1385+         DC    A(RE12)            address of expected resul
00001CA8  00000000 00000000                        1386+         DS    FD                 gap
00001CB0  00000000 00000000                        1387+V1O12    DS    XL16               V1 output
00001CB8  00000000 00000000
00001CC0  00000000 00000000                        1388+         DS    FD                    gap
00001CC8  00000000                                 1389+FPC_R_12 DS    F                  FPC after instruction
00001CD0  00000000 00000000                        1390+         DS    FD                    gap
00001CD8  40404040 40404040                        1391+         DC    CL8' '             was cross check skipped?
00001CE0  00000000 00000000                        1392+         DS    FD                    gap
00001CE8  00000000 00000000                        1393+XCO12    DS    XL16               Cross check Output
00001CF0  00000000 00000000
00001CF8  00000000 00000000                        1394+         DS    XL16
00001D00  00000000 00000000
00001D08  00000000 00000000                        1395+         DS    FD                    gap
00001D10  00000000                                 1396+FPC_XC_12 DS   F                 1st cross check FPC
00001D14  00000000                                 1397+         DS    F                 2nd cross check FPC
00001D18  00000000 00000000                        1398+         DS    FD                    gap
00001D20  00000000                                 1399+         DS    F                  debug area
00001D24  00000000                                 1400+         DS    F
                                                   1401+*
00001D28                                           1402+X12      DS    0F
00001D28  B29D 852C                      0000072C  1403+         LFPC  FPCINIT            initialize FPC
                                                   1404+*         LFPC  =XL4'08000000'          set trap exception
00001D2C  E320 500C 0014                 00001C94  1405+         LGF   R2,V2_12           get v2
00001D32  E767 2000 0C36                 00000000  1406+         VLM   V22,V23,0(R2)
00001D38  E666 7002 2E75                           1407+         VCRNF V22,V22,V23,2,2        test instruction (dest is source)
00001D3E  B29C 5040                      00001CC8  1408+         STFPC FPC_R_12           save FPC
00001D42  E760 5028 080E                 00001CB0  1409+         VST   V22,V1O12          save instruction result
00001D48  07FB                                     1410+         BR    R11                return
00001D4C                                           1411+RE12     DS    0F                 expected 16 byte result
00001D4C                                           1412+         DROP  R5
00001D4C  00000000 00000000                        1413          DC    XL16'0000000000000000 0000000000000000'
00001D54  00000000 00000000
00001D5C  7FC00000 00000000                        1414          DC    XL16'7FC0000000000000 0000000000000000'
00001D64  00000000 00000000
00001D6C  FFC00000 00000000                        1415          DC    XL16'FFC0000000000000 0000000000000000'
00001D74  00000000 00000000
                                                   1416
                                                   1417 * bad m5 - inexact
                                                   1418          VRR_C VCRNF,0,3,08,05,S                 skip xc: inexact
00001D80                                           1419+         DS    0FD
00001D80                         00001D80          1420+         USING *,R5               base for test data and test routine
00001D80  00001E20                                 1421+T13      DC    A(X13)             address of test routine
00001D84  000D                                     1422+         DC    H'13'              test number
00001D86  00                                       1423+         DC    X'00'
00001D87  E2                                       1424+         DC    CL1'S'             Y = skip cross check
00001D88  00                                       1425+         DC    HL1'0'             m4
00001D89  03                                       1426+         DC    HL1'3'             m5
00001D8A  08                                       1427+FLG13    DC    X'08'              expected FPC flags
00001D8B  05                                       1428+VXC13    DC    X'05'              expected VXC
00001D8C  00001E54                                 1429+V2_13    DC    A(RE13+16)         address of v2: 16-byte packed decimal
00001D90  E5C3D9D5 C6404040                        1430+         DC    CL8'VCRNF'         instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001D98  00000010                                 1431+         DC    A(16)              result length
00001D9C  00001E44                                 1432+         DC    A(RE13)            address of expected resul
00001DA0  00000000 00000000                        1433+         DS    FD                 gap
00001DA8  00000000 00000000                        1434+V1O13    DS    XL16               V1 output
00001DB0  00000000 00000000
00001DB8  00000000 00000000                        1435+         DS    FD                    gap
00001DC0  00000000                                 1436+FPC_R_13 DS    F                  FPC after instruction
00001DC8  00000000 00000000                        1437+         DS    FD                    gap
00001DD0  40404040 40404040                        1438+         DC    CL8' '             was cross check skipped?
00001DD8  00000000 00000000                        1439+         DS    FD                    gap
00001DE0  00000000 00000000                        1440+XCO13    DS    XL16               Cross check Output
00001DE8  00000000 00000000
00001DF0  00000000 00000000                        1441+         DS    XL16
00001DF8  00000000 00000000
00001E00  00000000 00000000                        1442+         DS    FD                    gap
00001E08  00000000                                 1443+FPC_XC_13 DS   F                 1st cross check FPC
00001E0C  00000000                                 1444+         DS    F                 2nd cross check FPC
00001E10  00000000 00000000                        1445+         DS    FD                    gap
00001E18  00000000                                 1446+         DS    F                  debug area
00001E1C  00000000                                 1447+         DS    F
                                                   1448+*
00001E20                                           1449+X13      DS    0F
00001E20  B29D 852C                     0000072C   1450+         LFPC  FPCINIT            initialize FPC
                                                   1451+*         LFPC  =XL4'08000000'          set trap exception
00001E24  E320 500C 0014                00001D8C   1452+         LGF   R2,V2_13           get v2
00001E2A  E767 2000 0C36                00000000   1453+         VLM   V22,V23,0(R2)
00001E30  E666 7003 0E75                           1454+         VCRNF V22,V22,V23,0,3       test instruction (dest is source)
00001E36  B29C 5040                     00001DC0   1455+         STFPC FPC_R_13           save FPC
00001E3A  E760 5028 080E                00001DA8   1456+         VST   V22,V1O13          save instruction result
00001E40  07FB                                     1457+         BR    R11                return
00001E44                                           1458+RE13     DS    0F                 expected 16 byte result
00001E44                                           1459+         DROP  R5
00001E44  00000000 00000000                        1460          DC    XL16'0000000000000000 0000000000000000'
00001E4C  00000000 00000000
00001E54  7FC00000 00000000                        1461          DC    XL16'7FC0000000000000 0000000000000000'
00001E5C  00000000 00000000
00001E64  FFC00000 00000000                        1462          DC    XL16'FFC0000000000000 0000000000000000'
00001E6C  00000000 00000000
                                                   1463
                                                   1464 * Additional tests
                                                   1465 *-----------------------------------------------------------------------
                                                   1466 * +99.1, -99.1
                                                   1467          VRR_C VCRNF,0,2,00,00,S                 skip xc: lost digits
00001E78                                           1468+         DS    0FD
00001E78                        00001E78           1469+         USING *,R5               base for test data and test routine
00001E78  00001F18                                 1470+T14      DC    A(X14)             address of test routine
00001E7C  000E                                     1471+         DC    H'14'              test number
00001E7E  00                                       1472+         DC    X'00'
00001E7F  E2                                       1473+         DC    CL1'S'             Y = skip cross check
00001E80  00                                       1474+         DC    HL1'0'             m4
00001E81  02                                       1475+         DC    HL1'2'             m5
00001E82  00                                       1476+FLG14    DC    X'00'              expected FPC flags
00001E83  00                                       1477+VXC14    DC    X'00'              expected VXC
00001E84  00001F4C                                 1478+V2_14    DC    A(RE14+16)         address of v2: 16-byte packed decimal
00001E88  E5C3D9D5 C6404040                        1479+         DC    CL8'VCRNF'         instruction name
00001E90  00000010                                 1480+         DC    A(16)              result length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001E94  00001F3C                                 1481+         DC    A(RE14)           address of expected resul
00001E98  00000000 00000000                        1482+         DS    FD                gap
00001EA0  00000000 00000000                        1483+V1O14    DS    XL16              V1 output
00001EA8  00000000 00000000
00001EB0  00000000 00000000                        1484+         DS    FD                   gap
00001EB8  00000000                                 1485+FPC_R_14 DS    F                 FPC after instruction
00001EC0  00000000 00000000                        1486+         DS    FD                   gap
00001EC8  40404040 40404040                        1487+         DC    CL8' '            was cross check skipped?
00001ED0  00000000 00000000                        1488+         DS    FD                   gap
00001ED8  00000000 00000000                        1489+XCO14    DS    XL16              Cross check Output
00001EE0  00000000 00000000
00001EE8  00000000 00000000                        1490+         DS    XL16
00001EF0  00000000 00000000
00001EF8  00000000 00000000                        1491+         DS    FD                   gap
00001F00  00000000                                 1492+FPC_XC_14 DS   F                1st cross check FPC
00001F04  00000000                                 1493+         DS    F                2nd cross check FPC
00001F08  00000000 00000000                        1494+         DS    FD                   gap
00001F10  00000000                                 1495+         DS    F                 debug area
00001F14  00000000                                 1496+         DS    F
                                                   1497+*
00001F18                                           1498+X14      DS    0F
00001F18  B29D 852C                     0000072C   1499+         LFPC  FPCINIT           initialize FPC
                                                   1500+*         LFPC  =XL4'08000000'         set trap exception
00001F1C  E320 500C 0014                00001E84   1501+         LGF   R2,V2_14          get v2
00001F22  E767 2000 0C36                00000000   1502+         VLM   V22,V23,0(R2)
00001F28  E666 7002 0E75                           1503+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
00001F2E  B29C 5040                     00001EB8   1504+         STFPC FPC_R_14          save FPC
00001F32  E760 5028 080E                00001EA0   1505+         VST   V22,V1O14         save instruction result
00001F38  07FB                                     1506+         BR    R11               return
00001F3C                                           1507+RE14     DS    0F                expected 16 byte result
00001F3C                                           1508+         DROP  R5
00001F3C  4B190000 00000000                        1509          DC    XL16'4B19000000000000 CB19000000000000'
00001F44  CB190000 00000000
00001F4C  42C63333 00000000                        1510          DC    XL16'42C6333300000000 0000000000000000'
00001F54  00000000 00000000
00001F5C  C2C63333 00000000                        1511          DC    XL16'C2C6333300000000 0000000000000000'
00001F64  00000000 00000000
                                                   1512
                                                   1513 * +100.9, -100.9
                                                   1514          VRR_C VCRNF,0,2,00,00,S                skip xc: lost digits
00001F70                                           1515+         DS    0FD
00001F70                        00001F70           1516+         USING *,R5              base for test data and test routine
00001F70  00002010                                 1517+T15      DC    A(X15)            address of test routine
00001F74  000F                                     1518+         DC    H'15'             test number
00001F76  00                                       1519+         DC    X'00'
00001F77  E2                                       1520+         DC    CL1'S'            Y = skip cross check
00001F78  00                                       1521+         DC    HL1'0'            m4
00001F79  02                                       1522+         DC    HL1'2'            m5
00001F7A  00                                       1523+FLG15    DC    X'00'             expected FPC flags
00001F7B  00                                       1524+VXC15    DC    X'00'             expected VXC
00001F7C  00002044                                 1525+V2_15    DC    A(RE15+16)        address of v2: 16-byte packed decimal
00001F80  E5C3D9D5 C6404040                        1526+         DC    CL8'VCRNF'        instruction name
00001F88  00000010                                 1527+         DC    A(16)             result length
00001F8C  00002034                                 1528+         DC    A(RE15)           address of expected resul
00001F90  00000000 00000000                        1529+         DS    FD                gap
00001F98  00000000 00000000                        1530+V1O15    DS    XL16              V1 output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001FA0  00000000 00000000
00001FA8  00000000 00000000                        1531+          DS    FD                    gap
00001FB0  00000000                                 1532+FPC_R_15 DS    F                  FPC after instruction
00001FB8  00000000 00000000                        1533+          DS    FD                    gap
00001FC0  40404040 40404040                        1534+          DC    CL8' '             was cross check skipped?
00001FC8  00000000 00000000                        1535+          DS    FD                    gap
00001FD0  00000000 00000000                        1536+XCO15     DS    XL16               Cross check Output
00001FD8  00000000 00000000
00001FE0  00000000 00000000                        1537+          DS    XL16
00001FE8  00000000 00000000
00001FF0  00000000 00000000                        1538+          DS    FD                    gap
00001FF8  00000000                                 1539+FPC_XC_15 DS   F                 1st cross check FPC
00001FFC  00000000                                 1540+          DS    F                 2nd cross check FPC
00002000  00000000 00000000                        1541+          DS    FD                    gap
00002008  00000000                                 1542+          DS    F                  debug area
0000200C  00000000                                 1543+          DS    F
                                                   1544+*
00002010                                           1545+X15       DS    0F
00002010  B29D 852C                     0000072C   1546+          LFPC  FPCINIT            initialize FPC
                                                   1547+*          LFPC  =XL4'08000000'          set trap exception
00002014  E320 500C 0014                00001F7C   1548+          LGF   R2,V2_15           get v2
0000201A  E767 2000 0C36                00000000   1549+          VLM   V22,V23,0(R2)
00002020  E666 7002 0E75                           1550+          VCRNF V22,V22,V23,0,2        test instruction (dest is source)
00002026  B29C 5040                     00001FB0   1551+          STFPC FPC_R_15           save FPC
0000202A  E760 5028 080E                00001F98   1552+          VST   V22,V1O15          save instruction result
00002030  07FB                                     1553+          BR    R11                return
00002034                                           1554+RE15      DS    0F                 expected 16 byte result
00002034                                           1555+          DROP  R5
00002034  4B270000 00000000                        1556           DC    XL16'4B27000000000000 CB27000000000000'
0000203C  CB270000 00000000
00002044  42C9CCCD 00000000                        1557           DC    XL16'42C9CCCD00000000 0000000000000000'
0000204C  00000000 00000000
00002054  C2C9CCCD 00000000                        1558           DC    XL16'C2C9CCCD00000000 0000000000000000'
0000205C  00000000 00000000
                                                   1559
                                                   1560 * +527.7895, -527.7895
                                                   1561           VRR_C VCRNF,0,2,00,00,S                skip xc: lost digits
00002068                                           1562+          DS    0FD
00002068                        00002068           1563+          USING *,R5               base for test data and test routine
00002068  00002108                                 1564+T16       DC    A(X16)             address of test routine
0000206C  0010                                     1565+          DC    H'16'              test number
0000206E  00                                       1566+          DC    X'00'
0000206F  E2                                       1567+          DC    CL1'S'             Y = skip cross check
00002070  00                                       1568+          DC    HL1'0'             m4
00002071  02                                       1569+          DC    HL1'2'             m5
00002072  00                                       1570+FLG16     DC    X'00'              expected FPC flags
00002073  00                                       1571+VXC16     DC    X'00'              expected VXC
00002074  0000213C                                 1572+V2_16     DC    A(RE16+16)         address of v2: 16-byte packed decimal
00002078  E5C3D9D5 C6404040                        1573+          DC    CL8'VCRNF'         instruction name
00002080  00000010                                 1574+          DC    A(16)              result length
00002084  0000212C                                 1575+          DC    A(RE16)            address of expected resul
00002088  00000000 00000000                        1576+          DS    FD                 gap
00002090  00000000 00000000                        1577+V1O16     DS    XL16               V1 output
00002098  00000000 00000000
000020A0  00000000 00000000                        1578+          DS    FD                    gap
000020A8  00000000                                 1579+FPC_R_16 DS    F                  FPC after instruction
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000020B0  00000000 00000000                        1580+          DS    FD                    gap
000020B8  40404040 40404040                        1581+          DC    CL8' '             was cross check skipped?
000020C0  00000000 00000000                        1582+          DS    FD                    gap
000020C8  00000000 00000000                        1583+XCO16     DS    XL16               Cross check Output
000020D0  00000000 00000000
000020D8  00000000 00000000                        1584+          DS    XL16
000020E0  00000000 00000000
000020E8  00000000 00000000                        1585+          DS    FD                    gap
000020F0  00000000                                 1586+FPC_XC_16 DS    F                 1st cross check FPC
000020F4  00000000                                 1587+          DS    F                 2nd cross check FPC
000020F8  00000000 00000000                        1588+          DS    FD                    gap
00002100  00000000                                 1589+          DS    F                  debug area
00002104  00000000                                 1590+          DS    F
                                                   1591+*
00002108                                           1592+X16       DS    0F
00002108  B29D 852C                     0000072C   1593+          LFPC  FPCINIT            initialize FPC
                                                   1594+*          LFPC  =XL4'08000000'          set trap exception
0000210C  E320 500C 0014                00002074   1595+          LGF   R2,V2_16           get v2
00002112  E767 2000 0C36                00000000   1596+          VLM   V22,V23,0(R2)
00002118  E666 7002 0E75                           1597+          VCRNF V22,V22,V23,0,2       test instruction (dest is source)
0000211E  B29C 5040                     000020A8   1598+          STFPC FPC_R_16           save FPC
00002122  E760 5028 080E                00002090   1599+          VST   V22,V1O16          save instruction result
00002128  07FB                                     1600+          BR    R11                return
0000212C                                           1601+RE16      DS    0F                 expected 16 byte result
0000212C                                           1602+          DROP  R5
0000212C  50100000 00000000                        1603           DC    XL16'5010000000000000 D010000000000000'
00002134  D0100000 00000000
0000213C  4403F287 00000000                        1604           DC    XL16'4403F28700000000 0000000000000000'
00002144  00000000 00000000
0000214C  C403F287 00000000                        1605           DC    XL16'C403F28700000000 0000000000000000'
00002154  00000000 00000000
                                                   1606
                                                   1607 * +1055.5790, -1055.5790
                                                   1608           VRR_C VCRNF,0,2,00,00,S                 skip xc: lost digits
00002160                                           1609+          DS    0FD
00002160                        00002160           1610+          USING *,R5               base for test data and test routine
00002160  00002200                                 1611+T17       DC    A(X17)             address of test routine
00002164  0011                                     1612+          DC    H'17'              test number
00002166  00                                       1613+          DC    X'00'
00002167  E2                                       1614+          DC    CL1'S'             Y = skip cross check
00002168  00                                       1615+          DC    HL1'0'             m4
00002169  02                                       1616+          DC    HL1'2'             m5
0000216A  00                                       1617+FLG17     DC    X'00'              expected FPC flags
0000216B  00                                       1618+VXC17     DC    X'00'              expected VXC
0000216C  00002234                                 1619+V2_17     DC    A(RE17+16)         address of v2: 16-byte packed decimal
00002170  E5C3D9D5 C6404040                        1620+          DC    CL8'VCRNF'         instruction name
00002178  00000010                                 1621+          DC    A(16)              result length
0000217C  00002224                                 1622+          DC    A(RE17)            address of expected resul
00002180  00000000 00000000                        1623+          DS    FD                 gap
00002188  00000000 00000000                        1624+V1O17     DS    XL16               V1 output
00002190  00000000 00000000
00002198  00000000 00000000                        1625+          DS    FD                    gap
000021A0  00000000                                 1626+FPC_R_17  DS    F                  FPC after instruction
000021A8  00000000 00000000                        1627+          DS    FD                    gap
000021B0  40404040 40404040                        1628+          DC    CL8' '             was cross check skipped?
000021B8  00000000 00000000                        1629+          DS    FD                    gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000021C0  00000000 00000000                        1630+XCO17    DS    XL16              Cross check Output
000021C8  00000000 00000000
000021D0  00000000 00000000                        1631+         DS    XL16
000021D8  00000000 00000000
000021E0  00000000 00000000                        1632+         DS    FD                   gap
000021E8  00000000                                 1633+FPC_XC_17 DS   F                 1st cross check FPC
000021EC  00000000                                 1634+         DS    F                 2nd cross check FPC
000021F0  00000000 00000000                        1635+         DS    FD                   gap
000021F8  00000000                                 1636+         DS    F                 debug area
000021FC  00000000                                 1637+         DS    F
                                                   1638+*
00002200                                           1639+X17      DS    0F
00002200  B29D 852C                     0000072C   1640+         LFPC  FPCINIT           initialize FPC
                                                   1641+*         LFPC  =XL4'08000000'         set trap exception
00002204  E320 500C 0014                0000216C   1642+         LGF   R2,V2_17          get v2
0000220A  E767 2000 0C36                00000000   1643+         VLM   V22,V23,0(R2)
00002210  E666 7002 0E75                           1644+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
00002216  B29C 5040                     000021A0   1645+         STFPC FPC_R_17          save FPC
0000221A  E760 5028 080E                00002188   1646+         VST   V22,V1O17         save instruction result
00002220  07FB                                     1647+         BR    R11               return
00002224                                           1648+RE17     DS    0F                expected 16 byte result
00002224                                           1649+         DROP  R5
00002224  52100000 00000000                        1650          DC    XL16'521000000000000 D210000000000000'
0000222C  D2100000 00000000
00002234  4483F287 00000000                        1651          DC    XL16'4483F28700000000 0000000000000000'
0000223C  00000000 00000000
00002244  C483F287 00000000                        1652          DC    XL16'C483F28700000000 0000000000000000'
0000224C  00000000 00000000
                                                   1653
                                                   1654 * +Zero, -Zero
                                                   1655          VRR_C VCRNF,0,2,00,00,N
00002258                                           1656+         DS    0FD
00002258                        00002258           1657+         USING *,R5              base for test data and test routine
00002258  000022F8                                 1658+T18      DC    A(X18)            address of test routine
0000225C  0012                                     1659+         DC    H'18'             test number
0000225E  00                                       1660+         DC    X'00'
0000225F  D5                                       1661+         DC    CL1'N'            Y = skip cross check
00002260  00                                       1662+         DC    HL1'0'            m4
00002261  02                                       1663+         DC    HL1'2'            m5
00002262  00                                       1664+FLG18    DC    X'00'             expected FPC flags
00002263  00                                       1665+VXC18    DC    X'00'             expected VXC
00002264  0000232C                                 1666+V2_18    DC    A(RE18+16)        address of v2: 16-byte packed decimal
00002268  E5C3D9D5 C6404040                        1667+         DC    CL8'VCRNF'        instruction name
00002270  00000010                                 1668+         DC    A(16)             result length
00002274  0000231C                                 1669+         DC    A(RE18)           address of expected resul
00002278  00000000 00000000                        1670+         DS    FD                gap
00002280  00000000 00000000                        1671+V1O18    DS    XL16              V1 output
00002288  00000000 00000000
00002290  00000000 00000000                        1672+         DS    FD                   gap
00002298  00000000                                 1673+FPC_R_18 DS    F                 FPC after instruction
000022A0  00000000 00000000                        1674+         DS    FD                   gap
000022A8  40404040 40404040                        1675+         DC    CL8' '            was cross check skipped?
000022B0  00000000 00000000                        1676+         DS    FD                   gap
000022B8  00000000 00000000                        1677+XCO18    DS    XL16              Cross check Output
000022C0  00000000 00000000
000022C8  00000000 00000000                        1678+         DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000022D0  00000000 00000000
000022D8  00000000 00000000                        1679+         DS    FD                    gap
000022E0  00000000                                 1680+FPC_XC_18 DS   F                 1st cross check FPC
000022E4  00000000                                 1681+         DS    F                 2nd cross check FPC
000022E8  00000000 00000000                        1682+         DS    FD                    gap
000022F0  00000000                                 1683+         DS    F                  debug area
000022F4  00000000                                 1684+         DS    F
                                                   1685+*
000022F8                                           1686+X18      DS    0F
000022F8  B29D 852C                     0000072C   1687+         LFPC  FPCINIT            initialize FPC
                                                   1688+*         LFPC  =XL4'08000000'          set trap exception
000022FC  E320 500C 0014                00002264   1689+         LGF   R2,V2_18           get v2
00002302  E767 2000 0C36                00000000   1690+         VLM   V22,V23,0(R2)
00002308  E666 7002 0E75                           1691+         VCRNF V22,V22,V23,0,2        test instruction (dest is source)
0000230E  B29C 5040                     00002298   1692+         STFPC FPC_R_18           save FPC
00002312  E760 5028 080E                00002280   1693+         VST   V22,V1O18          save instruction result
00002318  07FB                                     1694+         BR    R11                return
0000231C                                           1695+RE18     DS    0F                 expected 16 byte result
0000231C                                           1696+         DROP  R5
0000231C  00000000 00000000                        1697          DC    XL16'0000000000000000 8000000000000000'
00002324  80000000 00000000
0000232C  00000000 00000000                        1698          DC    XL16'0000000000000000 0000000000000000'
00002334  00000000 00000000
0000233C  80000000 00000000                        1699          DC    XL16'8000000000000000 0000000000000000'
00002344  00000000 00000000
                                                   1700
                                                   1701 * +Normal, -Normal
                                                   1702          VRR_C VCRNF,0,2,00,00,N                 skip xc: lost digits
00002350                                           1703+         DS    0FD
00002350                        00002350           1704+         USING *,R5               base for test data and test routine
00002350  000023F0                                 1705+T19      DC    A(X19)             address of test routine
00002354  0013                                     1706+         DC    H'19'              test number
00002356  00                                       1707+         DC    X'00'
00002357  D5                                       1708+         DC    CL1'N'             Y = skip cross check
00002358  00                                       1709+         DC    HL1'0'             m4
00002359  02                                       1710+         DC    HL1'2'             m5
0000235A  00                                       1711+FLG19    DC    X'00'              expected FPC flags
0000235B  00                                       1712+VXC19    DC    X'00'              expected VXC
0000235C  00002424                                 1713+V2_19    DC    A(RE19+16)         address of v2: 16-byte packed decimal
00002360  E5C3D9D5 C6404040                        1714+         DC    CL8'VCRNF'         instruction name
00002368  00000010                                 1715+         DC    A(16)              result length
0000236C  00002414                                 1716+         DC    A(RE19)            address of expected resul
00002370  00000000 00000000                        1717+         DS    FD                 gap
00002378  00000000 00000000                        1718+V1O19    DS    XL16               V1 output
00002380  00000000 00000000
00002388  00000000 00000000                        1719+         DS    FD                    gap
00002390  00000000                                 1720+FPC_R_19 DS    F                  FPC after instruction
00002398  00000000 00000000                        1721+         DS    FD                    gap
000023A0  40404040 40404040                        1722+         DC    CL8' '             was cross check skipped?
000023A8  00000000 00000000                        1723+         DS    FD                    gap
000023B0  00000000 00000000                        1724+XCO19    DS    XL16               Cross check Output
000023B8  00000000 00000000
000023C0  00000000 00000000                        1725+         DS    XL16
000023C8  00000000 00000000
000023D0  00000000 00000000                        1726+         DS    FD                    gap
000023D8  00000000                                 1727+FPC_XC_19 DS   F                 1st cross check FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000023DC  00000000                                1728+         DS    F                 2nd cross check FPC
000023E0  00000000 00000000                       1729+         DS    FD                    gap
000023E8  00000000                                1730+         DS    F                  debug area
000023EC  00000000                                1731+         DS    F
                                                  1732+*
000023F0                                          1733+X19      DS    0F
000023F0  B29D 852C                     0000072C  1734+         LFPC  FPCINIT            initialize FPC
                                                  1735+*         LFPC  =XL4'08000000'          set trap exception
000023F4  E320 500C 0014                0000235C  1736+         LGF   R2,V2_19           get v2
000023FA  E767 2000 0C36                00000000  1737+         VLM   V22,V23,0(R2)
00002400  E666 7002 0E75                          1738+         VCRNF V22,V22,V23,0,2        test instruction (dest is source)
00002406  B29C 5040                     00002390  1739+         STFPC FPC_R_19           save FPC
0000240A  E760 5028 080E                00002378  1740+         VST   V22,V1O19          save instruction result
00002410  07FB                                    1741+         BR    R11                return
00002414                                          1742+RE19     DS    0F                 expected 16 byte result
00002414                                          1743+         DROP  R5
00002414  40800000 00000000                       1744          DC    XL16'4080000000000000 C080000000000000'
0000241C  C0800000 00000000
00002424  40200000 00000000                       1745          DC    XL16'4020000000000000 0000000000000000'
0000242C  00000000 00000000
00002434  C0200000 00000000                       1746          DC    XL16'C020000000000000 0000000000000000'
0000243C  00000000 00000000
                                                  1747
                                                  1748 * +Subnormal, -Subnormal
                                                  1749          VRR_C VCRNF,0,2,10,44,S                 skip xc: lost digits
00002448                                          1750+         DS    0FD
00002448                        00002448          1751+         USING *,R5               base for test data and test routine
00002448  000024E8                                1752+T20      DC    A(X20)             address of test routine
0000244C  0014                                    1753+         DC    H'20'              test number
0000244E  00                                      1754+         DC    X'00'
0000244F  E2                                      1755+         DC    CL1'S'             Y = skip cross check
00002450  00                                      1756+         DC    HL1'0'             m4
00002451  02                                      1757+         DC    HL1'2'             m5
00002452  10                                      1758+FLG20    DC    X'10'              expected FPC flags
00002453  44                                      1759+VXC20    DC    X'44'              expected VXC
00002454  0000251C                                1760+V2_20    DC    A(RE20+16)         address of v2: 16-byte packed decimal
00002458  E5C3D9D5 C6404040                       1761+         DC    CL8'VCRNF'         instruction name
00002460  00000010                                1762+         DC    A(16)              result length
00002464  0000250C                                1763+         DC    A(RE20)            address of expected resul
00002468  00000000 00000000                       1764+         DS    FD                 gap
00002470  00000000 00000000                       1765+V1O20    DS    XL16               V1 output
00002478  00000000 00000000
00002480  00000000 00000000                       1766+         DS    FD                    gap
00002488  00000000                                1767+FPC_R_20 DS    F                  FPC after instruction
00002490  00000000 00000000                       1768+         DS    FD                    gap
00002498  40404040 40404040                       1769+         DC    CL8' '             was cross check skipped?
000024A0  00000000 00000000                       1770+         DS    FD                    gap
000024A8  00000000 00000000                       1771+XCO20    DS    XL16               Cross check Output
000024B0  00000000 00000000
000024B8  00000000 00000000                       1772+         DS    XL16
000024C0  00000000 00000000
000024C8  00000000 00000000                       1773+         DS    FD                    gap
000024D0  00000000                                1774+FPC_XC_20 DS   F                 1st cross check FPC
000024D4  00000000                                1775+         DS    F                 2nd cross check FPC
000024D8  00000000 00000000                       1776+         DS    FD                    gap
000024E0  00000000                                1777+         DS    F                  debug area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000024E4  00000000                                1778+         DS    F
                                                  1779+*
000024E8                                          1780+X20      DS    0F
000024E8  B29D 852C                     0000072C  1781+         LFPC  FPCINIT           initialize FPC
                                                  1782+*         LFPC  =XL4'08000000'         set trap exception
000024EC  E320 500C 0014                00002454  1783+         LGF   R2,V2_20          get v2
000024F2  E767 2000 0C36                00000000  1784+         VLM   V22,V23,0(R2)
000024F8  E666 7002 0E75                          1785+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
000024FE  B29C 5040                     00002488  1786+         STFPC FPC_R_20          save FPC
00002502  E760 5028 080E                00002470  1787+         VST   V22,V1O20         save instruction result
00002508  07FB                                    1788+         BR    R11               return
0000250C                                          1789+RE20     DS    0F                expected 16 byte result
0000250C                                          1790+         DROP  R5
0000250C  00000000 00000000                       1791          DC    XL16'0000000000000000 8000000000000000'
00002514  80000000 00000000
0000251C  007FFFFF 00000000                       1792          DC    XL16'007FFFFF00000000 0000000000000000'
00002524  00000000 00000000
0000252C  807FFFFF 00000000                       1793          DC    XL16'807FFFFF00000000 0000000000000000'
00002534  00000000 00000000
                                                  1794
                                                  1795 * +Infinity, -Infinity
                                                  1796          VRR_C VCRNF,0,2,20,43,S                skip xc: lost digits
00002540                                          1797+         DS    0FD
00002540                        00002540          1798+         USING *,R5              base for test data and test routine
00002540  000025E0                                1799+T21      DC    A(X21)            address of test routine
00002544  0015                                    1800+         DC    H'21'             test number
00002546  00                                      1801+         DC    X'00'
00002547  E2                                      1802+         DC    CL1'S'            Y = skip cross check
00002548  00                                      1803+         DC    HL1'0'            m4
00002549  02                                      1804+         DC    HL1'2'            m5
0000254A  20                                      1805+FLG21    DC    X'20'             expected FPC flags
0000254B  43                                      1806+VXC21    DC    X'43'             expected VXC
0000254C  00002614                                1807+V2_21    DC    A(RE21+16)        address of v2: 16-byte packed decimal
00002550  E5C3D9D5 C6404040                       1808+         DC    CL8'VCRNF'        instruction name
00002558  00000010                                1809+         DC    A(16)             result length
0000255C  00002604                                1810+         DC    A(RE21)           address of expected resul
00002560  00000000 00000000                       1811+         DS    FD                gap
00002568  00000000 00000000                       1812+V1O21    DS    XL16              V1 output
00002570  00000000 00000000
00002578  00000000 00000000                       1813+         DS    FD                   gap
00002580  00000000                                1814+FPC_R_21 DS    F                 FPC after instruction
00002588  00000000 00000000                       1815+         DS    FD                   gap
00002590  40404040 40404040                       1816+         DC    CL8' '            was cross check skipped?
00002598  00000000 00000000                       1817+         DS    FD                   gap
000025A0  00000000 00000000                       1818+XCO21    DS    XL16              Cross check Output
000025A8  00000000 00000000
000025B0  00000000 00000000                       1819+         DS    XL16
000025B8  00000000 00000000
000025C0  00000000 00000000                       1820+         DS    FD                   gap
000025C8  00000000                                1821+FPC_XC_21 DS   F                1st cross check FPC
000025CC  00000000                                1822+         DS    F                2nd cross check FPC
000025D0  00000000 00000000                       1823+         DS    FD                   gap
000025D8  00000000                                1824+         DS    F                 debug area
000025DC  00000000                                1825+         DS    F
                                                  1826+*
000025E0                                          1827+X21      DS    0F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000025E0  B29D 852C                     0000072C  1828+         LFPC  FPCINIT           initialize FPC
                                                  1829+*         LFPC  =XL4'08000000'         set trap exception
000025E4  E320 500C 0014                0000254C  1830+         LGF   R2,V2_21          get v2
000025EA  E767 2000 0C36                00000000  1831+         VLM   V22,V23,0(R2)
000025F0  E666 7002 0E75                          1832+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
000025F6  B29C 5040                     00002580  1833+         STFPC FPC_R_21          save FPC
000025FA  E760 5028 080E                00002568  1834+         VST   V22,V1O21         save instruction result
00002600  07FB                                    1835+         BR    R11               return
00002604                                          1836+RE21     DS    0F                expected 16 byte result
00002604                                          1837+         DROP  R5
00002604  7FFF0000 00000000                       1838          DC    XL16'7FFF000000000000 FFFF000000000000'
0000260C  FFFF0000 00000000
00002614  7F800000 00000000                       1839          DC    XL16'7F80000000000000 0000000000000000'
0000261C  00000000 00000000
00002624  FF800000 00000000                       1840          DC    XL16'FF80000000000000 0000000000000000'
0000262C  00000000 00000000
                                                  1841
                                                  1842 * +QNaN, -QNaN
                                                  1843          VRR_C VCRNF,0,2,80,41,S                skip xc: lost digits
00002638                                          1844+         DS    0FD
00002638                        00002638          1845+         USING *,R5              base for test data and test routine
00002638  000026D8                                1846+T22      DC    A(X22)            address of test routine
0000263C  0016                                    1847+         DC    H'22'             test number
0000263E  00                                      1848+         DC    X'00'
0000263F  E2                                      1849+         DC    CL1'S'            Y = skip cross check
00002640  00                                      1850+         DC    HL1'0'            m4
00002641  02                                      1851+         DC    HL1'2'            m5
00002642  80                                      1852+FLG22    DC    X'80'             expected FPC flags
00002643  41                                      1853+VXC22    DC    X'41'             expected VXC
00002644  0000270C                                1854+V2_22    DC    A(RE22+16)        address of v2: 16-byte packed decimal
00002648  E5C3D9D5 C6404040                       1855+         DC    CL8'VCRNF'        instruction name
00002650  00000010                                1856+         DC    A(16)             result length
00002654  000026FC                                1857+         DC    A(RE22)           address of expected resul
00002658  00000000 00000000                       1858+         DS    FD                gap
00002660  00000000 00000000                       1859+V1O22    DS    XL16              V1 output
00002668  00000000 00000000
00002670  00000000 00000000                       1860+         DS    FD                   gap
00002678  00000000                                1861+FPC_R_22 DS    F                 FPC after instruction
00002680  00000000 00000000                       1862+         DS    FD                   gap
00002688  40404040 40404040                       1863+         DC    CL8' '            was cross check skipped?
00002690  00000000 00000000                       1864+         DS    FD                   gap
00002698  00000000 00000000                       1865+XCO22    DS    XL16              Cross check Output
000026A0  00000000 00000000
000026A8  00000000 00000000                       1866+         DS    XL16
000026B0  00000000 00000000
000026B8  00000000 00000000                       1867+         DS    FD                   gap
000026C0  00000000                                1868+FPC_XC_22 DS   F                1st cross check FPC
000026C4  00000000                                1869+         DS    F                2nd cross check FPC
000026C8  00000000 00000000                       1870+         DS    FD                   gap
000026D0  00000000                                1871+         DS    F                 debug area
000026D4  00000000                                1872+         DS    F
                                                  1873+*
000026D8                                          1874+X22      DS    0F
000026D8  B29D 852C                     0000072C  1875+         LFPC  FPCINIT           initialize FPC
                                                  1876+*         LFPC  =XL4'08000000'         set trap exception
000026DC  E320 500C 0014                00002644  1877+         LGF   R2,V2_22          get v2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000026E2  E767 2000 0C36                00000000  1878+         VLM   V22,V23,0(R2)
000026E8  E666 7002 0E75                          1879+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
000026EE  B29C 5040                     00002678  1880+         STFPC FPC_R_22          save FPC
000026F2  E760 5028 080E                00002660  1881+         VST   V22,V1O22         save instruction result
000026F8  07FB                                    1882+         BR    R11               return
000026FC                                          1883+RE22     DS    0F                expected 16 byte result
000026FC                                          1884+         DROP  R5
000026FC  7FFF0000 00000000                       1885          DC    XL16'7FFF000000000000 FFFF000000000000'
00002704  FFFF0000 00000000
0000270C  7FC10000 00000000                       1886          DC    XL16'7FC1000000000000 0000000000000000'
00002714  00000000 00000000
0000271C  FFC10000 00000000                       1887          DC    XL16'FFC1000000000000 0000000000000000'
00002724  00000000 00000000
                                                  1888
                                                  1889 * +SNaN, -SNaN
                                                  1890          VRR_C VCRNF,0,2,80,41,S                skip xc: lost digits
00002730                                          1891+         DS    0FD
00002730                        00002730          1892+         USING *,R5              base for test data and test routine
00002730  000027D0                                1893+T23      DC    A(X23)            address of test routine
00002734  0017                                    1894+         DC    H'23'             test number
00002736  00                                      1895+         DC    X'00'
00002737  E2                                      1896+         DC    CL1'S'            Y = skip cross check
00002738  00                                      1897+         DC    HL1'0'            m4
00002739  02                                      1898+         DC    HL1'2'            m5
0000273A  80                                      1899+FLG23    DC    X'80'             expected FPC flags
0000273B  41                                      1900+VXC23    DC    X'41'             expected VXC
0000273C  00002804                                1901+V2_23    DC    A(RE23+16)        address of v2: 16-byte packed decimal
00002740  E5C3D9D5 C6404040                       1902+         DC    CL8'VCRNF'        instruction name
00002748  00000010                                1903+         DC    A(16)             result length
0000274C  000027F4                                1904+         DC    A(RE23)           address of expected resul
00002750  00000000 00000000                       1905+         DS    FD                gap
00002758  00000000 00000000                       1906+V1O23    DS    XL16              V1 output
00002760  00000000 00000000
00002768  00000000 00000000                       1907+         DS    FD                   gap
00002770  00000000                                1908+FPC_R_23 DS    F                 FPC after instruction
00002778  00000000 00000000                       1909+         DS    FD                   gap
00002780  40404040 40404040                       1910+         DC    CL8' '            was cross check skipped?
00002788  00000000 00000000                       1911+         DS    FD                   gap
00002790  00000000 00000000                       1912+XCO23    DS    XL16              Cross check Output
00002798  00000000 00000000
000027A0  00000000 00000000                       1913+         DS    XL16
000027A8  00000000 00000000
000027B0  00000000 00000000                       1914+         DS    FD                   gap
000027B8  00000000                                1915+FPC_XC_23 DS   F                1st cross check FPC
000027BC  00000000                                1916+         DS    F                2nd cross check FPC
000027C0  00000000 00000000                       1917+         DS    FD                   gap
000027C8  00000000                                1918+         DS    F                 debug area
000027CC  00000000                                1919+         DS    F
                                                  1920+*
000027D0                                          1921+X23      DS    0F
000027D0  B29D 852C                     0000072C  1922+         LFPC  FPCINIT           initialize FPC
                                                  1923+*         LFPC  =XL4'08000000'          set trap exception
000027D4  E320 500C 0014                0000273C  1924+         LGF   R2,V2_23          get v2
000027DA  E767 2000 0C36                00000000  1925+         VLM   V22,V23,0(R2)
000027E0  E666 7002 0E75                          1926+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
000027E6  B29C 5040                     00002770  1927+         STFPC FPC_R_23          save FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000027EA  E760 5028 080E                00002758  1928+         VST   V22,V1O23         save instruction result
000027F0  07FB                                    1929+         BR    R11               return
000027F4                                          1930+RE23     DS    0F                expected 16 byte result
000027F4                                          1931+         DROP  R5
000027F4  7FFF0000 00000000                       1932          DC    XL16'7FFF000000000000 FFFF000000000000'
000027FC  FFFF0000 00000000
00002804  7F810000 00000000                       1933          DC    XL16'7F81000000000000 0000000000000000'
0000280C  00000000 00000000
00002814  FF810000 00000000                       1934          DC    XL16'FF81000000000000 0000000000000000'
0000281C  00000000 00000000
                                                  1935
                                                  1936 * Additional tests - multiple excecptions
                                                  1937 *-----------------------------------------------------------------
                                                  1938
                                                  1939 * +Subnormal, -Infinity
                                                  1940          VRR_C VCRNF,0,2,30,43,S                 skip xc: lost digits
00002828                                          1941+         DS    0FD
00002828                        00002828          1942+         USING *,R5              base for test data and test routine
00002828  000028C8                                1943+T24      DC    A(X24)            address of test routine
0000282C  0018                                    1944+         DC    H'24'             test number
0000282E  00                                      1945+         DC    X'00'
0000282F  E2                                      1946+         DC    CL1'S'            Y = skip cross check
00002830  00                                      1947+         DC    HL1'0'            m4
00002831  02                                      1948+         DC    HL1'2'            m5
00002832  30                                      1949+FLG24    DC    X'30'             expected FPC flags
00002833  43                                      1950+VXC24    DC    X'43'             expected VXC
00002834  000028FC                                1951+V2_24    DC    A(RE24+16)        address of v2: 16-byte packed decimal
00002838  E5C3D9D5 C6404040                       1952+         DC    CL8'VCRNF'        instruction name
00002840  00000010                                1953+         DC    A(16)             result length
00002844  000028EC                                1954+         DC    A(RE24)           address of expected resul
00002848  00000000 00000000                       1955+         DS    FD                gap
00002850  00000000 00000000                       1956+V1O24    DS    XL16              V1 output
00002858  00000000 00000000
00002860  00000000 00000000                       1957+         DS    FD                   gap
00002868  00000000                                1958+FPC_R_24 DS    F                 FPC after instruction
00002870  00000000 00000000                       1959+         DS    FD                   gap
00002878  40404040 40404040                       1960+         DC    CL8' '            was cross check skipped?
00002880  00000000 00000000                       1961+         DS    FD                   gap
00002888  00000000 00000000                       1962+XCO24    DS    XL16              Cross check Output
00002890  00000000 00000000
00002898  00000000 00000000                       1963+         DS    XL16
000028A0  00000000 00000000
000028A8  00000000 00000000                       1964+         DS    FD                   gap
000028B0  00000000                                1965+FPC_XC_24 DS   F                1st cross check FPC
000028B4  00000000                                1966+         DS    F                2nd cross check FPC
000028B8  00000000 00000000                       1967+         DS    FD                   gap
000028C0  00000000                                1968+         DS    F                 debug area
000028C4  00000000                                1969+         DS    F
                                                  1970+*
000028C8                                          1971+X24      DS    0F
000028C8  B29D 852C                     0000072C  1972+         LFPC  FPCINIT           initialize FPC
                                                  1973+*         LFPC  =XL4'08000000'         set trap exception
000028CC  E320 500C 0014                00002834  1974+         LGF   R2,V2_24          get v2
000028D2  E767 2000 0C36                00000000  1975+         VLM   V22,V23,0(R2)
000028D8  E666 7002 0E75                          1976+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
000028DE  B29C 5040                     00002868  1977+         STFPC FPC_R_24          save FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000028E2  E760 5028 080E                00002850 1978+         VST   V22,V1O24         save instruction result
000028E8  07FB                                   1979+         BR    R11               return
000028EC                                         1980+RE24     DS    0F                expected 16 byte result
000028EC                                         1981+         DROP  R5
000028EC  00000000 00000000                      1982          DC    XL16'0000000000000000 FFFF000000000000'
000028F4  FFFF0000 00000000
000028FC  007FFFFF 00000000                      1983          DC    XL16'007FFFFF00000000 0000000000000000'
00002904  00000000 00000000
0000290C  FF800000 00000000                      1984          DC    XL16'FF80000000000000 0000000000000000'
00002914  00000000 00000000
                                                 1985
                                                 1986 * -Infinity, +Subnormal
                                                 1987          VRR_C VCRNF,0,2,30,64,S                skip xc: lost digits
00002920                                         1988+         DS    0FD
00002920                      00002920           1989+         USING *,R5              base for test data and test routine
00002920  000029C0                               1990+T25      DC    A(X25)            address of test routine
00002924  0019                                   1991+         DC    H'25'             test number
00002926  00                                     1992+         DC    X'00'
00002927  E2                                     1993+         DC    CL1'S'            Y = skip cross check
00002928  00                                     1994+         DC    HL1'0'            m4
00002929  02                                     1995+         DC    HL1'2'            m5
0000292A  30                                     1996+FLG25    DC    X'30'             expected FPC flags
0000292B  64                                     1997+VXC25    DC    X'64'             expected VXC
0000292C  000029F4                               1998+V2_25    DC    A(RE25+16)        address of v2: 16-byte packed decimal
00002930  E5C3D9D5 C6404040                      1999+         DC    CL8'VCRNF'        instruction name
00002938  00000010                               2000+         DC    A(16)             result length
0000293C  000029E4                               2001+         DC    A(RE25)           address of expected resul
00002940  00000000 00000000                      2002+         DS    FD                gap
00002948  00000000 00000000                      2003+V1O25    DS    XL16              V1 output
00002950  00000000 00000000
00002958  00000000 00000000                      2004+         DS    FD                   gap
00002960  00000000                               2005+FPC_R_25 DS    F                 FPC after instruction
00002968  00000000 00000000                      2006+         DS    FD                   gap
00002970  40404040 40404040                      2007+         DC    CL8' '            was cross check skipped?
00002978  00000000 00000000                      2008+         DS    FD                   gap
00002980  00000000 00000000                      2009+XCO25    DS    XL16              Cross check Output
00002988  00000000 00000000
00002990  00000000 00000000                      2010+         DS    XL16
00002998  00000000 00000000
000029A0  00000000 00000000                      2011+         DS    FD                   gap
000029A8  00000000                               2012+FPC_XC_25 DS   F                1st cross check FPC
000029AC  00000000                               2013+         DS    F                2nd cross check FPC
000029B0  00000000 00000000                      2014+         DS    FD                   gap
000029B8  00000000                               2015+         DS    F                 debug area
000029BC  00000000                               2016+         DS    F
                                                 2017+*
000029C0                                         2018+X25      DS    0F
000029C0  B29D 852C                   0000072C   2019+         LFPC  FPCINIT           initialize FPC
                                                 2020+*         LFPC  =XL4'08000000'          set trap exception
000029C4  E320 500C 0014              0000292C   2021+         LGF   R2,V2_25          get v2
000029CA  E767 2000 0C36              00000000   2022+         VLM   V22,V23,0(R2)
000029D0  E666 7002 0E75                         2023+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
000029D6  B29C 5040                   00002960   2024+         STFPC FPC_R_25          save FPC
000029DA  E760 5028 080E              00002948   2025+         VST   V22,V1O25         save instruction result
000029E0  07FB                                   2026+         BR    R11               return
000029E4                                         2027+RE25     DS    0F                expected 16 byte result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000029E4                                           2028+         DROP  R5
000029E4  00000000 00000000                        2029          DC    XL16'0000000000000000 FFFF000000000000'
000029EC  FFFF0000 00000000
000029F4  00000000 00000000                        2030          DC    XL16'0000000000000000 0000000000000000'
000029FC  00000000 00000000
00002A04  FF800000 00000000                        2031          DC    XL16'FF80000000000000 007FFFFF00000000'
00002A0C  007FFFFF 00000000
                                                   2032
                                                   2033 * +Infinity, -QNaN
                                                   2034          VRR_C VCRNF,0,2,A0,41,S                skip xc: lost digits
00002A18                                           2035+         DS    0FD
00002A18                       00002A18            2036+         USING *,R5              base for test data and test routine
00002A18  00002AB8                                 2037+T26      DC    A(X26)            address of test routine
00002A1C  001A                                     2038+         DC    H'26'             test number
00002A1E  00                                       2039+         DC    X'00'
00002A1F  E2                                       2040+         DC    CL1'S'            Y = skip cross check
00002A20  00                                       2041+         DC    HL1'0'            m4
00002A21  02                                       2042+         DC    HL1'2'            m5
00002A22  A0                                       2043+FLG26    DC    X'A0'             expected FPC flags
00002A23  41                                       2044+VXC26    DC    X'41'             expected VXC
00002A24  00002AEC                                 2045+V2_26    DC    A(RE26+16)        address of v2: 16-byte packed decimal
00002A28  E5C3D9D5 C6404040                        2046+         DC    CL8'VCRNF'        instruction name
00002A30  00000010                                 2047+         DC    A(16)             result length
00002A34  00002ADC                                 2048+         DC    A(RE26)           address of expected resul
00002A38  00000000 00000000                        2049+         DS    FD                gap
00002A40  00000000 00000000                        2050+V1O26    DS    XL16              V1 output
00002A48  00000000 00000000
00002A50  00000000 00000000                        2051+         DS    FD                   gap
00002A58  00000000                                 2052+FPC_R_26 DS    F                 FPC after instruction
00002A60  00000000 00000000                        2053+         DS    FD                   gap
00002A68  40404040 40404040                        2054+         DC    CL8' '            was cross check skipped?
00002A70  00000000 00000000                        2055+         DS    FD                   gap
00002A78  00000000 00000000                        2056+XCO26    DS    XL16              Cross check Output
00002A80  00000000 00000000
00002A88  00000000 00000000                        2057+         DS    XL16
00002A90  00000000 00000000
00002A98  00000000 00000000                        2058+         DS    FD                   gap
00002AA0  00000000                                 2059+FPC_XC_26 DS   F                1st cross check FPC
00002AA4  00000000                                 2060+         DS    F                2nd cross check FPC
00002AA8  00000000 00000000                        2061+         DS    FD                   gap
00002AB0  00000000                                 2062+         DS    F                 debug area
00002AB4  00000000                                 2063+         DS    F
                                                   2064+*
00002AB8                                           2065+X26      DS    0F
00002AB8  B29D 852C                    0000072C    2066+         LFPC  FPCINIT           initialize FPC
                                                   2067+*         LFPC  =XL4'08000000'          set trap exception
00002ABC  E320 500C 0014               00002A24    2068+         LGF   R2,V2_26          get v2
00002AC2  E767 2000 0C36               00000000    2069+         VLM   V22,V23,0(R2)
00002AC8  E666 7002 0E75                           2070+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
00002ACE  B29C 5040                    00002A58    2071+         STFPC FPC_R_26          save FPC
00002AD2  E760 5028 080E               00002A40    2072+         VST   V22,V1O26         save instruction result
00002AD8  07FB                                     2073+         BR    R11               return
00002ADC                                           2074+RE26     DS    0F                expected 16 byte result
00002ADC                                           2075+         DROP  R5
00002ADC  7FFF0000 00000000                        2076          DC    XL16'7FFF000000000000 FFFF000000000000'
00002AE4  FFFF0000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002AEC  7F800000 00000000                        2077          DC    XL16'7F80000000000000 0000000000000000'
00002AF4  00000000 00000000
00002AFC  FFC10000 00000000                        2078          DC    XL16'FFC1000000000000 0000000000000000'
00002B04  00000000 00000000
                                                   2079
                                                   2080 * +Infinity, -QNaN, +Infinity
                                                   2081          VRR_C VCRNF,0,2,A0,63,S                skip xc: lost digits
00002B10                                           2082+         DS    0FD
00002B10                       00002B10            2083+         USING *,R5              base for test data and test routine
00002B10  00002BB0                                 2084+T27      DC    A(X27)            address of test routine
00002B14  001B                                     2085+         DC    H'27'             test number
00002B16  00                                       2086+         DC    X'00'
00002B17  E2                                       2087+         DC    CL1'S'            Y = skip cross check
00002B18  00                                       2088+         DC    HL1'0'            m4
00002B19  02                                       2089+         DC    HL1'2'            m5
00002B1A  A0                                       2090+FLG27    DC    X'A0'             expected FPC flags
00002B1B  63                                       2091+VXC27    DC    X'63'             expected VXC
00002B1C  00002BE4                                 2092+V2_27    DC    A(RE27+16)        address of v2: 16-byte packed decimal
00002B20  E5C3D9D5 C6404040                        2093+         DC    CL8'VCRNF'        instruction name
00002B28  00000010                                 2094+         DC    A(16)             result length
00002B2C  00002BD4                                 2095+         DC    A(RE27)           address of expected resul
00002B30  00000000 00000000                        2096+         DS    FD                gap
00002B38  00000000 00000000                        2097+V1O27    DS    XL16              V1 output
00002B40  00000000 00000000
00002B48  00000000 00000000                        2098+         DS    FD                   gap
00002B50  00000000                                 2099+FPC_R_27 DS    F                 FPC after instruction
00002B58  00000000 00000000                        2100+         DS    FD                   gap
00002B60  40404040 40404040                        2101+         DC    CL8' '            was cross check skipped?
00002B68  00000000 00000000                        2102+         DS    FD                   gap
00002B70  00000000 00000000                        2103+XCO27    DS    XL16              Cross check Output
00002B78  00000000 00000000
00002B80  00000000 00000000                        2104+         DS    XL16
00002B88  00000000 00000000
00002B90  00000000 00000000                        2105+         DS    FD                   gap
00002B98  00000000                                 2106+FPC_XC_27 DS   F                1st cross check FPC
00002B9C  00000000                                 2107+         DS    F                2nd cross check FPC
00002BA0  00000000 00000000                        2108+         DS    FD                   gap
00002BA8  00000000                                 2109+         DS    F                 debug area
00002BAC  00000000                                 2110+         DS    F
                                                   2111+*
00002BB0                                           2112+X27      DS    0F
00002BB0  B29D 852C                     0000072C   2113+         LFPC  FPCINIT           initialize FPC
                                                   2114+*         LFPC  =XL4'08000000'          set trap exception
00002BB4  E320 500C 0014                00002B1C   2115+         LGF   R2,V2_27          get v2
00002BBA  E767 2000 0C36                00000000   2116+         VLM   V22,V23,0(R2)
00002BC0  E666 7002 0E75                           2117+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
00002BC6  B29C 5040                     00002B50   2118+         STFPC FPC_R_27          save FPC
00002BCA  E760 5028 080E                00002B38   2119+         VST   V22,V1O27         save instruction result
00002BD0  07FB                                     2120+         BR    R11               return
00002BD4                                           2121+RE27     DS    0F                expected 16 byte result
00002BD4                                           2122+         DROP  R5
00002BD4  7FFF0000 00000000                        2123          DC    XL16'7FFF000000000000 FFFF00007FFF0000'
00002BDC  FFFF0000 7FFF0000
00002BE4  7F800000 00000000                        2124          DC    XL16'7F80000000000000 0000000000000000'
00002BEC  00000000 00000000
00002BF4  FFC10000 00000000                        2125          DC    XL16'FFC1000000000000 7F80000000000000'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002BFC  7F800000 00000000
                                                  2126
                                                  2127 * +Infinity, -QNaN, +Subnormal
                                                  2128          VRR_C VCRNF,0,2,B0,64,S                 skip xc: lost digits
00002C08                                          2129+         DS    0FD
00002C08                      00002C08            2130+         USING *,R5              base for test data and test routine
00002C08  00002CA8                                2131+T28      DC    A(X28)            address of test routine
00002C0C  001C                                    2132+         DC    H'28'             test number
00002C0E  00                                      2133+         DC    X'00'
00002C0F  E2                                      2134+         DC    CL1'S'            Y = skip cross check
00002C10  00                                      2135+         DC    HL1'0'            m4
00002C11  02                                      2136+         DC    HL1'2'            m5
00002C12  B0                                      2137+FLG28    DC    X'B0'             expected FPC flags
00002C13  64                                      2138+VXC28    DC    X'64'             expected VXC
00002C14  00002CDC                                2139+V2_28    DC    A(RE28+16)        address of v2: 16-byte packed decimal
00002C18  E5C3D9D5 C6404040                       2140+         DC    CL8'VCRNF'        instruction name
00002C20  00000010                                2141+         DC    A(16)             result length
00002C24  00002CCC                                2142+         DC    A(RE28)           address of expected resul
00002C28  00000000 00000000                       2143+         DS    FD                gap
00002C30  00000000 00000000                       2144+V1O28    DS    XL16              V1 output
00002C38  00000000 00000000
00002C40  00000000 00000000                       2145+         DS    FD                   gap
00002C48  00000000                                2146+FPC_R_28 DS    F                 FPC after instruction
00002C50  00000000 00000000                       2147+         DS    FD                   gap
00002C58  40404040 40404040                       2148+         DC    CL8' '            was cross check skipped?
00002C60  00000000 00000000                       2149+         DS    FD                   gap
00002C68  00000000 00000000                       2150+XCO28    DS    XL16              Cross check Output
00002C70  00000000 00000000
00002C78  00000000 00000000                       2151+         DS    XL16
00002C80  00000000 00000000
00002C88  00000000 00000000                       2152+         DS    FD                   gap
00002C90  00000000                                2153+FPC_XC_28 DS   F                1st cross check FPC
00002C94  00000000                                2154+         DS    F                2nd cross check FPC
00002C98  00000000 00000000                       2155+         DS    FD                   gap
00002CA0  00000000                                2156+         DS    F                 debug area
00002CA4  00000000                                2157+         DS    F
                                                  2158+*
00002CA8                                          2159+X28      DS    0F
00002CA8  B29D 852C                   0000072C    2160+         LFPC  FPCINIT           initialize FPC
                                                  2161+*         LFPC  =XL4'08000000'         set trap exception
00002CAC  E320 500C 0014              00002C14    2162+         LGF   R2,V2_28          get v2
00002CB2  E767 2000 0C36              00000000    2163+         VLM   V22,V23,0(R2)
00002CB8  E666 7002 0E75                          2164+         VCRNF V22,V22,V23,0,2       test instruction (dest is source)
00002CBE  B29C 5040                   00002C48    2165+         STFPC FPC_R_28          save FPC
00002CC2  E760 5028 080E              00002C30    2166+         VST   V22,V1O28         save instruction result
00002CC8  07FB                                    2167+         BR    R11               return
00002CCC                                          2168+RE28     DS    0F                expected 16 byte result
00002CCC                                          2169+         DROP  R5
00002CCC  7FFF0000 00000000                       2170          DC    XL16'7FFF000000000000 FFFF000000000000'
00002CD4  FFFF0000 00000000
00002CDC  7F800000 00000000                       2171          DC    XL16'7F80000000000000 0000000000000000'
00002CE4  00000000 00000000
00002CEC  FFC10000 00000000                       2172          DC    XL16'FFC1000000000000 007FFFFF00000000'
00002CF4  007FFFFF 00000000
                                                  2173
                                                  2174
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002CFC  00000000                                2175          DC    F'0'     END OF TABLE
00002D00  00000000                                2176          DC    F'0'
                                                  2177 *
                                                  2178 * table of pointers to individual tests
                                                  2179 *
00002D04                                          2180 E6TESTS  DS    0F
                                                  2181          PTTABLE
00002D04                                          2182+TTABLE   DS    0F
00002D04  000011E0                                2183+         DC    A(T1)              TEST &CUR
00002D08  000012D8                                2184+         DC    A(T2)              TEST &CUR
00002D0C  000013D0                                2185+         DC    A(T3)              TEST &CUR
00002D10  000014C8                                2186+         DC    A(T4)              TEST &CUR
00002D14  000015C0                                2187+         DC    A(T5)              TEST &CUR
00002D18  000016B8                                2188+         DC    A(T6)              TEST &CUR
00002D1C  000017B0                                2189+         DC    A(T7)              TEST &CUR
00002D20  000018A8                                2190+         DC    A(T8)              TEST &CUR
00002D24  000019A0                                2191+         DC    A(T9)              TEST &CUR
00002D28  00001A98                                2192+         DC    A(T10)             TEST &CUR
00002D2C  00001B90                                2193+         DC    A(T11)             TEST &CUR
00002D30  00001C88                                2194+         DC    A(T12)             TEST &CUR
00002D34  00001D80                                2195+         DC    A(T13)             TEST &CUR
00002D38  00001E78                                2196+         DC    A(T14)             TEST &CUR
00002D3C  00001F70                                2197+         DC    A(T15)             TEST &CUR
00002D40  00002068                                2198+         DC    A(T16)             TEST &CUR
00002D44  00002160                                2199+         DC    A(T17)             TEST &CUR
00002D48  00002258                                2200+         DC    A(T18)             TEST &CUR
00002D4C  00002350                                2201+         DC    A(T19)             TEST &CUR
00002D50  00002448                                2202+         DC    A(T20)             TEST &CUR
00002D54  00002540                                2203+         DC    A(T21)             TEST &CUR
00002D58  00002638                                2204+         DC    A(T22)             TEST &CUR
00002D5C  00002730                                2205+         DC    A(T23)             TEST &CUR
00002D60  00002828                                2206+         DC    A(T24)             TEST &CUR
00002D64  00002920                                2207+         DC    A(T25)             TEST &CUR
00002D68  00002A18                                2208+         DC    A(T26)             TEST &CUR
00002D6C  00002B10                                2209+         DC    A(T27)             TEST &CUR
00002D70  00002C08                                2210+         DC    A(T28)             TEST &CUR
                                                  2211+*
00002D74  00000000                                2212+         DC    A(0)               END OF TABLE
00002D78  00000000                                2213+         DC    A(0)
                                                  2214
00002D7C  00000000                                2215          DC    F'0'     END OF TABLE
00002D80  00000000                                2216          DC    F'0'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                          2218 ************************************************************************
                                          2219 *        Register equates
                                          2220 ************************************************************************


                             00000000  00000001  2222 R0       EQU   0
                             00000001  00000001  2223 R1       EQU   1
                             00000002  00000001  2224 R2       EQU   2
                             00000003  00000001  2225 R3       EQU   3
                             00000004  00000001  2226 R4       EQU   4
                             00000005  00000001  2227 R5       EQU   5
                             00000006  00000001  2228 R6       EQU   6
                             00000007  00000001  2229 R7       EQU   7
                             00000008  00000001  2230 R8       EQU   8
                             00000009  00000001  2231 R9       EQU   9
                             0000000A  00000001  2232 R10      EQU   10
                             0000000B  00000001  2233 R11      EQU   11
                             0000000C  00000001  2234 R12      EQU   12
                             0000000D  00000001  2235 R13      EQU   13
                             0000000E  00000001  2236 R14      EQU   14
                             0000000F  00000001  2237 R15      EQU   15


                                          2239 ************************************************************************
                                          2240 *        Register equates
                                          2241 ************************************************************************


                             00000000  00000001  2243 FPR0     EQU   0
                             00000001  00000001  2244 FPR1     EQU   1
                             00000002  00000001  2245 FPR2     EQU   2
                             00000003  00000001  2246 FPR3     EQU   3
                             00000004  00000001  2247 FPR4     EQU   4
                             00000005  00000001  2248 FPR5     EQU   5
                             00000006  00000001  2249 FPR6     EQU   6
                             00000007  00000001  2250 FPR7     EQU   7
                             00000008  00000001  2251 FPR8     EQU   8
                             00000009  00000001  2252 FPR9     EQU   9
                             0000000A  00000001  2253 FPR10    EQU   10
                             0000000B  00000001  2254 FPR11    EQU   11
                             0000000C  00000001  2255 FPR12    EQU   12
                             0000000D  00000001  2256 FPR13    EQU   13
                             0000000E  00000001  2257 FPR14    EQU   14
                             0000000F  00000001  2258 FPR15    EQU   15


                                          2260 ************************************************************************
                                          2261 *        Register equates
                                          2262 ************************************************************************


                             00000000  00000001  2264 V0       EQU   0
                             00000001  00000001  2265 V1       EQU   1
                             00000002  00000001  2266 V2       EQU   2
                             00000003  00000001  2267 V3       EQU   3
                             00000004  00000001  2268 V4       EQU   4
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

                               00000005  00000001  2269 V5       EQU   5
                               00000006  00000001  2270 V6       EQU   6
                               00000007  00000001  2271 V7       EQU   7
                               00000008  00000001  2272 V8       EQU   8
                               00000009  00000001  2273 V9       EQU   9
                               0000000A  00000001  2274 V10      EQU   10
                               0000000B  00000001  2275 V11      EQU   11
                               0000000C  00000001  2276 V12      EQU   12
                               0000000D  00000001  2277 V13      EQU   13
                               0000000E  00000001  2278 V14      EQU   14
                               0000000F  00000001  2279 V15      EQU   15
                               00000010  00000001  2280 V16      EQU   16
                               00000011  00000001  2281 V17      EQU   17
                               00000012  00000001  2282 V18      EQU   18
                               00000013  00000001  2283 V19      EQU   19
                               00000014  00000001  2284 V20      EQU   20
                               00000015  00000001  2285 V21      EQU   21
                               00000016  00000001  2286 V22      EQU   22
                               00000017  00000001  2287 V23      EQU   23
                               00000018  00000001  2288 V24      EQU   24
                               00000019  00000001  2289 V25      EQU   25
                               0000001A  00000001  2290 V26      EQU   26
                               0000001B  00000001  2291 V27      EQU   27
                               0000001C  00000001  2292 V28      EQU   28
                               0000001D  00000001  2293 V29      EQU   29
                               0000001E  00000001  2294 V30      EQU   30
                               0000001F  00000001  2295 V31      EQU   31
                                                   2296
                                                   2297          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
BEGIN	I	00000200	2	172	136	168	169	170									
CHECKRES	U	00000324	1	252	249												
CHECKVXC	U	00000316	1	247	244												
CTLR0	F	00000724	4	570	182	183	184	185									
DECNUM	C	00001190	16	691	326	328	335	337	342	344	373	375	382	384	389	391	409
					411	418	420	425	427	446	448	455	457	462	464		
DONEXT	U	00000346	1	266	260												
E6TEST	4	00000000	160	705	231												
E6TESTS	F	00002D04	4	2180	224												
EDIT	X	00001164	18	686	327	336	343	374	383	390	410	419	426	447	456	463	
ENDTEST	U	000005F4	1	484	229												
EOJ	I	00000708	4	560	217	487											
EOJPSW	D	000006F8	8	558	560												
FAILCONT	U	000005E4	1	474													
FAILED	F	00001000	4	606	323	354	370	406	443	476	485						
FAILMSG	U	00000574	1	441	264												
FAILPSW	D	00000710	8	562	564												
FAILTEST	I	00000720	4	564	488												
FB0001	F	00000298	8	201	205	206	208										
FLG	X	0000000A	1	712	243	381											
FLG1	X	000011EA	1	863													
FLG10	X	00001AA2	1	1286													
FLG11	X	00001B9A	1	1333													
FLG12	X	00001C92	1	1380													
FLG13	X	00001D8A	1	1427													
FLG14	X	00001E82	1	1476													
FLG15	X	00001F7A	1	1523													
FLG16	X	00002072	1	1570													
FLG17	X	0000216A	1	1617													
FLG18	X	00002262	1	1664													
FLG19	X	0000235A	1	1711													
FLG2	X	000012E2	1	910													
FLG20	X	00002452	1	1758													
FLG21	X	0000254A	1	1805													
FLG22	X	00002642	1	1852													
FLG23	X	0000273A	1	1899													
FLG24	X	00002832	1	1949													
FLG25	X	0000292A	1	1996													
FLG26	X	00002A22	1	2043													
FLG27	X	00002B1A	1	2090													
FLG28	X	00002C12	1	2137													
FLG3	X	000013DA	1	957													
FLG4	X	000014D2	1	1004													
FLG5	X	000015CA	1	1051													
FLG6	X	000016C2	1	1098													
FLG7	X	000017BA	1	1145													
FLG8	X	000018B2	1	1192													
FLG9	X	000019AA	1	1239													
FPCINIT	X	0000072C	4	572	294	301	886	933	980	1027	1074	1121	1168	1215	1262	1309	1356
					1403	1450	1499	1546	1593	1640	1687	1734	1781	1828	1875	1922	1972
					2019	2066	2113	2160									
FPCMSG	U	00000490	1	368	245												
FPCPEXP	C	00001052	3	621	385												
FPCPGOT	C	00001067	3	624	392												
FPCPLINE	C	00001008	13	616	626	395											
FPCPLNG	U	00000063	1	626	394												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES					
FPCPNAME	C	00001039	8	619	378					
FPCPNUM	C	00001015	3	617	376					
FPC_R	F	00000040	4	721	243	248	257	278	388	424
FPC_R_1	F	00001220	4	872	891					
FPC_R_10	F	00001AD8	4	1295	1314					
FPC_R_11	F	00001BD0	4	1342	1361					
FPC_R_12	F	00001CC8	4	1389	1408					
FPC_R_13	F	00001DC0	4	1436	1455					
FPC_R_14	F	00001EB8	4	1485	1504					
FPC_R_15	F	00001FB0	4	1532	1551					
FPC_R_16	F	000020A8	4	1579	1598					
FPC_R_17	F	000021A0	4	1626	1645					
FPC_R_18	F	00002298	4	1673	1692					
FPC_R_19	F	00002390	4	1720	1739					
FPC_R_2	F	00001318	4	919	938					
FPC_R_20	F	00002488	4	1767	1786					
FPC_R_21	F	00002580	4	1814	1833					
FPC_R_22	F	00002678	4	1861	1880					
FPC_R_23	F	00002770	4	1908	1927					
FPC_R_24	F	00002868	4	1958	1977					
FPC_R_25	F	00002960	4	2005	2024					
FPC_R_26	F	00002A58	4	2052	2071					
FPC_R_27	F	00002B50	4	2099	2118					
FPC_R_28	F	00002C48	4	2146	2165					
FPC_R_3	F	00001410	4	966	985					
FPC_R_4	F	00001508	4	1013	1032					
FPC_R_5	F	00001600	4	1060	1079					
FPC_R_6	F	000016F8	4	1107	1126					
FPC_R_7	F	000017F0	4	1154	1173					
FPC_R_8	F	000018E8	4	1201	1220					
FPC_R_9	F	000019E0	4	1248	1267					
FPC_XC1	F	00000088	4	728	298	308				
FPC_XC2	F	0000008C	4	729	305	311				
FPC_XC_1	F	00001268	4	879						
FPC_XC_10	F	00001B20	4	1302						
FPC_XC_11	F	00001C18	4	1349						
FPC_XC_12	F	00001D10	4	1396						
FPC_XC_13	F	00001E08	4	1443						
FPC_XC_14	F	00001F00	4	1492						
FPC_XC_15	F	00001FF8	4	1539						
FPC_XC_16	F	000020F0	4	1586						
FPC_XC_17	F	000021E8	4	1633						
FPC_XC_18	F	000022E0	4	1680						
FPC_XC_19	F	000023D8	4	1727						
FPC_XC_2	F	00001360	4	926						
FPC_XC_20	F	000024D0	4	1774						
FPC_XC_21	F	000025C8	4	1821						
FPC_XC_22	F	000026C0	4	1868						
FPC_XC_23	F	000027B8	4	1915						
FPC_XC_24	F	000028B0	4	1965						
FPC_XC_25	F	000029A8	4	2012						
FPC_XC_26	F	00002AA0	4	2059						
FPC_XC_27	F	00002B98	4	2106						
FPC_XC_28	F	00002C90	4	2153						
FPC_XC_3	F	00001458	4	973						
FPC_XC_4	F	00001550	4	1020						

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
FPC_XC_5	F	00001648	4	1067													
FPC_XC_6	F	00001740	4	1114													
FPC_XC_7	F	00001838	4	1161													
FPC_XC_8	F	00001930	4	1208													
FPC_XC_9	F	00001A28	4	1255													
FPR0	U	00000000	1	2243													
FPR1	U	00000001	1	2244													
FPR10	U	0000000A	1	2253													
FPR11	U	0000000B	1	2254													
FPR12	U	0000000C	1	2255													
FPR13	U	0000000D	1	2256													
FPR14	U	0000000E	1	2257													
FPR15	U	0000000F	1	2258													
FPR2	U	00000002	1	2245													
FPR3	U	00000003	1	2246													
FPR4	U	00000004	1	2247													
FPR5	U	00000005	1	2248													
FPR6	U	00000006	1	2249													
FPR7	U	00000007	1	2250													
FPR8	U	00000008	1	2251													
FPR9	U	00000009	1	2252													
IMAGE	1	00000000	11652	0													
K	U	00000400	1	589	590	591	592										
K64	U	00010000	1	591													
M4	U	00000008	1	710	334	454											
M5	U	00000009	1	711	341	461											
MB	U	00100000	1	592													
MSG	I	00000638	4	520	216	503											
MSGCMD	C	00000686	9	550	533	534											
MSGMSG	C	0000068F	100	551	527	548	525										
MSGMVC	I	00000680	6	548	531												
MSGOK	I	0000064E	2	529	526												
MSGRET	I	0000066E	4	544	537	540											
MSGSAVE	F	00000674	4	547	523	544											
NEXTE6	U	000002EC	1	226	268	479											
OPNAME	C	00000010	8	715	284	331	378	414	451								
PAGE	U	00001000	1	590													
PRT3	C	0000117A	18	689	327	328	329	336	337	338	343	344	345	374	375	376	383
					384	385	390	391	392	410	411	412	419	420	421	426	427
					428	447	448	449	456	457	458	463	464	465			
PRTLINE	C	000010CE	13	654	664	468											
PRTLNG	U	00000048	1	664	467												
PRTM4	C	00001107	2	659	458												
PRTM5	C	00001113	2	662	465												
PRTNAME	C	000010F6	8	657	451												
PRTNUM	C	000010DB	3	655	449												
R0	U	00000000	1	2222	130	182	185	205	207	208	209	214	233	234	322	323	348
					353	354	369	370	394	405	406	430	442	443	467	475	476
					502	504	520	523	525	527	529	544					
R1	U	00000001	1	2223	215	256	257	258	259	262	263	314	315	349	395	431	468
					485	486	534	548									
R10	U	0000000A	1	2232	170	179	180										
R11	U	0000000B	1	2233	236	237	893	940	987	1034	1081	1128	1175	1222	1269	1316	1363
					1410	1457	1506	1553	1600	1647	1694	1741	1788	1835	1882	1929	1979
					2026	2073	2120	2167									
R12	U	0000000C	1	2234	224	227	267	478									

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
R13	U	0000000D	1	2235													
R14	U	0000000E	1	2236													
R15	U	0000000F	1	2237	239	277	279	289	309	312	317	347	350	351	355	396	432
					469	497	507	508									
R2	U	00000002	1	2224	216	325	326	333	334	335	340	341	342	372	373	380	381
					382	387	388	389	408	409	416	417	418	423	424	425	445
					446	453	454	455	460	461	462	502	503	504	521	523	529
					530	531	533	539	544	545	888	889	935	936	982	983	1029
					1030	1076	1077	1123	1124	1170	1171	1217	1218	1264	1265	1311	1312
					1358	1359	1405	1406	1452	1453	1501	1502	1548	1549	1595	1596	1642
					1643	1689	1690	1736	1737	1783	1784	1830	1831	1877	1878	1924	1925
					1974	1975	2021	2022	2068	2069	2115	2116	2162	2163			
R3	U	00000003	1	2225													
R4	U	00000004	1	2226													
R5	U	00000005	1	2227	227	228	231	498	506	856	895	903	942	950	989	997	1036
					1044	1083	1091	1130	1138	1177	1185	1224	1232	1271	1279	1318	1326
					1365	1373	1412	1420	1459	1469	1508	1516	1555	1563	1602	1610	1649
					1657	1696	1704	1743	1751	1790	1798	1837	1845	1884	1892	1931	1942
					1981	1989	2028	2036	2075	2083	2122	2130	2169				
R6	U	00000006	1	2228													
R7	U	00000007	1	2229	245	250	397	433									
R8	U	00000008	1	2230	168	172	173	174	176								
R9	U	00000009	1	2231	169	176	177	179									
RE1	F	000012A4	4	894	865	868											
RE10	F	00001B5C	4	1317	1288	1291											
RE11	F	00001C54	4	1364	1335	1338											
RE12	F	00001D4C	4	1411	1382	1385											
RE13	F	00001E44	4	1458	1429	1432											
RE14	F	00001F3C	4	1507	1478	1481											
RE15	F	00002034	4	1554	1525	1528											
RE16	F	0000212C	4	1601	1572	1575											
RE17	F	00002224	4	1648	1619	1622											
RE18	F	0000231C	4	1695	1666	1669											
RE19	F	00002414	4	1742	1713	1716											
RE2	F	0000139C	4	941	912	915											
RE20	F	0000250C	4	1789	1760	1763											
RE21	F	00002604	4	1836	1807	1810											
RE22	F	000026FC	4	1883	1854	1857											
RE23	F	000027F4	4	1930	1901	1904											
RE24	F	000028EC	4	1980	1951	1954											
RE25	F	000029E4	4	2027	1998	2001											
RE26	F	00002ADC	4	2074	2045	2048											
RE27	F	00002BD4	4	2121	2092	2095											
RE28	F	00002CCC	4	2168	2139	2142											
RE3	F	00001494	4	988	959	962											
RE4	F	0000158C	4	1035	1006	1009											
RE5	F	00001684	4	1082	1053	1056											
RE6	F	0000177C	4	1129	1100	1103											
RE7	F	00001874	4	1176	1147	1150											
RE8	F	0000196C	4	1223	1194	1197											
RE9	F	00001A64	4	1270	1241	1244											
READDR	A	0000001C	4	717	262												
REG2LOW	U	000000DD	1	596													
REG2PATT	U	AABBCCDD	1	595													
RELEN	A	00000018	4	716													
RPTDWSAV	D	00000628	8	513	502	504											

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
RPTERROR	I	00000602	4	497	350	396	432	469
RPTSAVE	F	00000620	4	510	497	507		
RPTSVR5	F	00000624	4	511	498	506		
SKIPXC	C	00000050	8	723	275	283	288	
SKL0001	U	0000005F	1	198	214			
SKT0001	C	0000022A	26	195	198	215		
SVOLDPSW	U	00000140	0	132				
T1	A	000011E0	4	857	2183			
T10	A	00001A98	4	1280	2192			
T11	A	00001B90	4	1327	2193			
T12	A	00001C88	4	1374	2194			
T13	A	00001D80	4	1421	2195			
T14	A	00001E78	4	1470	2196			
T15	A	00001F70	4	1517	2197			
T16	A	00002068	4	1564	2198			
T17	A	00002160	4	1611	2199			
T18	A	00002258	4	1658	2200			
T19	A	00002350	4	1705	2201			
T2	A	000012D8	4	904	2184			
T20	A	00002448	4	1752	2202			
T21	A	00002540	4	1799	2203			
T22	A	00002638	4	1846	2204			
T23	A	00002730	4	1893	2205			
T24	A	00002828	4	1943	2206			
T25	A	00002920	4	1990	2207			
T26	A	00002A18	4	2037	2208			
T27	A	00002B10	4	2084	2209			
T28	A	00002C08	4	2131	2210			
T3	A	000013D0	4	951	2185			
T4	A	000014C8	4	998	2186			
T5	A	000015C0	4	1045	2187			
T6	A	000016B8	4	1092	2188			
T7	A	000017B0	4	1139	2189			
T8	A	000018A8	4	1186	2190			
T9	A	000019A0	4	1233	2191			
TESTING	F	00001004	4	607	234			
TNUM	H	00000004	2	707	233	325	372	408	445
TSUB	A	00000000	4	706	236			
TTABLE	F	00002D04	4	2182				
V0	U	00000000	1	2264				
V1	U	00000001	1	2265				
V10	U	0000000A	1	2274				
V11	U	0000000B	1	2275				
V12	U	0000000C	1	2276				
V13	U	0000000D	1	2277				
V14	U	0000000E	1	2278				
V15	U	0000000F	1	2279	297	299	304	306
V16	U	00000010	1	2280	296	297	303	304
V17	U	00000011	1	2281				
V18	U	00000012	1	2282				
V19	U	00000013	1	2283				
V1FUDGE	X	000011B0	16	697				
V1INPUT	X	000011C0	16	698				
V1O1	X	00001208	16	870	892			
V1O10	X	00001AC0	16	1293	1315			
V1O11	X	00001BB8	16	1340	1362			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V1O12	X	00001CB0	16	1387	1409												
V1O13	X	00001DA8	16	1434	1456												
V1O14	X	00001EA0	16	1483	1505												
V1O15	X	00001F98	16	1530	1552												
V1O16	X	00002090	16	1577	1599												
V1O17	X	00002188	16	1624	1646												
V1O18	X	00002280	16	1671	1693												
V1O19	X	00002378	16	1718	1740												
V1O2	X	00001300	16	917	939												
V1O20	X	00002470	16	1765	1787												
V1O21	X	00002568	16	1812	1834												
V1O22	X	00002660	16	1859	1881												
V1O23	X	00002758	16	1906	1928												
V1O24	X	00002850	16	1956	1978												
V1O25	X	00002948	16	2003	2025												
V1O26	X	00002A40	16	2050	2072												
V1O27	X	00002B38	16	2097	2119												
V1O28	X	00002C30	16	2144	2166												
V1O3	X	000013F8	16	964	986												
V1O4	X	000014F0	16	1011	1033												
V1O5	X	000015E8	16	1058	1080												
V1O6	X	000016E0	16	1105	1127												
V1O7	X	000017D8	16	1152	1174												
V1O8	X	000018D0	16	1199	1221												
V1O9	X	000019C8	16	1246	1268												
V1OUTPUT	X	00000028	16	719	263	296	303										
V2	U	00000002	1	2266													
V20	U	00000014	1	2284													
V21	U	00000015	1	2285													
V22	U	00000016	1	2286	889	890	892	936	937	939	983	984	986	1030	1031	1033	1077
					1078	1080	1124	1125	1127	1171	1172	1174	1218	1219	1221	1265	1266
					1268	1312	1313	1315	1359	1360	1362	1406	1407	1409	1453	1454	1456
					1502	1503	1505	1549	1550	1552	1596	1597	1599	1643	1644	1646	1690
					1691	1693	1737	1738	1740	1784	1785	1787	1831	1832	1834	1878	1879
					1881	1925	1926	1928	1975	1976	1978	2022	2023	2025	2069	2070	2072
					2116	2117	2119	2163	2164	2166							
V23	U	00000017	1	2287	889	890	936	937	983	984	1030	1031	1077	1078	1124	1125	1171
					1172	1218	1219	1265	1266	1312	1313	1359	1360	1406	1407	1453	1454
					1502	1503	1549	1550	1596	1597	1643	1644	1690	1691	1737	1738	1784
					1785	1831	1832	1878	1879	1925	1926	1975	1976	2022	2023	2069	2070
					2116	2117	2163	2164									
V24	U	00000018	1	2288													
V25	U	00000019	1	2289													
V26	U	0000001A	1	2290													
V27	U	0000001B	1	2291													
V28	U	0000001C	1	2292													
V29	U	0000001D	1	2293													
V2ADDR	A	0000000C	4	714	314												
V2_1	A	000011EC	4	865	888												
V2_10	A	00001AA4	4	1288	1311												
V2_11	A	00001B9C	4	1335	1358												
V2_12	A	00001C94	4	1382	1405												
V2_13	A	00001D8C	4	1429	1452												
V2_14	A	00001E84	4	1478	1501												
V2_15	A	00001F7C	4	1525	1548												
V2_16	A	00002074	4	1572	1595												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V2_17	A	0000216C	4	1619	1642
V2_18	A	00002264	4	1666	1689
V2_19	A	0000235C	4	1713	1736
V2_2	A	000012E4	4	912	935
V2_20	A	00002454	4	1760	1783
V2_21	A	0000254C	4	1807	1830
V2_22	A	00002644	4	1854	1877
V2_23	A	0000273C	4	1901	1924
V2_24	A	00002834	4	1951	1974
V2_25	A	0000292C	4	1998	2021
V2_26	A	00002A24	4	2045	2068
V2_27	A	00002B1C	4	2092	2115
V2_28	A	00002C14	4	2139	2162
V2_3	A	000013DC	4	959	982
V2_4	A	000014D4	4	1006	1029
V2_5	A	000015CC	4	1053	1076
V2_6	A	000016C4	4	1100	1123
V2_7	A	000017BC	4	1147	1170
V2_8	A	000018B4	4	1194	1217
V2_9	A	000019AC	4	1241	1264
V3	U	00000003	1	2267	
V30	U	0000001E	1	2294	
V31	U	0000001F	1	2295	
V4	U	00000004	1	2268	
V5	U	00000005	1	2269	
V6	U	00000006	1	2270	
V7	U	00000007	1	2271	
V8	U	00000008	1	2272	
V9	U	00000009	1	2273	
VXC	X	0000000B	1	713	248 417
VXC1	X	000011EB	1	864	
VXC10	X	00001AA3	1	1287	
VXC11	X	00001B9B	1	1334	
VXC12	X	00001C93	1	1381	
VXC13	X	00001D8B	1	1428	
VXC14	X	00001E83	1	1477	
VXC15	X	00001F7B	1	1524	
VXC16	X	00002073	1	1571	
VXC17	X	0000216B	1	1618	
VXC18	X	00002263	1	1665	
VXC19	X	0000235B	1	1712	
VXC2	X	000012E3	1	911	
VXC20	X	00002453	1	1759	
VXC21	X	0000254B	1	1806	
VXC22	X	00002643	1	1853	
VXC23	X	0000273B	1	1900	
VXC24	X	00002833	1	1950	
VXC25	X	0000292B	1	1997	
VXC26	X	00002A23	1	2044	
VXC27	X	00002B1B	1	2091	
VXC28	X	00002C13	1	2138	
VXC3	X	000013DB	1	958	
VXC4	X	000014D3	1	1005	
VXC5	X	000015CB	1	1052	
VXC6	X	000016C3	1	1099	
VXC7	X	000017BB	1	1146	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
VXC8	X	000018B3	1	1193		
VXC9	X	000019AB	1	1240		
VXCMSG	U	00000502	1	404	250	
VXCPEXP	C	000010B5	3	640	421	
VXCPGOT	C	000010CA	3	643	428	
VXCPLINE	C	0000106B	13	635	645	431
VXCPLNG	U	00000063	1	645	430	
VXCPNAME	C	0000109C	8	638	414	
VXCPNUM	C	00001078	3	636	412	
WK1	F	00000098	4	731		
WK2	F	0000009C	4	732		
X0001	U	000002C0	1	204	192	205
X1	F	00001280	4	885	857	
X10	F	00001B38	4	1308	1280	
X11	F	00001C30	4	1355	1327	
X12	F	00001D28	4	1402	1374	
X13	F	00001E20	4	1449	1421	
X14	F	00001F18	4	1498	1470	
X15	F	00002010	4	1545	1517	
X16	F	00002108	4	1592	1564	
X17	F	00002200	4	1639	1611	
X18	F	000022F8	4	1686	1658	
X19	F	000023F0	4	1733	1705	
X2	F	00001378	4	932	904	
X20	F	000024E8	4	1780	1752	
X21	F	000025E0	4	1827	1799	
X22	F	000026D8	4	1874	1846	
X23	F	000027D0	4	1921	1893	
X24	F	000028C8	4	1971	1943	
X25	F	000029C0	4	2018	1990	
X26	F	00002AB8	4	2065	2037	
X27	F	00002BB0	4	2112	2084	
X28	F	00002CA8	4	2159	2131	
X3	F	00001470	4	979	951	
X4	F	00001568	4	1026	998	
X5	F	00001660	4	1073	1045	
X6	F	00001758	4	1120	1092	
X7	F	00001850	4	1167	1139	
X8	F	00001948	4	1214	1186	
X9	F	00001A40	4	1261	1233	
XC0001	U	000002E8	1	218	210	
XCFAILMSG	H	000003D6	2	321	316	
XCHECK	U	0000034E	1	274	239	
XCO1	X	00001240	16	876		
XCO10	X	00001AF8	16	1299		
XCO11	X	00001BF0	16	1346		
XCO12	X	00001CE8	16	1393		
XCO13	X	00001DE0	16	1440		
XCO14	X	00001ED8	16	1489		
XCO15	X	00001FD0	16	1536		
XCO16	X	000020C8	16	1583		
XCO17	X	000021C0	16	1630		
XCO18	X	000022B8	16	1677		
XCO19	X	000023B0	16	1724		
XCO2	X	00001338	16	923		
XCO20	X	000024A8	16	1771		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES					
XCO21	X	000025A0	16	1818						
XCO22	X	00002698	16	1865						
XCO23	X	00002790	16	1912						
XCO24	X	00002888	16	1962						
XCO25	X	00002980	16	2009						
XCO26	X	00002A78	16	2056						
XCO27	X	00002B70	16	2103						
XCO28	X	00002C68	16	2150						
XCO3	X	00001430	16	970						
XCO4	X	00001528	16	1017						
XCO5	X	00001620	16	1064						
XCO6	X	00001718	16	1111						
XCO7	X	00001810	16	1158						
XCO8	X	00001908	16	1205						
XCO9	X	00001A00	16	1252						
XCOUTPUT	X	00000060	16	725	299	306	315			
XCPLINE	C	00001116	13	672	681	349				
XCPLNG	U	0000004E	1	681	348					
XCPM4	C	00001156	2	677	338					
XCPM5	C	00001161	2	679	345					
XCPNAME	C	00001145	8	675	331					
XCPTNUM	C	00001123	3	673	329					
XCR15	F	00000488	8	361	347	351				
XCRESULT	X	00000458	16	358						
XCSKIP	C	00000007	1	709	276					
XCV1	X	00000468	16	359						
XCV2	X	00000478	16	360						
XCVCRNF	F	00000380	4	293	285					
ZVE6TST	J	00000000	11652	129	132	134	138	142	605	130
=A(E6TESTS)	A	0000074C	4	580	224					
=AL2(L'MSGMSG)	R	0000075A	2	584	525					
=CL1'S'	C	0000075C	1	585	276					
=CL8' '	C	00000738	8	577	283					
=CL8'SKIP XC '	C	00000730	8	576	275	288				
=CL8'VCRNF'	C	00000740	8	578	284					
=F'1'	F	00000754	4	582	322	353	369	405	442	475
=F'4'	F	00000748	4	579	209					
=H'0'	H	00000758	2	583	520					
=XL4'00000008'	X	00000750	4	581	258					

```
 MACRO   DEFN  REFERENCES

FCHECK     81    191
PTTABLE   813   2181
VRR_C     748    854    901    948    995   1042   1089   1136   1183   1230   1277   1324   1371   1418   1467   1514   1561   1608
               1655   1702   1749   1796   1843   1890   1940   1987   2034   2081   2128
```

```
   DESC     SYMBOL   SIZE     POS        ADDR

Entry: 0

Image      IMAGE    11652  0000-2D83  0000-2D83
  Region            11652  0000-2D83  0000-2D83
    CSECT  ZVE6TST  11652  0000-2D83  0000-2D83
```

```
   STMT                      FILE NAME
1     /devstor/sharedvfp/tests/zvector-e6-21-VCRNF.asm

** NO ERRORS FOUND **
```