J-K Flip-Flop

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12/5/2018

ECE 09.414 VLSI Design

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Outline

- J-K Flip-Flop Overview / Description
- Features / Problems
- Block Diagram
- Truth Table
- Master Slave Design
- Design Choices
- Logical Design
- Worst Case Design
- Logical Effort, Number of Stages, Delay
- Gate Sizes for Optimized Design
- Standard Cell Library & Layout Simulations
- Conclusion

Overview

JK Flip-Flop with Clear

- like the SR flip-flop, includes a "toggle" function when inputs are set to 1.
- Outputs only change with a clock pulse (Synchronous)

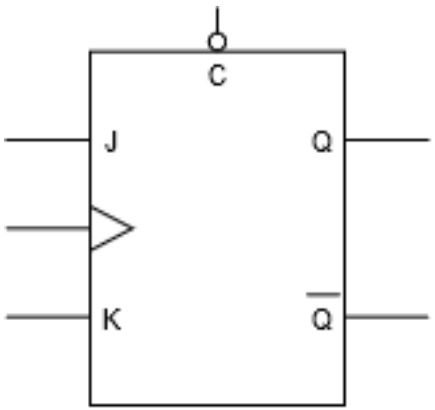
- J (set) and K (reset)
  - In other words:

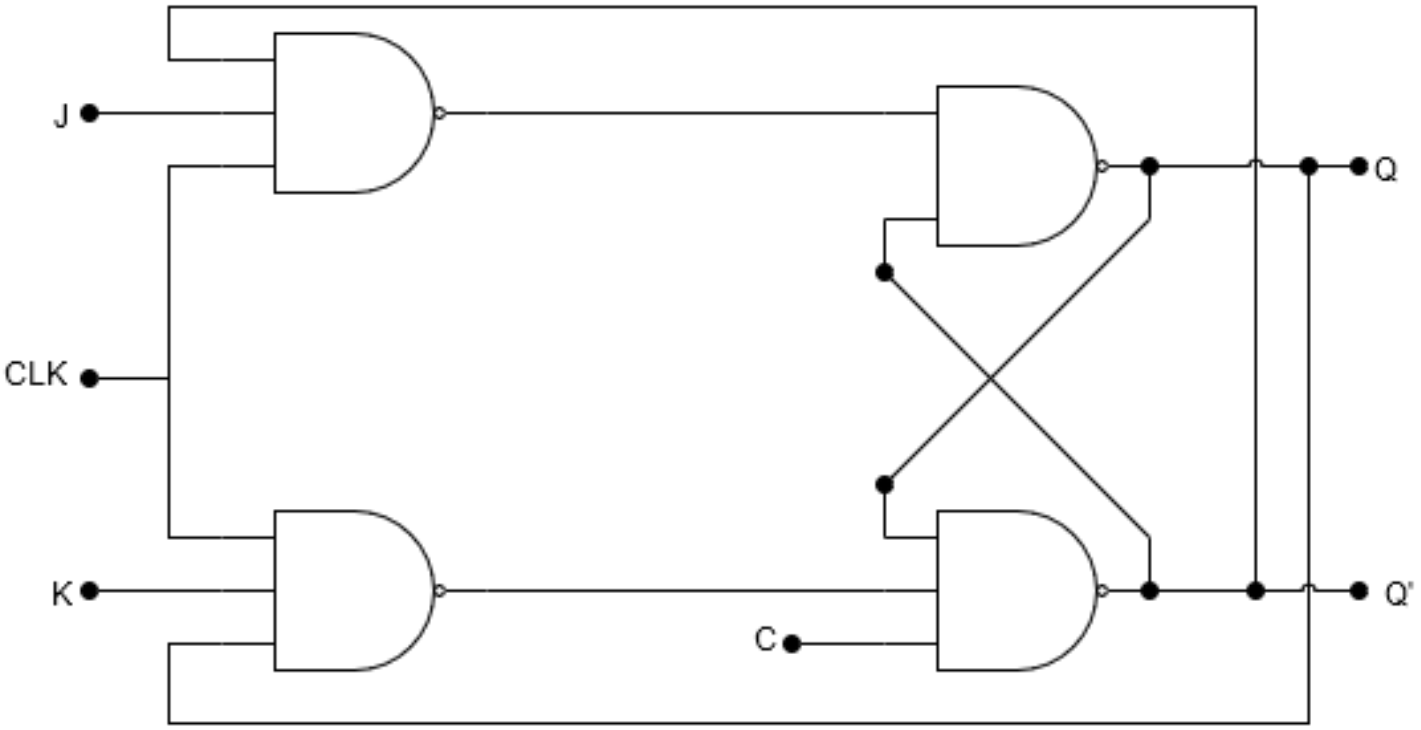
    J=1, K=0 sets the flip-flop

    J=0, K=1 resets the flip-flop

    J=1, K=1 toggles the flip-flop

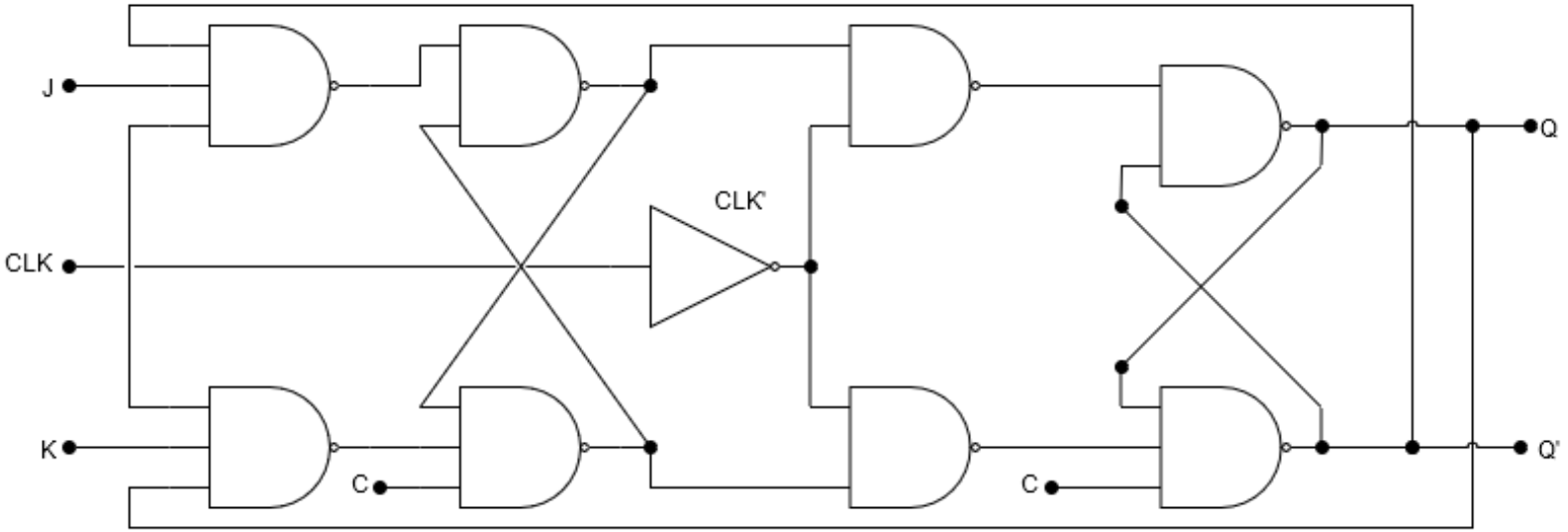
Block Diagram





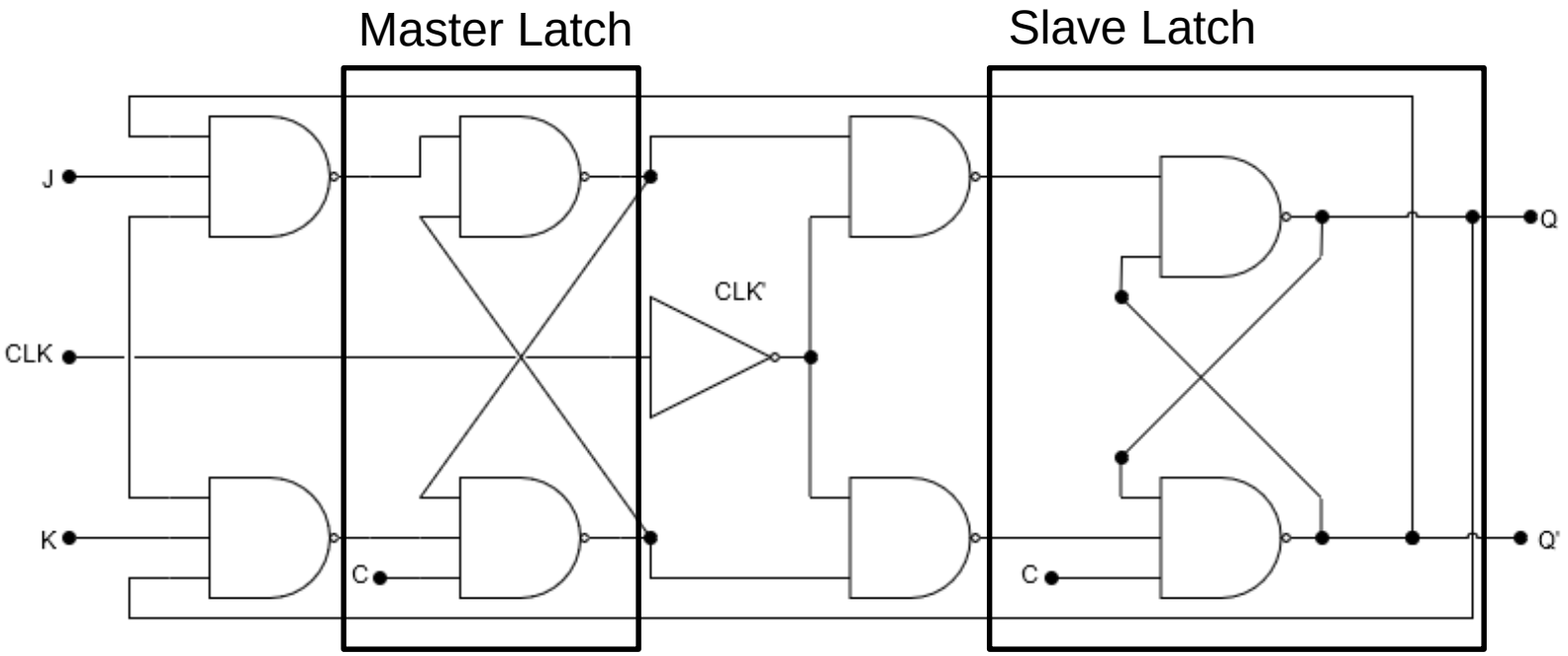
Input			Output		Description
J	K	C	Q	$\overline{Q}$	
0	0	0	0	0	Memory No change
0	0	0	0	1	
0	1	0	1	0	Reset Q >> 0
0	1	0	1	1	
1	0	0	0	0	Set Q >> 1
1	0	0	0	1	
1	1	0	1	0	Toggle
1	1	0	1	1	
x	x	1	0	1	Clear

Master/Slave Flip-Flop



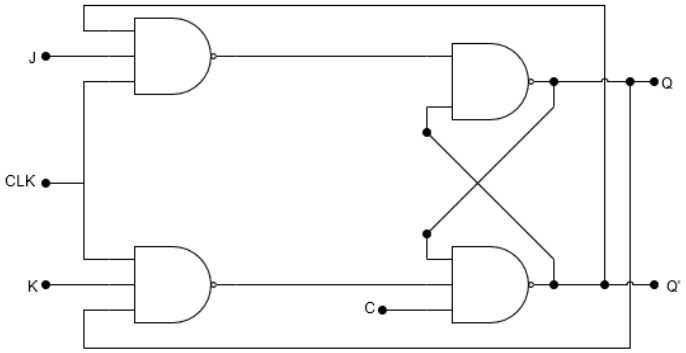
- Single flip-flops suffer from “race” timing problems
- Race timing occurs if the output *Q* changes state before the timing pulse of the clock input has time to go “OFF”.

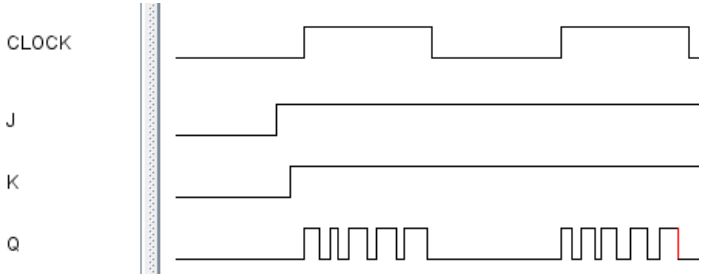
Master/Slave Flip-Flop



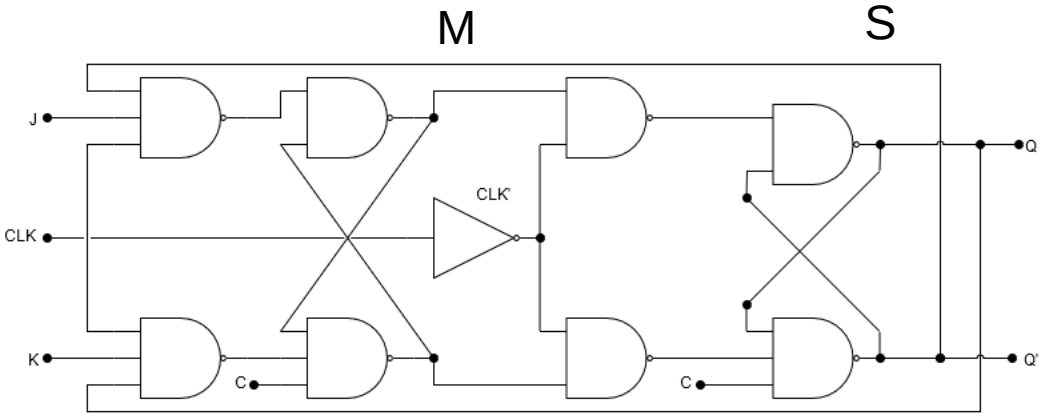
- Two latch stages in a cascaded configuration
- Activated with opposite clock phases
- Eliminates uncontrolled oscillations since only one stage is active at any given time

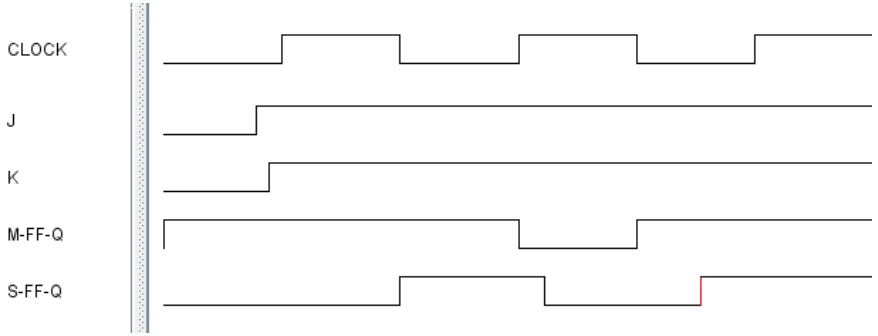
Master/Slave Flip-Flop





- Uncontrolled toggling when clock is high





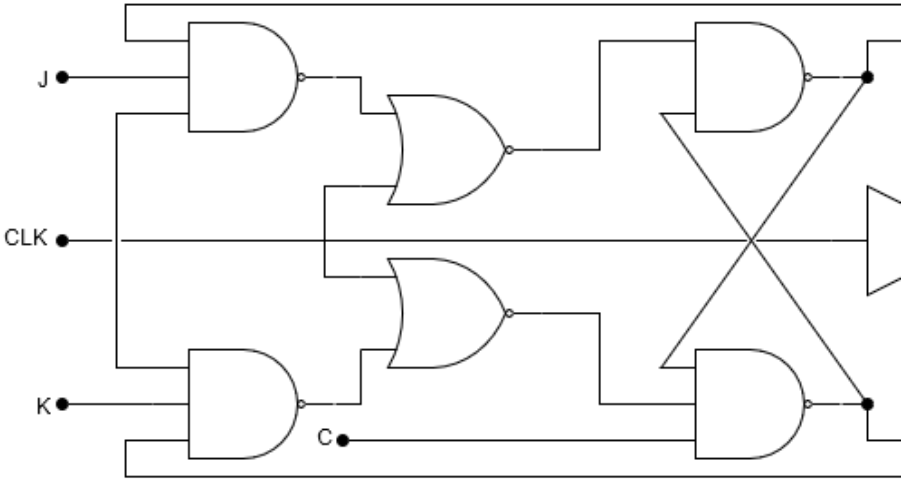
- Slave toggles half a clock cycle after the master latch

Design Overview

- POSSIBILITY 1: Simple NAND Logic Gate
  - PROS:
    - Simple design
    - Small design area
    - Easily understandable
  - CONS:
    - Some constraints on the clock pulse width
    - Minimized features
    - 32 Transistors Required

Design Overview

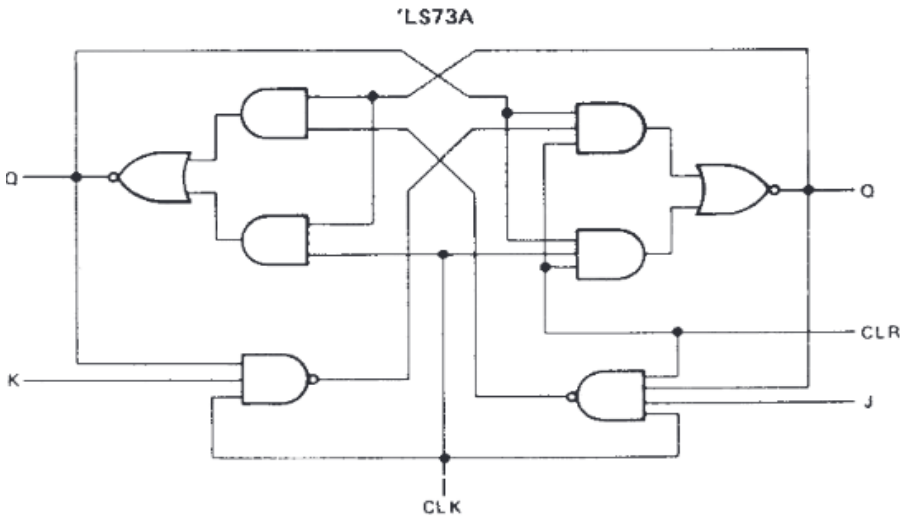
- POSSIBILITY 2.1: Edge Triggered NAND-NOR
  - PROS:
    - Edge-triggered
    - Easily understandable
  - CONS:
    - Inputs must be stable for some time before clock goes low.



    - Larger design area than NAND only (+2 NOR +2 NOT)
    - 44+ Transistors Required (Highest)
    - Timing is slower

Design Overview

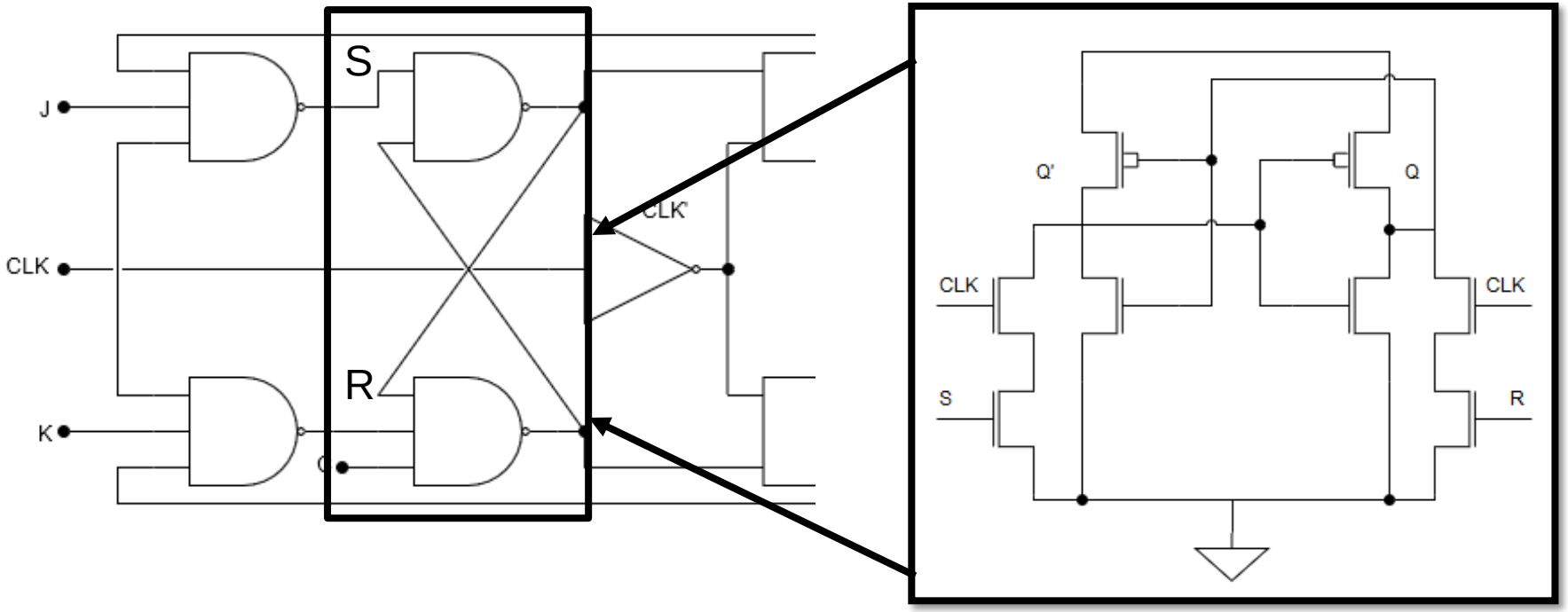
- POSSIBILITY 2.2: LS73A Based
  - PROS:
    - Edge-triggered
    - Professional Based
    - Fast Switching
  - CONS:
    - Inputs must be stable for some time before clock goes low.



- Larger design area than NAND only (+4 AND +8 NOT)
- Timing is slower
- Power consumption is higher

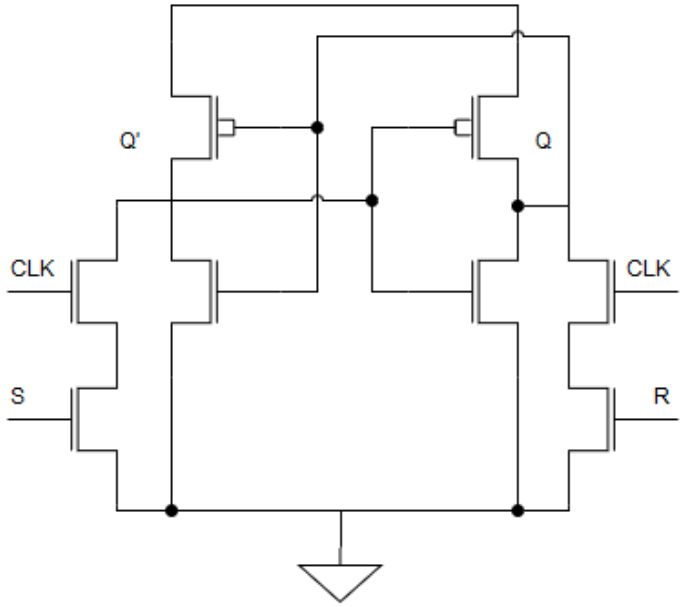
Design Overview

- POSSIBILITY 3: Pass Transistors

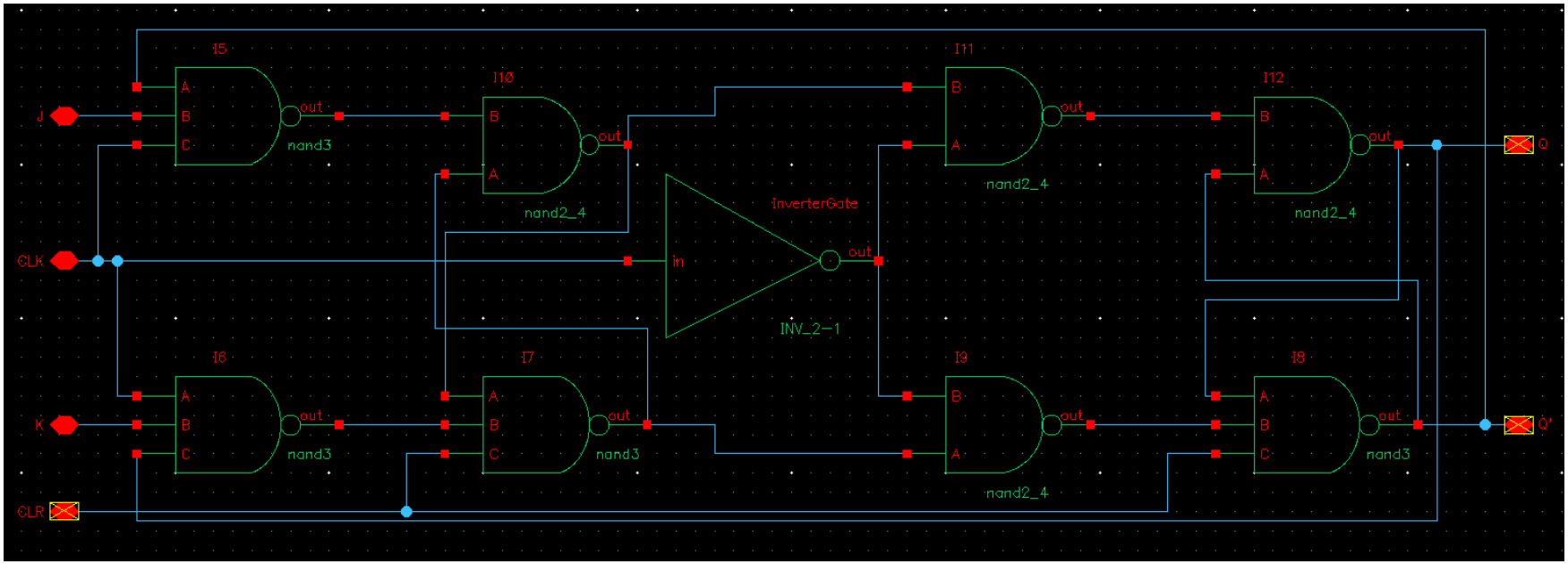


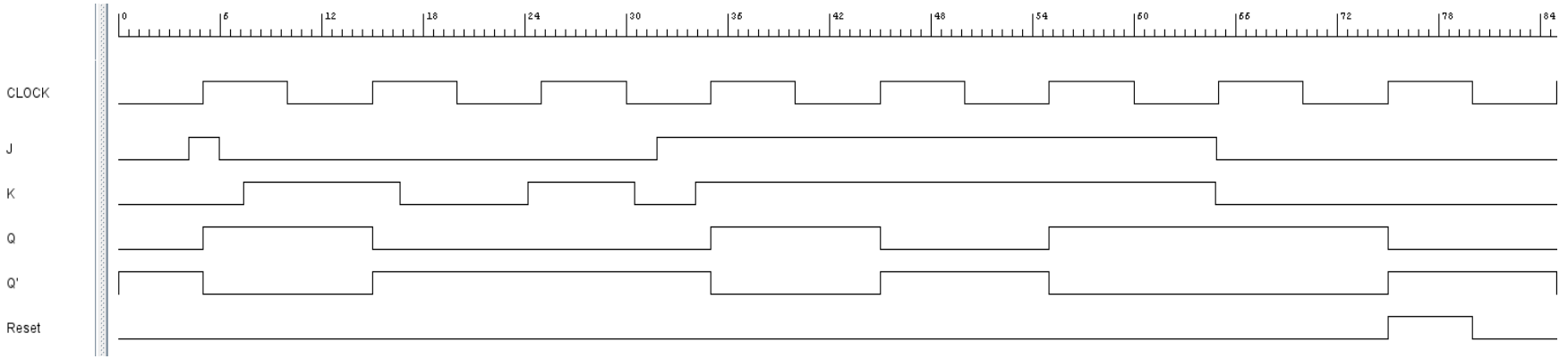
Design Overview

- POSSIBILITY 3: Pass Transistors
  - PROS
    - 18 Transistors
    - Smallest Logic Area
  - CONS
    - Additional components in latch area
    - Bad for pull-up level

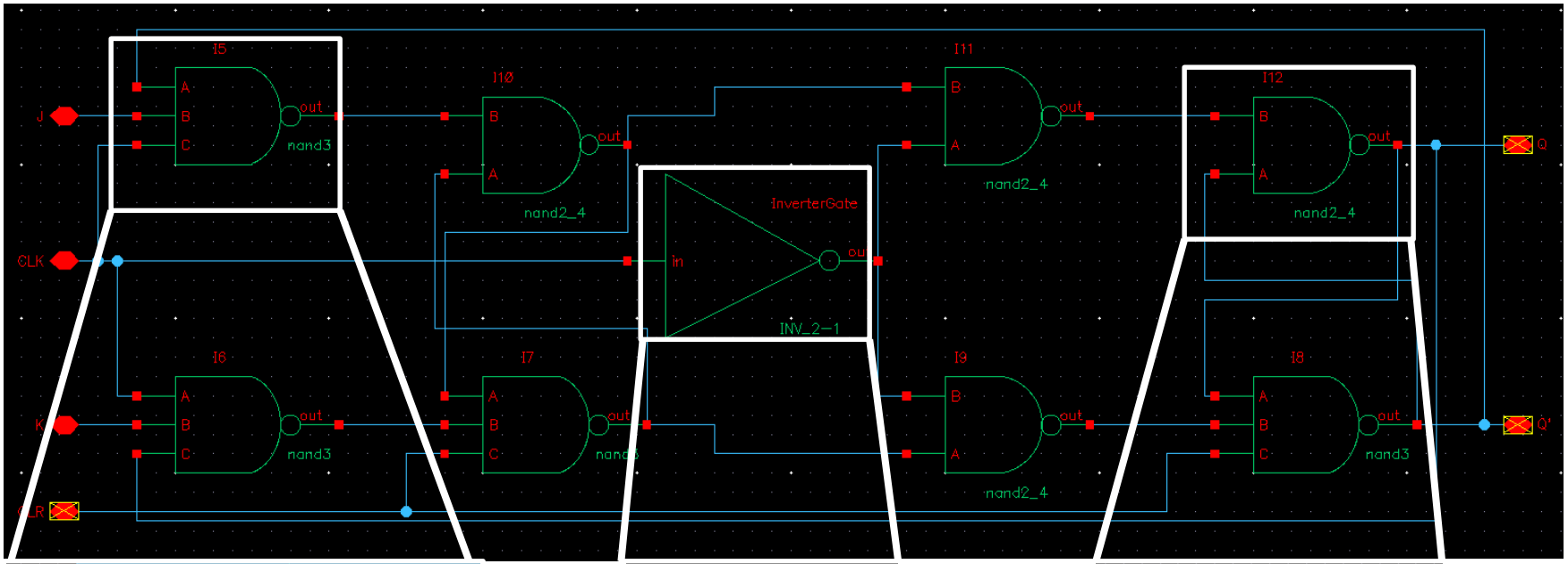


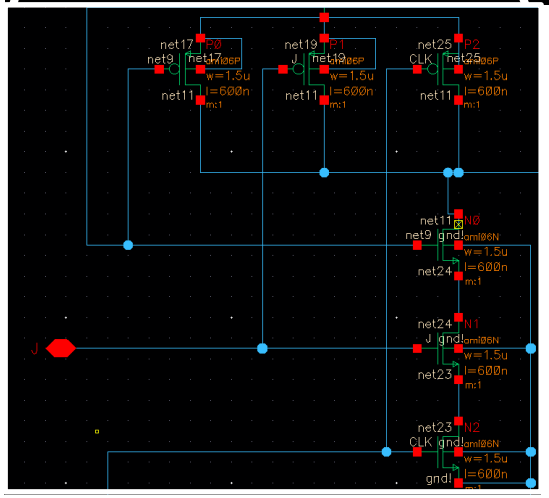
Logic Design

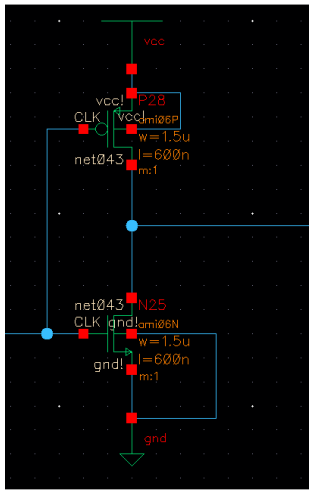


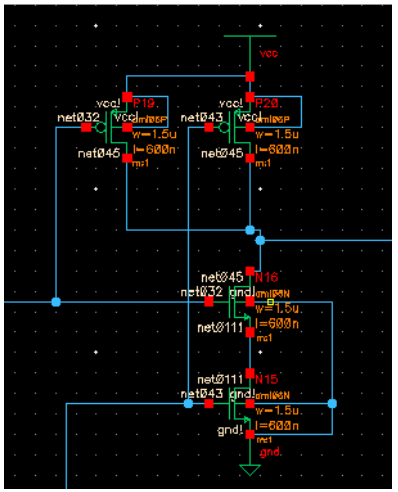


Transistor Design

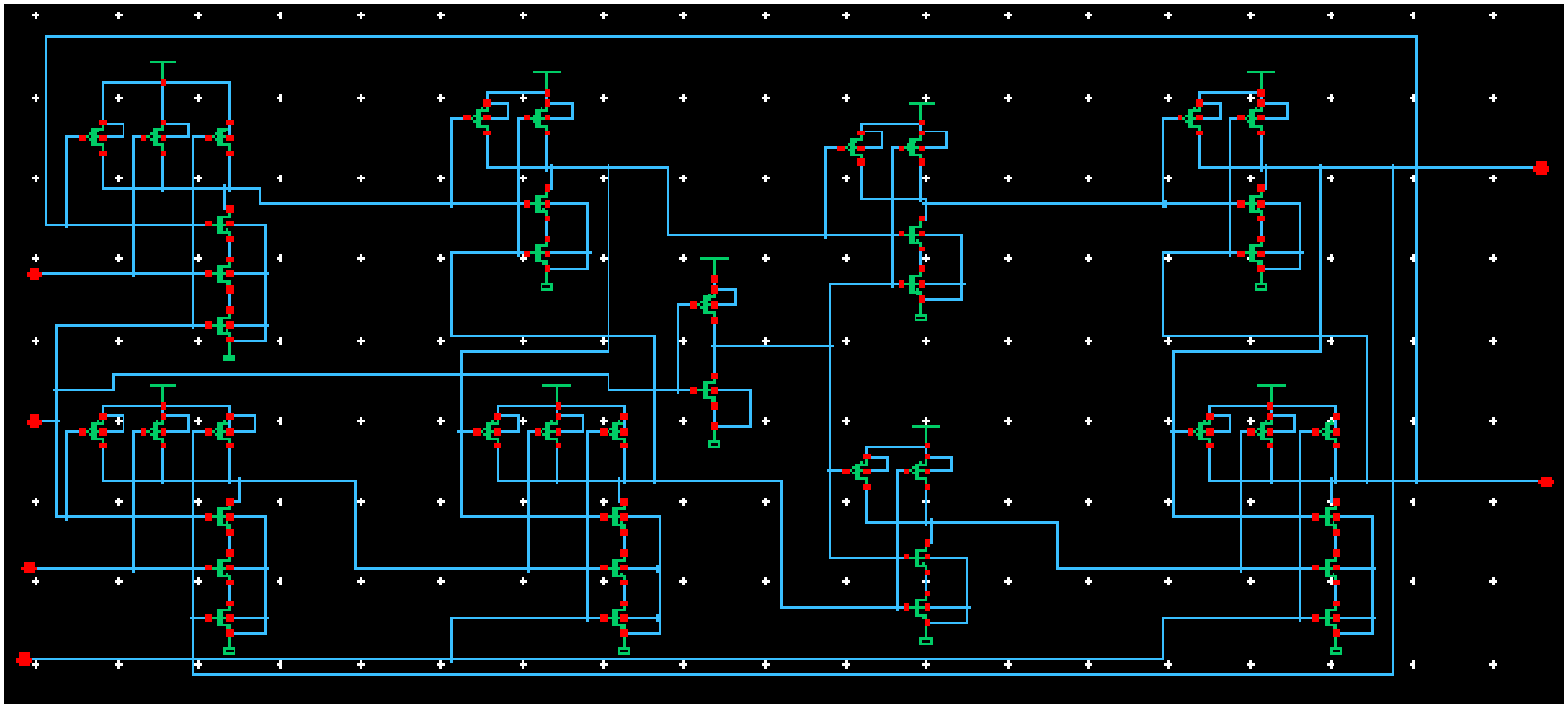




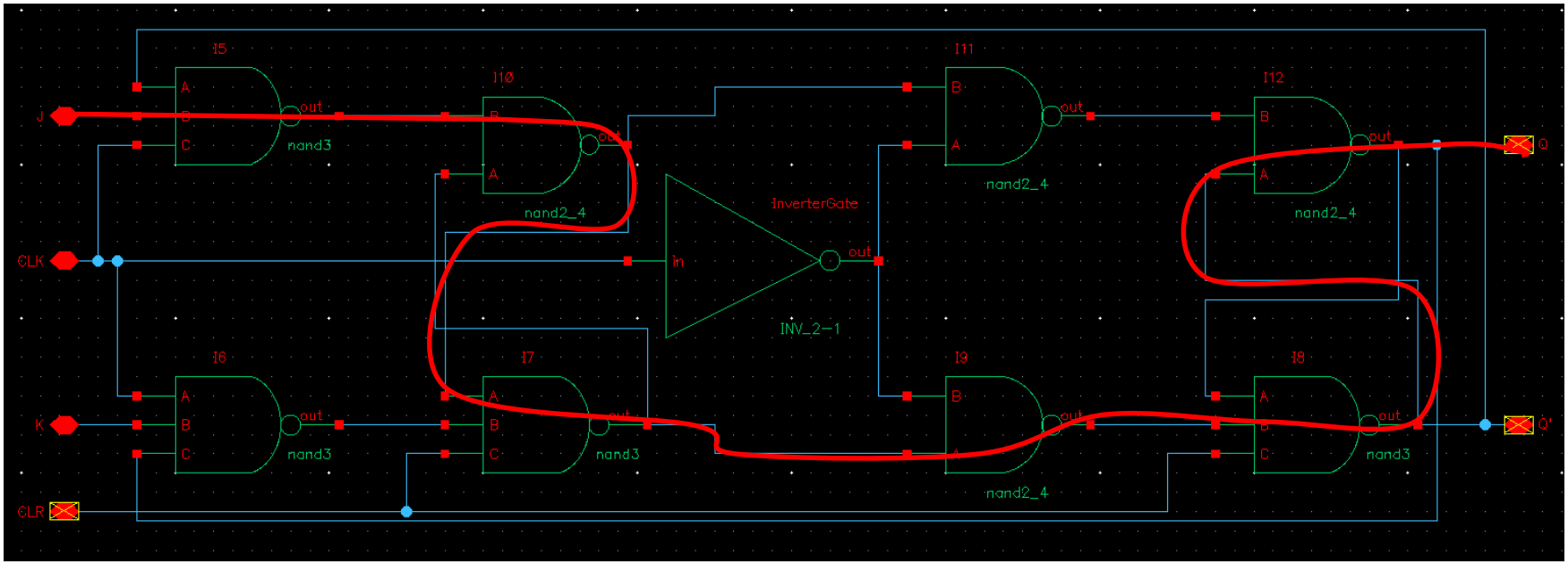




Transistor Design



Worst Case Logical Path



Logical Effort, Number of Stages, Delay

Variable	Stage				N = 4
	1	2	3	4	Path
b	1	2	1	3	B = 6
g	5/3	5/3	4/3	4/3	G = 400/81
h	0.364	0.364	0.455	0.455	H = 90/3 = 30
p	3	3	2	2	P = 10
$\hat{f} = \mathrm{F}^{\frac{1}{N}}$	5.46	5.46	5.46	5.46	F = GBH = 888.88

$$\mathrm{D} = N\hat{f} + P = 4 * 5.46 + 10 =$$

Spreadsheet Comparing Different Designs

Gate Sizes for Optimized Design

R	9.828
S	32.197
T	131.84
U	21.978

Standard Cell Library

Standard Cell Library Layouts

Standard Cell Library Extracted Layouts

Standard Cell Library Simulation “Spectre” Netlist

Standard Cell Library Simulation Input / Output Waveforms

Snap-together Standard Cells Circuit Layout

Snap-together Standard Cells Simulation Input / Output Waveform

Delay Comparison
Logical Effort vs. Spectre

Conclusions