ECE 09.414 VLSI Design
Fall 2018

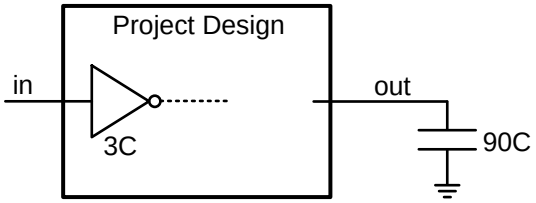
Course Project Description

The course project is an **individual** design project, so every student is responsible to analyze/design his/her circuit, write a full technical report, and present the project results to the class.

1. **Schedule & Important Dates**
   - Design period: 11/13 (Tue) ~ 12/8 (Sat)
   - **Presentation slides DUE**: **12/9 (Sun)**
   - **Oral Presentation**: During the **Lab/Lecture hours on 12/11 (Tue)** and **12/12 (Wed)**
   - **Written report DUE**: **12/17 (Mon)**

2. **Project Topic**: You will be given one project topic out of the following list:
   (a) Full adder
   (b) D Flip-Flop with Clear
   (c) J-K Flip-Flop with Clear
   (d) Parity Generator
   (e) 4-to-1 Multiplexer

3. **Input and Output Specification**
   (a) Take an inverter as the input gate to your design, and assume that the input inverter presents a load of 3 units of transistor width on its input.
   (b) And assume that the output load of your design is equivalent to 90 units of transistor width.



4. **Analysis and Preliminary Design**
   (a) For the chosen (or given) circuit, you may start from analyzing its Truth table.
   (b) Design *preliminary* logic, circuits, etc.
   (c) Then, using **Logical Efforts**, determine:
      - Number of stages to use for your design for **minimum delay**
      - How large each gate should be
      - How fast the circuit can operate
   (d) Optimize your design and finalize.

5. **Cadence Design**
   (a) Sketch a transistor-level schematic for the circuit showing transistor sizes
   (b) Layout your circuit using 0.6um poly-gate CMOS lambda-based design rules
   (c) Check layout design rules using DRC program
   (d) Verify LVS for your logic and circuit
   (e) Extract parasitic capacitances from Layout.
   (f) Determine circuit delay using Spectre and compare against your estimated value.

6. **Written Report**
   Although you are encouraged to collaborate during lab, each of you must individually prepare your own project presentation and written project report.
   - Your report should be organized, neat and legible.
   - Your report should be complete, thorough, understandable and literate.
   - You may use a concise summary style with clear discussions included where necessary.
   - You should include a well-drawn and labeled engineering schematic for each significant circuit investigated. Well-drawn free-hand sketches are permissible for schematics.
   - Space must be provided in the flow of your discussion for any tables or figures. Do not collect figures and drawings in a single appendix at the end of the report.
   - Experimental facts should always be given in the past tense.
   - Discussions or remarks about the presentation of data should mainly be in the present tense.
   - Discussions of results can be in both the present and past tenses, shifting back and forth from experimental facts to the presentation.
   - Any specific conclusions or deductions should be expressed in the past tense, general truths in the present tense.