Extraction and Layout Versus Schematic (LVS)

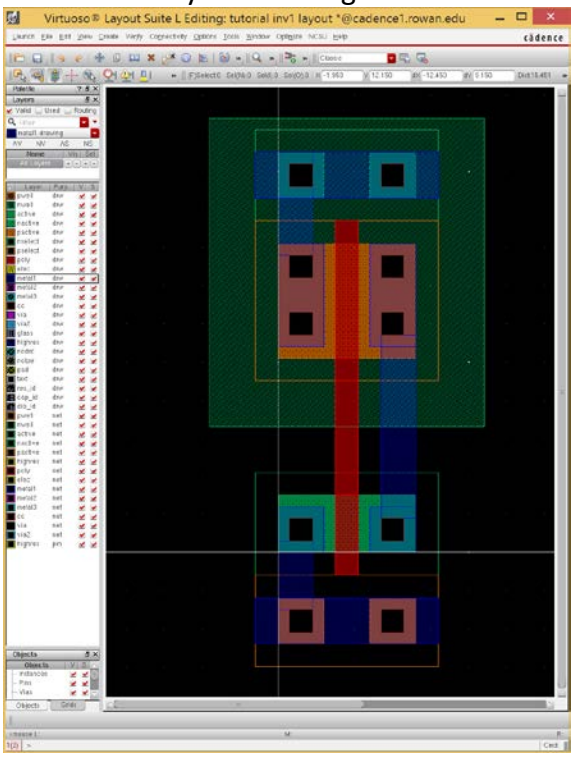
In this lab, we are going to practice with:

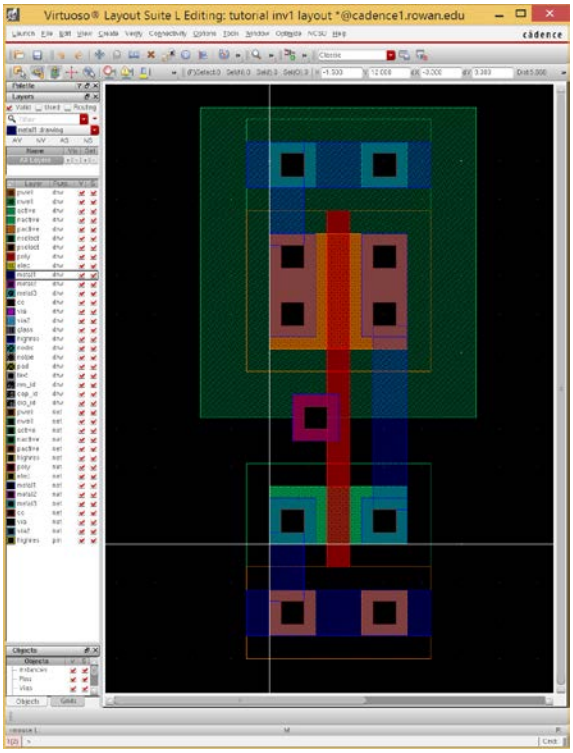
- Netlist extraction from the layout
- Netlist comparison: Layout vs. Schematic (LVS)
- Post-layout simulation with the extracted view

This tutorial is based on the inverter layout you designed for the last tutorials.

In order to proceed to extract netlist from the layout design, pins must be placed on the layout with the exactly same types and names as those in the schematic design. Then we'll use the DivaEXT to extract nets. The next verification step is to compare the extracted netlist against the netlist of the schematic design. It will be done with DivaLVS. Once you pass the LVS process, you should check the circuit functions again through simulations with the extracted netlist.

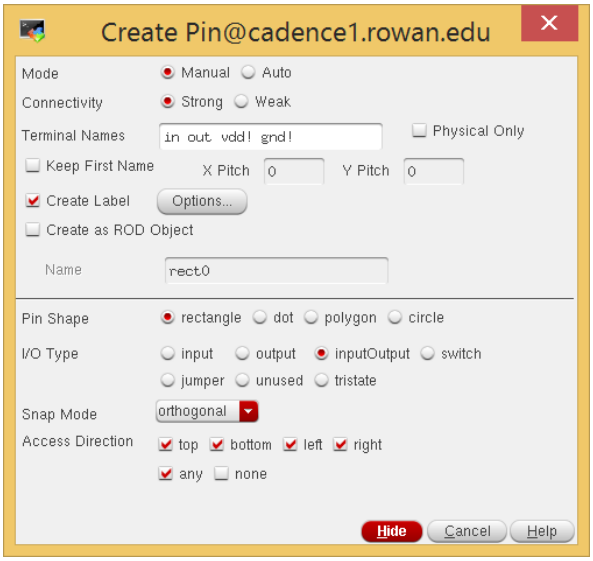
1) **Create PINs**:
   a. Starting from the **inverter layout** you've done during the last lab, you're to check if your layout exactly matches to its schematic. To do that you will firstly need to create electric PINs (in, out, vdd!, and gnd!) on the layout. You can use any physical layer for the PINs, however as a standard practice, we're going to use Metal-1 layer for all PINs.
   Open your inverter layout, and draw the poly contact surrounded by Metal-1 layer.
   Make sure all your drawings have no DRC error.



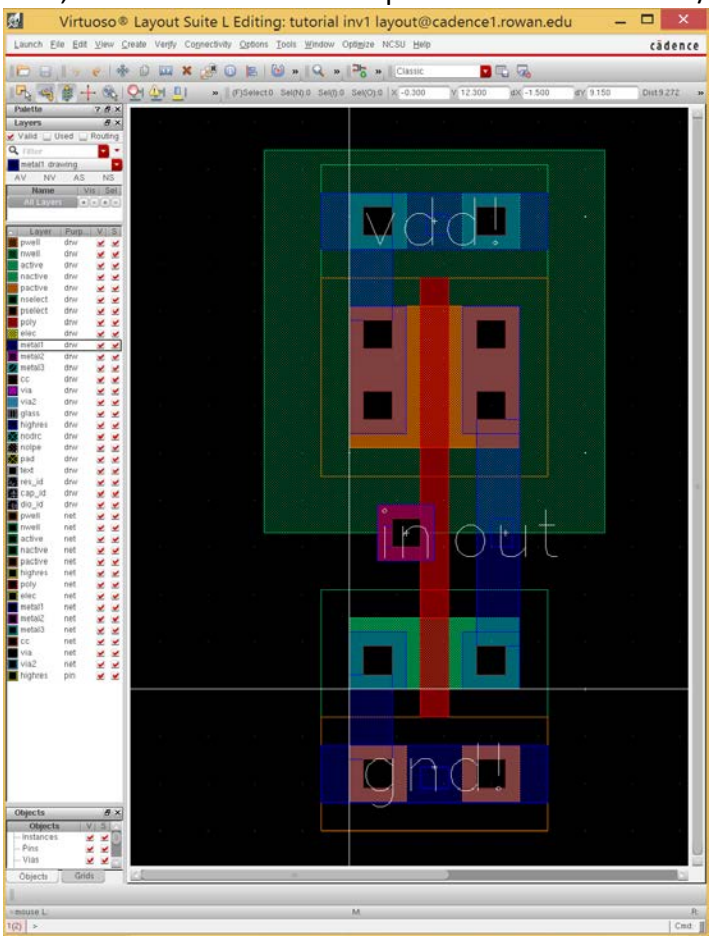


b. **<u>Add PINs</u>**: From the **LSW**, select **metal1** (drw) since we're to place PINs all with Metal-1 layer.

Then from the **Layout Editor**, choose *<u>Create -> Pin</u>* (or, its hotkey '**Ctrl+p**'). You should get a **Create Pin** window, where you can specify the pin names and properties. <u>Type the pin names</u> in the dialog box, <u>check for 'Create Label'</u>, and <u>choose I/O type</u> with the same type used in Schematic.



If click on 'hide' and get back to the Layout Editor, you're now ready to draw PINs and place their labels. Locate your mouse pointer to the position you want to place the pin, draw the pin in a rectangle, and click on the location you want to place the pin label on. You can do this one-by-one for all PINs, or do combine for multiple PINs with the same I/O type.



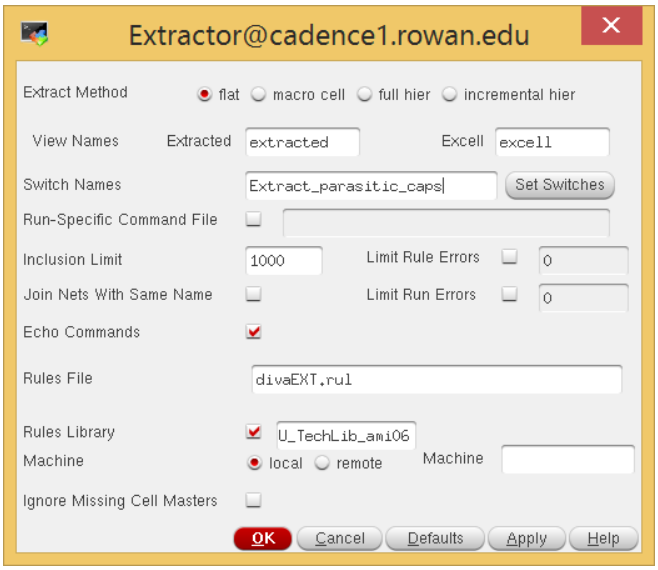
Don't forget to do DRC!!

2) **Create Extract View** from the layout:

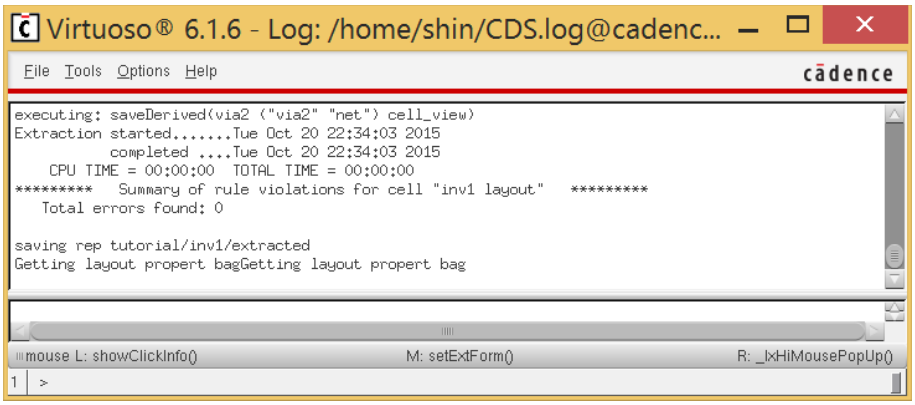
a. **<u>Netlist Extraction</u>**: The mask layout just contains coordinates of rectangles drawn in different layers. The extraction process identifies devices from the layout, and creates a netlist and other files that are necessary for the next steps of verifications and simulations.

From the **Layout Editor**, choose ***<u>Verify -> Extract</u>***. Then you should get a new window with extraction options. Click on **Set Switches** and select **Extract_parasitic_caps**. With the switch option, the extracted view will include parasitic capacitances extracted from the layout. Options set as the following will work fine.

To run Extract, click **OK**.

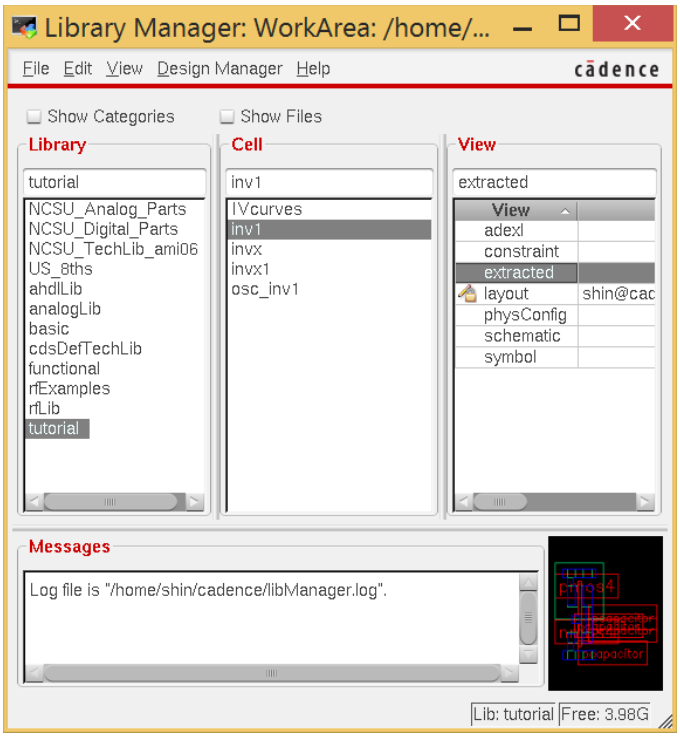


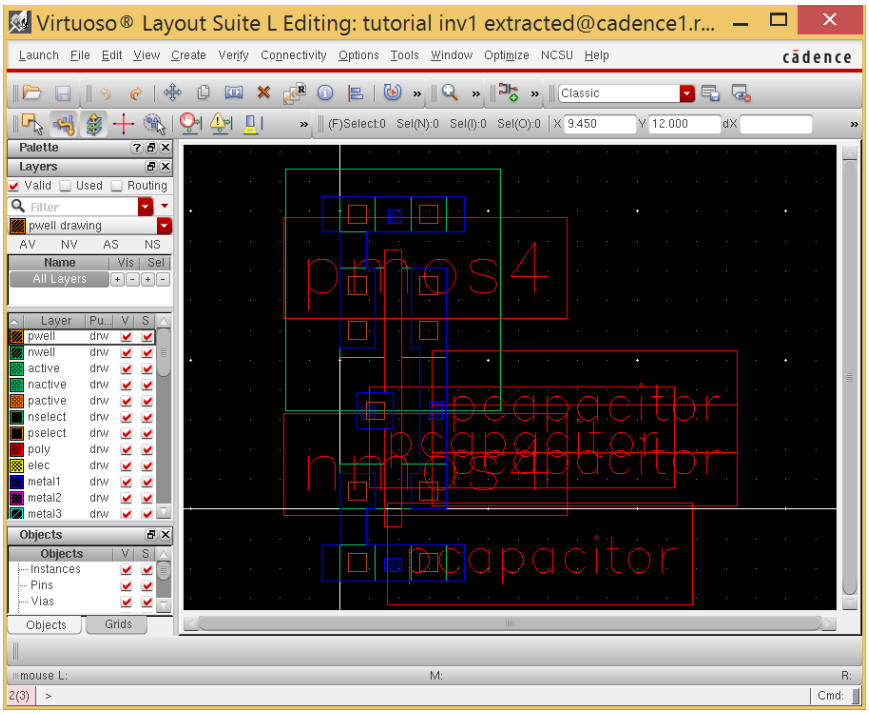
Check the **CIW** to make sure there is no error.



b. **<u>Check Extracted View</u>**: After successful completion of the extraction, new cell view, ***extracted*** view, of the ***inv1*** cell should be added to the **Library Manager**.

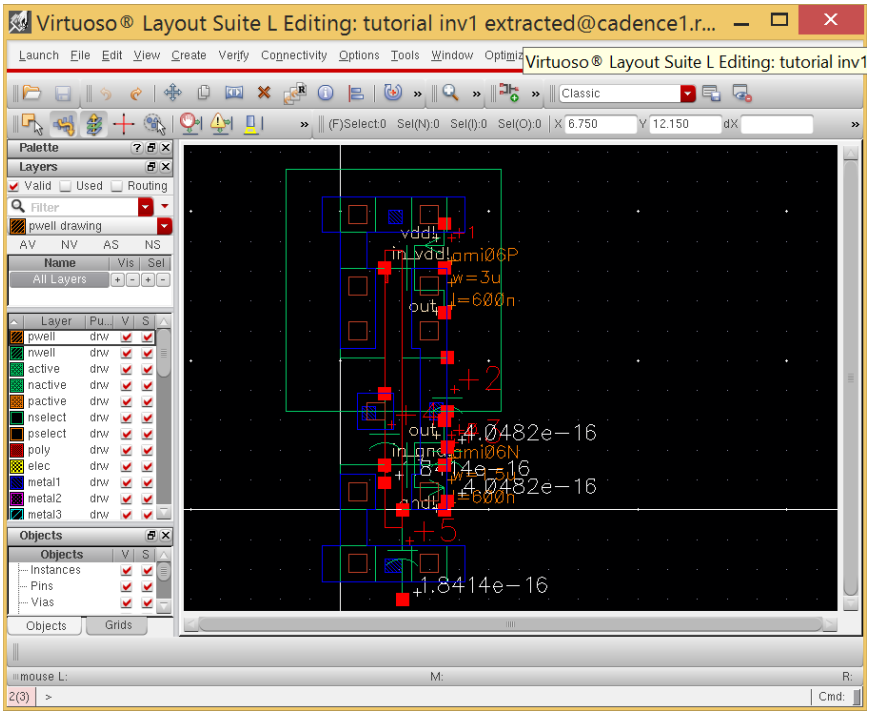
To open the extracted view, double click on the **extracted** view of the cell. This will open up a layout that looks almost identical to the layout view. You will notice that only the I/O pins appear as solid blocks and all other shapes appear as outlines. The red rectangles indicate that there are a number of instances (electrical elements) within this hierarchy.





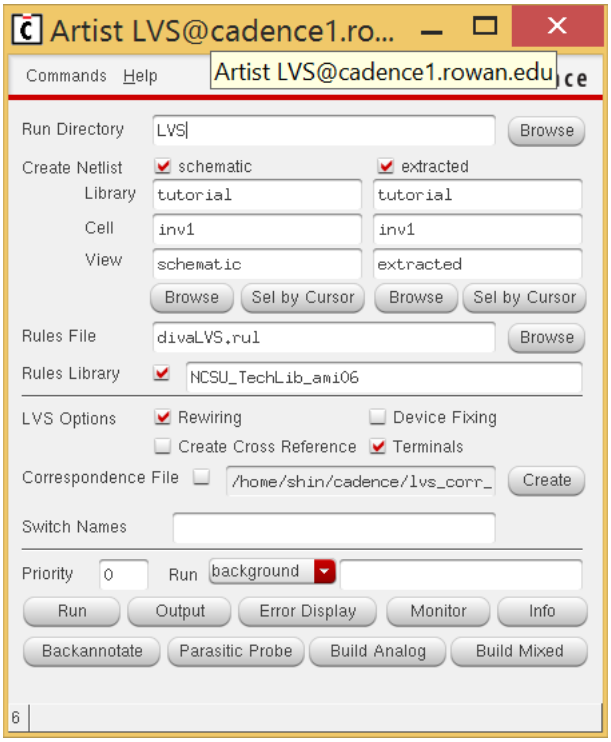
To see the complete hierarchy with details of extracted device symbols, type the hotkey '**Shift+F**'. You will see circuit elements you drawn in the layout, where the extracted device sizes should represent the values you drawn. In addition to the actual transistors you will notice a number of elements (mainly capacitors) in your extracted cell view.

These are not actual devices. They are parasitic capacitances, which are side effects formed by different layers you used for your layout. To disable this view, press '**Ctrl+F**'.



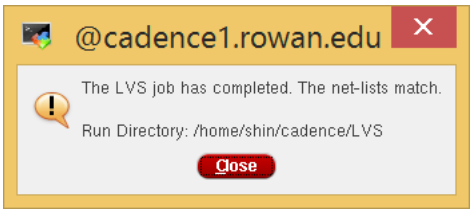
3) **Layout vs. Schematic (LVS)** Comparison:

a. The next step is to compare the netlist extracted from the layout with the schematic to ensure the layout you have drawn is an identical match to the schematic.
From the **Layout Editor**, select ***Verify -> LVS*** to open the LVS window. The top half of the LVS options window is split into two parts, schematic and extracted. Put the entries with the Library name, Cell name, and View, for each section.



b. Click on **Run** button to start the comparison.

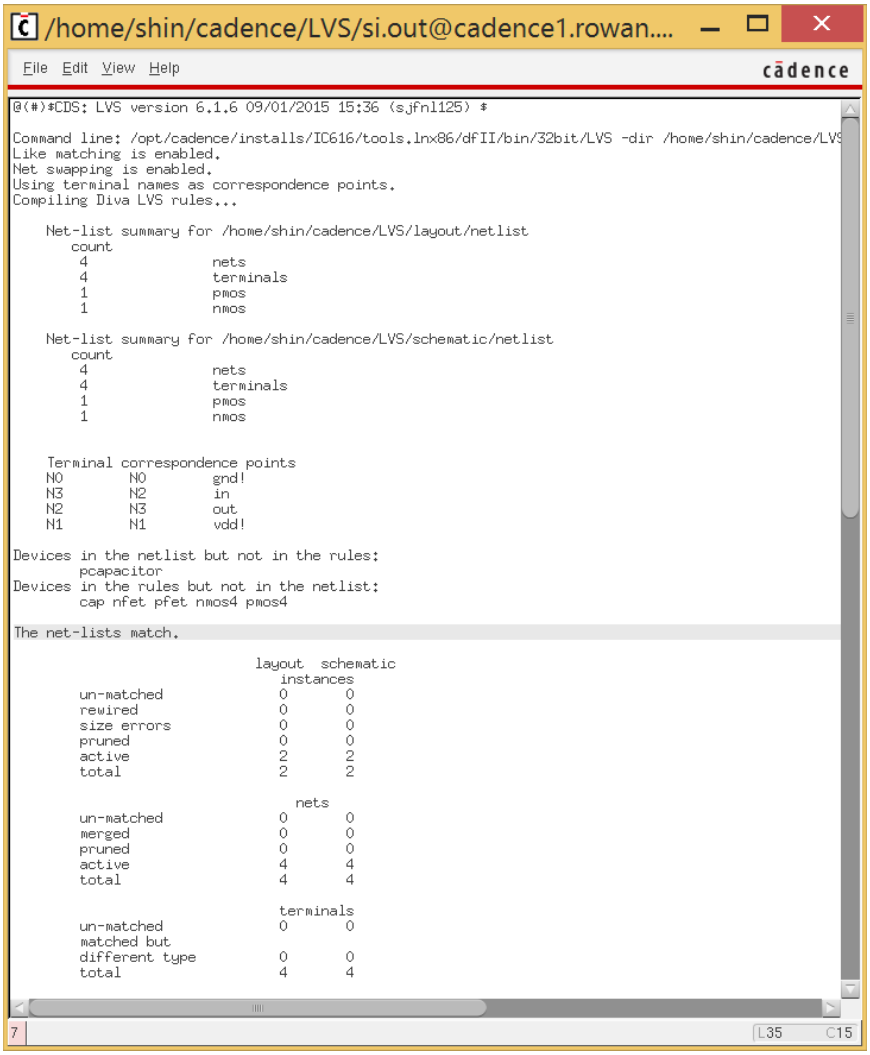
The comparison will be run in the background, and the results of the LVS will be displayed in a message box.



When the LVS comparison is complete you will get a pop up window saying “The LVS job . . .” Close the window.

From the **LVS** window, click on the **Output** button to display the LVS results. Scroll through this window and take a look at the LVS result.

The most important part of the report tells if errors were found or if netlists did match (“The net-lists match” as shown below). If no error, your layout is complete and correct. If there are errors, you will have to reload the layout view, fix the problems, and re-run DRC/Extract/LVS until there is no error.



4) **Post-Layout Simulation**:

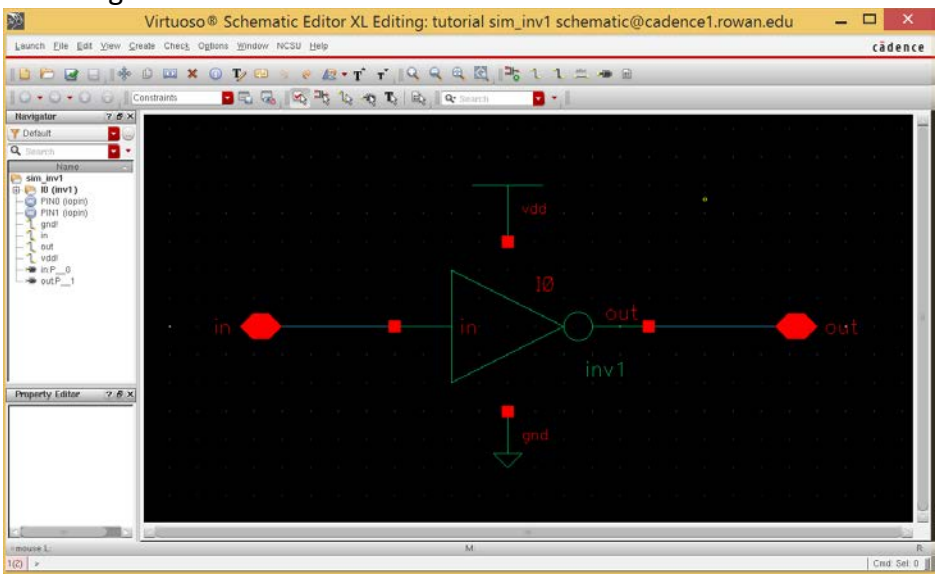
Having the extracted view of the inverter cell, now we can run simulations with the extracted netlists, so called post-layout simulation. This simulation will more accurately predict the behavior of the fabricated chip. In general the performance shifts caused by the layout parasitics can be substantial for large complicated chips, however, our inverter cell layout is very small in size so the parasitics would not lead significant shift.

To do the post-layout simulation, we're to create a new schematic cell view, and run the exactly same simulation we've done with the schematic view.

a. **Create a new *schematic* cell view**, ***sim_inv1***:

From the **Library Manager**, create new schematic cell view and give it a name **sim_inv1**.

In the **Schematic Editor** window, draw the schematic with an **inv1 symbol** as the following:

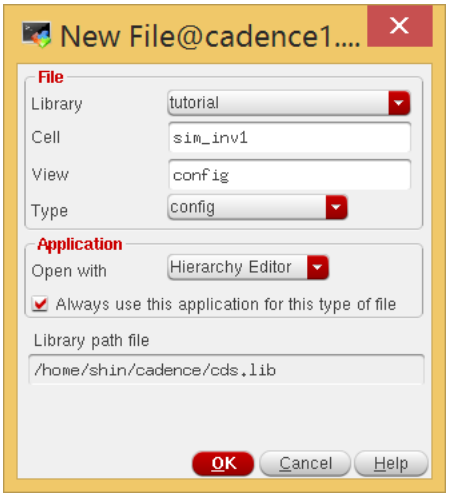


After editing, do **Check and Save**!

b. **Create a new *config* cell view** for ***sim_inv1***:

We are now to create a **config** view that will enable us to select/change between the schematic view and the extracted view.

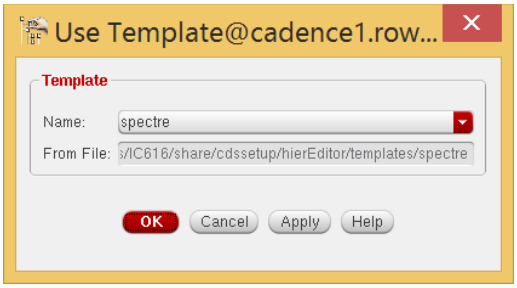
In order to create the **config** view, choose *File->New->Cell View* from the **Library Manager**. Select **config** for the *Type* and choose **Hierarchy Editor** for the *Open with* drop-down menu. Then click **OK**.



Now you should get an empty **New Configuration** window.

In the **Top Cell** section, fill the blanks with the cell view information, e.g., Library=tutorial, Cell=sim_inv1, View=schematic.

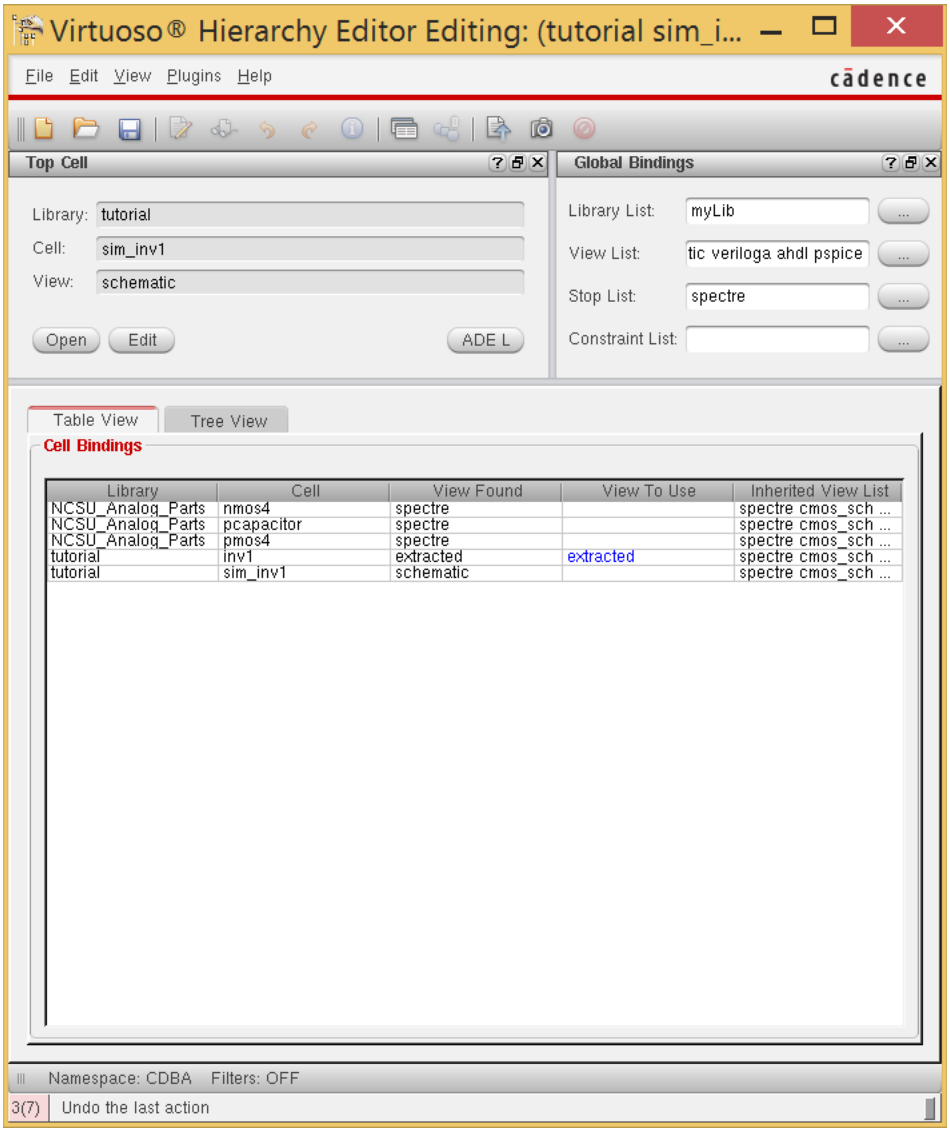
To load default settings for the **Global Bindings** section, click on the **Use Template** buton at the bottom of the window, then choose **spectre** from the *Name* list. Click **OK**.



Then the **New Configuration** window comes with settings for Global Bindings section.

Click OK, then you should get a new **Hierarchy Editor** where we can choose a view for the listed cell bindings. Since we're to run post-layout simulation with extracted view of inv1 cell, we'll choose extracted view for the inv1. To do that, **right click** on the **inv1** line and under the **Set Cell View** option select **extracted**. Then the Hierarchy Editor window should look like this:

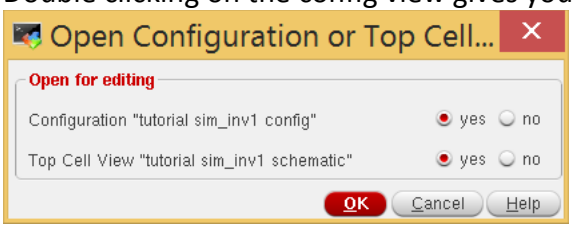
Save the setting! Now you can close this window.



c. **<u>Run post-layout simulation</u>**:

To run the simulation with the extracted view, it is important that you start from the **config** view you just created. If you start your simulation from the schematic view, you will only be simulating on the schematic, not the extracted view.

Double clicking on the config view gives you this window:



Clicking OK will get you with two windows, one for the configuration editor and the other one is the schematic view. If you don't want to open the configuration editor, you can select no for the upper checkbok.

From the schematic editor window brought up, you can do launch ADE GXL. Then in the ADE Test Editor, you can load the simulation setting saved for the inverter simulation. (Tip: Choose **spectre** for the simulator first, and then load the saved setting.) Double check all the settings you used before were loaded correctly. Running the simulation here is the post-layout simulation which reflects the effects of your layout, accounting parasitic resistances and capacitances.

Compare the post-layout simulation results (propagation delay) with those of inv1.

5) **Activity**

For the 2-input NAND gate you've drawn during the last lab, do the followings:

- Netlist extraction from the layout
- Successful LVS comparison
- Post-layout simulation (Use the input stimuli pattern we used for the inverter simulation only for one input, while applying constant 5V (or 0V) for the other input)
- Results comparison: pre-simulation vs. post-layout simulation