Lab 5: Extraction and Layout Versus Schematic

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***Abstract*—Integrated circuit (IC) layouts are susceptible to errors which can usually only be detected after a sample chip has been created. This report details the verification programs that identify the errors that delay or corrupt IC layouts at a point earlier in the design cycle of a given chip. These programs compare layout against schematic (LVS) design and extract a theoretical view of the bridge the gap between hypothetical circuit design and application to real layout designs. As such, regarding propagation delay, the developed layout designs produced a smaller propagation delay of a 0.147 % increase for the inverter design and a comparatively larger difference of 24.5% decrease of delay for the NAND design. Conclusively, the custom designed, layout-based schematic diagram, after passing appropriate checks, produced a more efficient output to the given circuit design by decreasing propagation delay.**

I. Introduction and Objectives

Comparison between layout and schematic design ensures that the layout design is functionally equivalent to the circuit design of the logic in question. In this lab, the extracted visual design and circuit netlist is compared. Using DivaEXT to extract netlists, the next verification step is to pass the Layout Versus Schematic (LVS) process and check the circuit functions through simulations with the extracted netlist.

II. Background and Relevant Theory

A. NOT Gate

Also known as an inverter, the NOT gate inverts the state of the input signal to the opposite state. The NOT gate is the most basic design for CMOS logic, displaying the NMOS and PMOS pairing characteristics. With an input (A) at ground value of 0, the inverter PMOS transistor in the NOT circuit pulls the source voltage of the output (Y) pin to high. With input at a high value of 1, the NMOS pulls down the output to 0. Physically, the NOT gate represents a CMOS logic ratio of 2:1 with the PMOS layout design being larger at the p+ diffusion layer.

B. NAND Gate

Transistors in NAND gate have equal size. This is illustrated in the width and length of the NMOS and PMOS of Figure 14. With a 2-input NAND gate, Here, the output is pulled low only when both of the inputs labelled A and B are both turned high. NAND circuits produce a $\frac{4}{3}$ logical effort to the design[1]. As such, the logical effort of the system proportially applies to the size of the system. Naturally, the delay in a NAND system is higher than the delay of a NOT circuit as due to the larger CMOS devices. This trend goes into a larger explanation in Section II-F.

C. CMOS Layout Architecture

CMOS architecture and layout design can be constructed using the layers of conductive and insulating composition. The layers used in this design for all models are listed in Table I along with the purpose of each layer. Understanding the overview of layout components allow for the layout designs of the NAND and NOT circuit to develop trends in delay reduction at the component level.

Layer	Description
n-well	creation formed on a bare p-type silicon wafer to lay the base for NMOS transistor design
n+ diffusion	lays ground for the transistor active area of negative diffusion
p+ diffusion	lays ground for the transistor active area of negative diffusion
polysilicon	establishes connection between NMOS and PMOS through a polysilicon layer
metal	used to connect metal contact between transistors and to output, VDD, and ground pins
contact	position to distinguish connections for CMOS and provide a contact for metal layers

TABLE I: Descriptions of layout design layers

D. Layout Extraction

Circuit extraction is the configuration of an integrated circuit layout translated into an electrical circuit of intended similar design[1]. The extracted circuit is required for circuit simulation, optimization, and logic to layout comparison.

E. Design Rules

The custom integrated chip (IC) layout for the CMOS logic design represents the layered masks used to fabricate a single component of a silicon wafer. The main objectives of the layout design are to build circuits in a reliably compact area. Design rules are defined regarding layer separations, feature sizes, and overlaps based in lambda-based design rules[1]. Lambda (λ) describes resolution of the design process as a unit. Total verification of a chip involves the design rule check (DRC) and layout versus schematic (LVS) along with a few other checks. For this experiment, each layout was run under both design checks to properly verify each design

for the NOT and NAND circuits. Design rules represent a compromise between chip performance and electrical yield with stronger rules producing greater opportunity for circuit improvements[1].

F. Delay

Delay within an inverter system can be measured to show the imperfections set by a transistor used in a design or the elements surrounding the transistor. For this report, delay characteristics of concern are the rise time, fall time, and propagation delay.

$$d = gh + p \tag{1}$$

Additionally, Equation 1 references the delay of the gate of a single logic gate along with the components attached to it. This equation, with g being the logical effort, h being the electrical effort, and p being the parasitic delay, measures the total delay of a certain CMOS logic system. Simply, the equation provides a trend to improve the delay of a system's performance based on gate type.

G. Rise & Fall Time

Rise time and fall time is the time between 20% and the 80% of the total transfer curve values. Specifically, rise time is the difference of time between the 20% of the total value to 80% of the total value. In this example, Equation2 and Equation 3 refers to these properties measured on the input and output signal[1].

$$t_f = |t_{VDD@80\%} - t_{VDD@20\%}| \tag{2}$$

$$t_r = |t_{VDD@20\%} - t_{VDD@80\%}| \tag{3}$$

H. Propagation Delay

Propagation delay refers to the maximum time from the input crossing signal at 50% to the output crossing signal at 50%. The average of the values at the rise and fall of the input and output signal is the propagation delay (t_{pd}) represented by Equation 4[1].

$$\frac{t_{pdf} + t_{pdr}}{2} \tag{4}$$

Propagation delay is the greater obstacle in the area of IC development and can effectively bottleneck systems. Reducing propagation delay decreases the length of time for the input to become reactive and stable to change.

III. Procedure

Cadence Layout Design software was used to develop the layout circuit design process and checking system. As a start, an inverter was created in the Cadence software. Layout designs used ran through a DRC check and the LVS check against a previously designed circuit, matching netlists. The layout was extracted and generated on a separate symbol schematic in order to compare the inverter layout against the pre-simulated circuit design built into cadence. This process was repeated for a NAND logic circuit. Delay relating to propagation, rise time, and fall time was measured at the appropriate junctures in order to compare the graphical simulations at each point.

IV. Results and Discussion

A. Inverter Layout

The custom inverter layout represents the CMOS masks used in wafers to fabricate a small part of the IC chips. The layout design provided in Figure 1 processes the layers detailed in Section II-C color-coded with an implemented input pin provided at the poly layer in the middle of the design.

Notably, Figure 1 includes the total size of the CMOS inverter design at 14.4λ by 7.2λ. This total schematic design plays a role in the delay and cost of the overall design as detailed in Section II-E & II-F. Improvements based on the framework of this design are explained in Section IV-E.

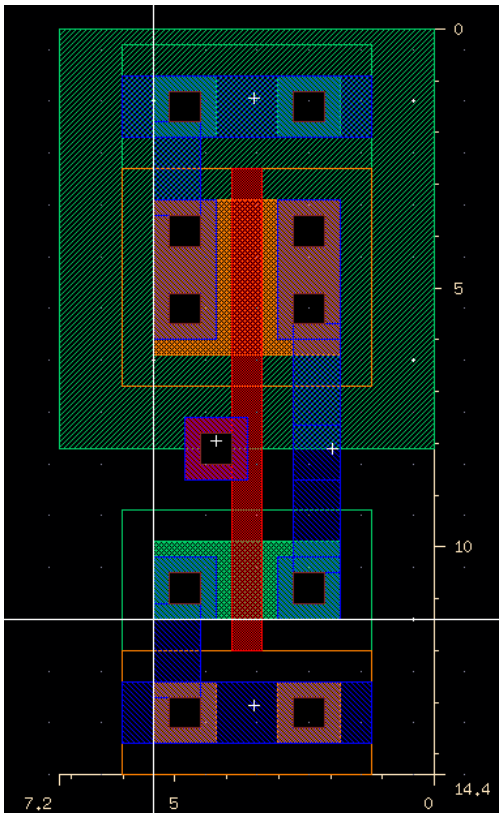

Fig. 1: Inverter layout for comparison between the inverter circuit Figure 12

Extracted views from the design of Figure 1 in Appendix Section VI-C This extracted circuit imposes the circuit simulation against the layout design for optimization to bring logic to layout comparison.

B. LVS Comparison

Successful LVS comparison displays a determination on whether the integrated circuit layout corresponds to the original schematic or circuit diagram of the design. Figure 2

displays the successful run of the inverter LVS design check of Figure 1 and Figure 12

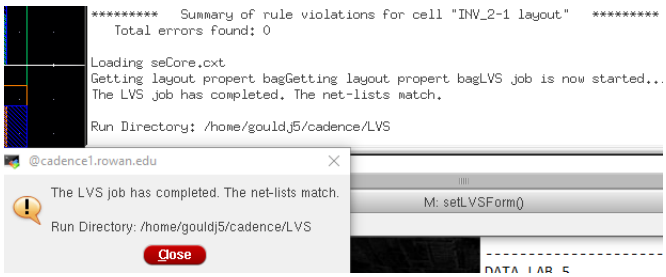

Fig. 2: LVS text output verification showing no errors with a matching net-list report.

A full LVS output as provided in Section VI-H.

C. Symbol Diagram

Symbol schematic designs as provided in Figure 3 allow for a compact representation of the extracted layout design to be easily simulated graphically to find rise, fall, and propagation delay times as well as any leakage provided at the output. As such, modelled by the in-out pins labeled appropriately "in" and "out" at the ends of the schematic of Figure 3 correspond to the vdd and gnd terminal pins at the top and bottom of the inverter layout of Figure 1.

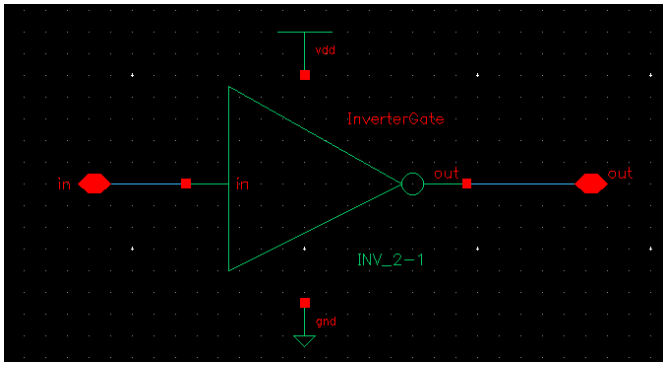

Fig. 3: Inverter simulation symbol diagram for set of extracted view from Figure 1

Outputs of this design are provided in Section IV-D on Figure 4 where the input terminal is depicted in blue, and output red.

D. Post-Layout Simulation

Post-layout simulation used for the inverter simulation with one input varying at a period of 2n where n is the variable representing the time-frame of the inverter schematic, while applying constant 5V (or 0V) for global maximum input.

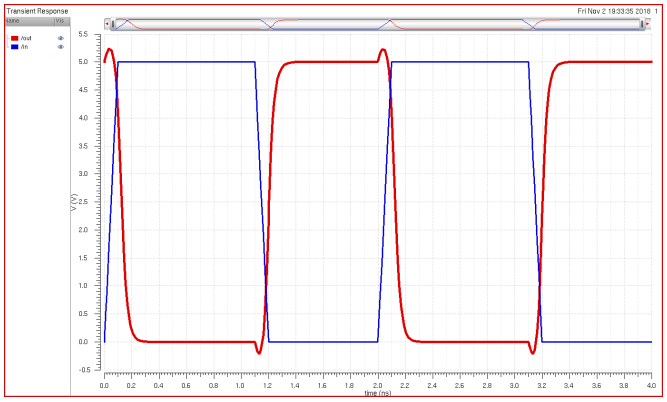

Fig. 4: Layout based simulation output used in Figure 3 with plotted values at the input and output of the layout design with a reference voltage input of 5 V.

Component	Delay	Value (ns)
Input	t_f	0.06
Input	t_r	0.06
Output	t_f	0.05386
Output	t_r	0.05117
In/Out	t_{pd}	0.064710

TABLE II: Inverter (NOT) Input to Output data involving rise, fall, and propagation delay for layout design transient simulation provided in Figure 4.

Post layout simulation details are provided at Figure 16 and with Section VI-G. Presently, each component of delay is measured using Equation 3, 2, and 4.

E. Result Comparison Between Inverter Simulations

Results of the pre-layout simulation from Lab 4 layout solutions and present the input to output graphical representations from the circuit provided in Figure 12.

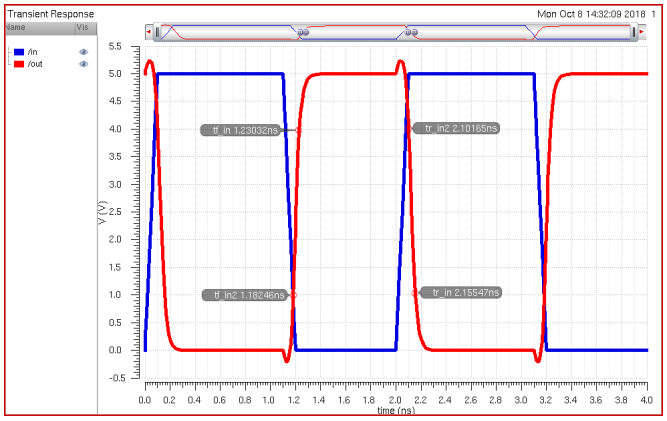

Fig. 5: Pre-layout inverter simulation output based on the theoretical circuit diagram.

Of notable design, the input of each circuit presented to be similar in that the input power to this layout and circuit are measured without any circuit modifications.

Component	Delay	Value (ns)
Input	t_f	0.06
Input	t_r	0.06
Output	t_f	0.05382
Output	t_r	0.04786
In/Out	t_{pd}	0.064805

TABLE III: Inverter (NOT) Input to Output data involving rise, fall, and propagation delay for circuit-based delay values.

Component	Percent Difference (%)
t_f	0.0743 %
t_r	6.92 %
t_{pd}	0.147 %

TABLE IV: Comparison of values between Figure 4 and 5 displaying the percent error between each output value provided by the Tables of III and II.

Of interest to delay prospects, the inverter design output produced by the layout of Figure 1 should process a lower propagation delay where a shorter amount of time between input and output allows for a decreased system switch time and increased system stability. As such the absolute value of percent difference to the two systems show that the propagation delay of the layout design improved in performance allowing to make assumptions that the overall design of Figure 1 to be said to have improved the IC. However, it is of note that the rise time of the system increased for the layout design which notably delays the system from an 'off' to 'on' state. This design specification is applied to the PMOS device as the PMOS device pulls the inverter to Vdd. The system capacitance at the PMOS device should be decreased in order to improve this characteristic.

F. NAND Layout

Figure 6 includes the pinout label of the CMOS inverter design at a size of 18.9λ by 9.6λ. This total schematic design plays a role in the delay and cost of the overall design as detailed in Section II-E and II-F. Improvements based on the framework of this design are explained in Section IV-K.

Section VI-D displays with Figure 14 that the design NAND circuit elements followed a CMOS size-ratio of 2:2 along with the layout design provided below. This schematic is referenced with Figure 6 to meet LVS design requirements and cross-check the netlist elements on each work.

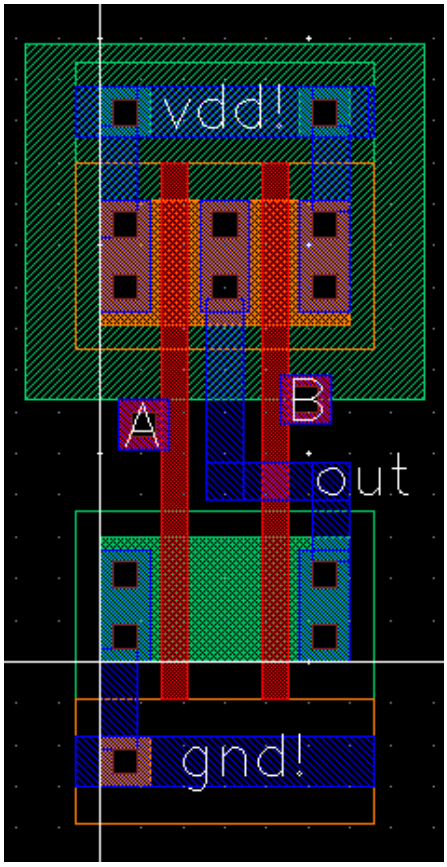

Fig. 6: Layout design for NAND circuit provided in Figure 14 with applied pins at Vdd, ground, output, and input pins at A and B

G. NAND DRC Results

```
DRC started.......Fri Oct 19 18:50:09 2018
    completed ....Fri Oct 19 18:50:09 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "nand2_4 layout"   *********
   Total errors found: 0

Found no matching marker(s) in view: "nand2_4".
```

Fig. 7: DRC results of NAND layout design displaying an output of no errors

Design rule checking of the electronic design determined that the physical layout matched the design rules. However, DRC does not promise an accurate representation of the circuit desired in fabrication. LVS check is used to guarantee this design representation for real-world implementation

H. LVS Comparison

Successful LVS comparison

```
Run Directory: /home/gouldj5/cadence/LVS

wire drawing -> net: "net13" bounding box: (0.69,0.12) (1.19,0.12)
Getting schematic propert bagGetting schematic propert bagINFO (SCH-1117): "nand2_4 schematic"
saved.
INFO (SCH-1170): Extracting "nand2_4 schematic"
INFO (SCH-1426): Schematic check completed with no errors.
Getting schematic propert bagGetting schematic propert bagINFO (SCH-1181): "Lab5 nand2_4 schematic"
saved.
LVS job is now started...
The LVS job has completed. The net-lists match.

Run Directory: /home/gouldj5/cadence/LVS
```

Fig. 8: LVS text output verification for NAND layout design showing no errors.

The successful LVS comparison displays a that the integrated circuit layout corresponded to the original schematic or circuit diagram of the design. Figure 8 displays the successful run of the inverter LVS design check of Figure 6 and Figure 14. A detailed view of the NAND LVS output is provided in Appendix Section VI-I

I. NAND Schematic

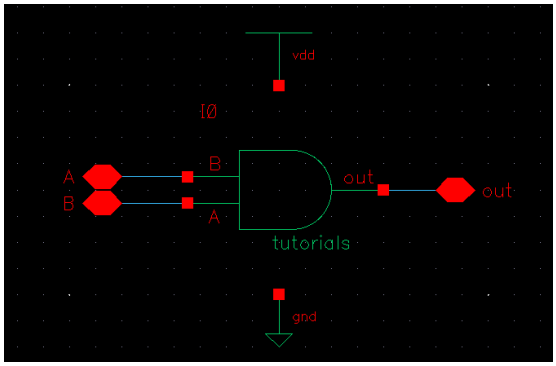

Fig. 9: Caption

The NAND symbol schematic is modeled after the extracted view of the Figure 15 with in-out pins at A, B, and out. Pins correspond to the pins displayed on the layout design of Figure 6 displaying for the output at Figure 10.

J. Post Layout Simulation

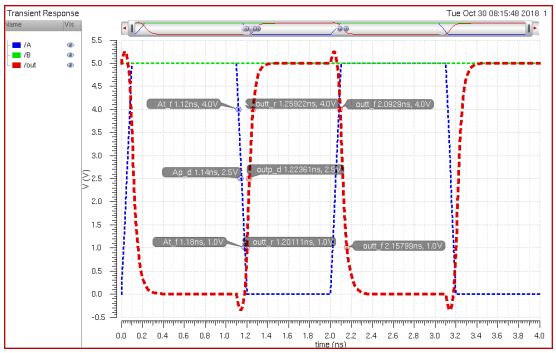

Fig. 10: Transient simulation of layout symbol (Figure 9) from 0 to 5 volt DC over time at varying input at 'B' and stable input at 'A' with 5 volt DC to vary output design. Simulation is labeled with time delay characteristics to show differences between a circuit based theoretical simulation.

Component	Delay	Value (ns)
A	t_f	0.06
A	t_r	0.06
Output	t_f	0.06509
Output	t_r	0.05811
In/Out	t_{pd}	0.075405

TABLE V: NAND Input to Output data with 'B' input set to a steady 5 Vdc involving rise, fall, and propagation delay for layout design transient simulation.

K. Result Comparison

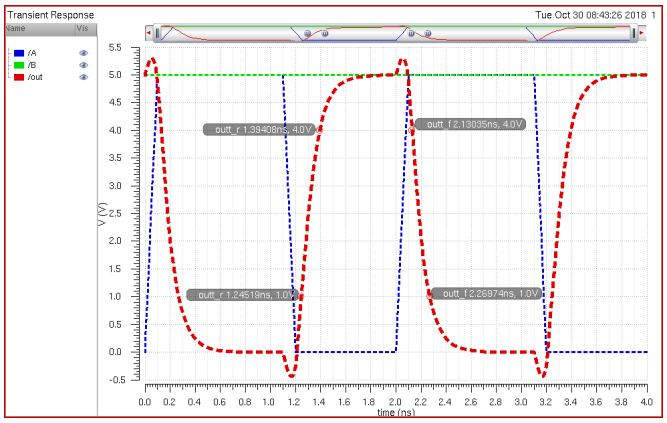

Fig. 11: Transient simulation of circuit from 0 to 5 volt DC over time at varying input at 'B' and stable input at 'A' with 5 volt DC to vary output design. Simulation is labeled with time delay characteristics to show differences between a layout based experimental simulation.

Similarly to the NOT design, the input of each circuit presented to be similar in that the input power to this layout and circuit are measured without any circuit modifications.

Component	Delay	Value (ns)
A	t_f	0.06
A	t_r	0.06
Output	t_f	0.12005
Output	t_r	0.07146
In/Out	t_{pd}	0.099895

TABLE VI: NAND Input to Output data with 'B' input set to a steady 5 Vdc involving rise, fall, and propagation delay for circuit-based delay.

Component	Percent Difference (%)
t_f	45.8 %
t_r	18.7 %
t_{pd}	24.5 %

TABLE VII: Comparison of values between Figure 10 and 11 displaying the percent error between each output value provided by the Tables of V and VI.

The NAND design output, similar to the NOT gate, produced by the layout of Figure 6 processes a lower propagation delay where a shorter amount of time between input and

output allows for a decreased system switch time and increased system stability. As such the absolute value of percent difference to the two systems show that the propagation delay of the layout design improved in performance allowing to make assumptions that the overall design of Figure 6 to be said to have improved the IC. Unlike the inverter however, the NAND design improved on all fronts, for time rise, fall, and propagation by a larger margin than the inverter. System improvements could be performed on reducing the distance between diffusion layers of the layout and the overall surface area.

V. Conclusions

In this experiment, layout design was implemented through the Cadence medium to perform a visual comparison of CMOS logic models. The NOT, NAND, and NOR layouts create a visual to show the surface area of the chip that relates to increase in production requirements and delay. DRC results of the layout circuit design, similar in given design rules, produced no errors. This verifies that the layouts followed design rules.

References

[1] *N. Weste and D. Harris, Principles of CMOS VLSI design*. Reading, Mass.: Addison-Wesley Pub. Co., 1993.

VI. Appendix

A. Lab 5 Data Tables

Component	Delay	Value (ns)	Component	Delay	Value (ns)
Input	t_f	0.06	Input	t_f	0.06
Input	t_r	0.06	Input	t_r	0.06
Output	t_f	0.05386	Output	t_f	0.05382
Output	t_r	0.05117	Output	t_r	0.04786
In/Out	t_{pd}	0.064710	In/Out	t_{pd}	0.064805

TABLE VIII: Inverter (NOT) Input to Output data involving rise, fall, and propagation delay for layout design transient simulation (left) and circuit-based delay (right).

Component	Delay	Value (ns)	Component	Delay	Value (ns)
A	t_f	0.06	A	t_f	0.06
A	t_r	0.06	A	t_r	0.06
Output	t_f	0.06509	Output	t_f	0.12005
Output	t_r	0.05811	Output	t_r	0.07146
In/Out	t_{pd}	0.075405	In/Out	t_{pd}	0.099895

TABLE IX: NAND Input to Output data with 'B' input set to a steady 5 Vdc involving rise, fall, and propagation delay for layout design transient simulation (left) and circuit-based delay (right).

B. NOT Circuit

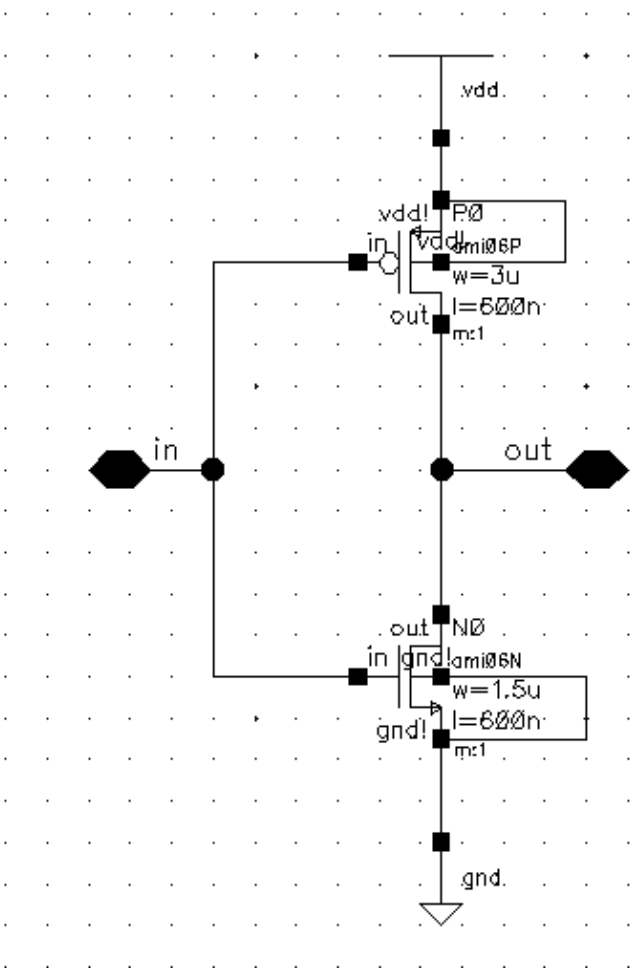

Fig. 12: Circuit design for NOT logic with PMOS to NMOS area of 2 to 1 respectively. Pin-outs for the circuit provided match the in-out pins of the schematic provided in Figure 3.

C. Inverter Netlist Extraction

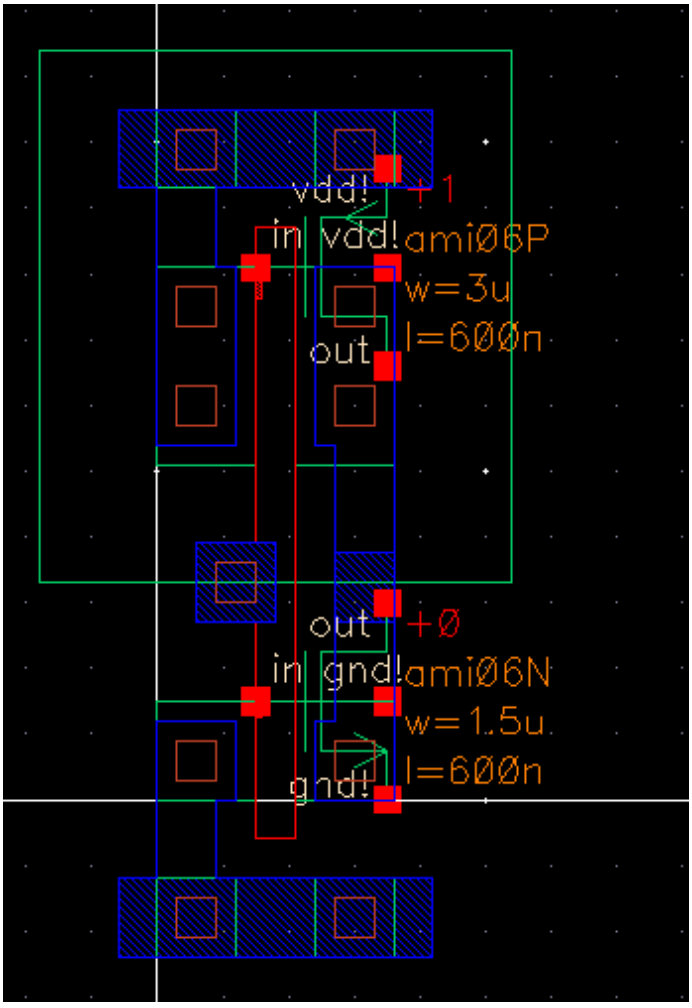

Fig. 13: Extracted view of inverter layout provided in Figure 1

D. NAND Circuit

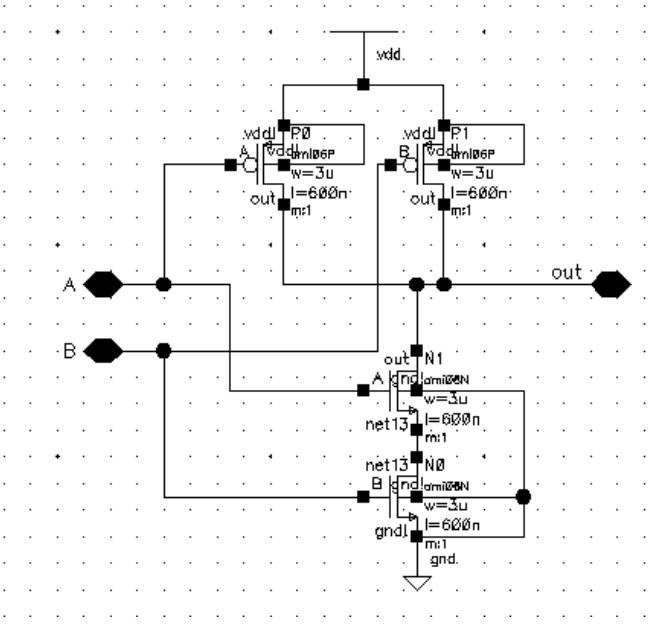

Fig. 14: Circuit design for NAND logic with PMOS to NMOS area of 2 to 2 respectively. Pin-outs for the circuit provided match the in-out pins of the schematic provided in Figure 9.

E. NAND extracted design

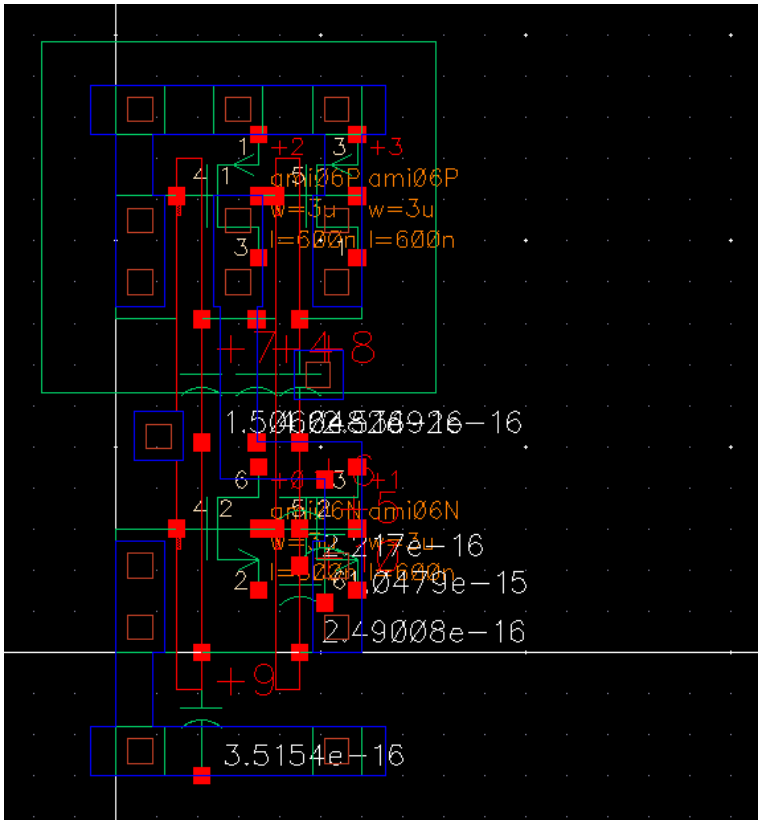

Fig. 15: Extracted view of NAND layout provided in Figure 6

F. NAND Detailed Output

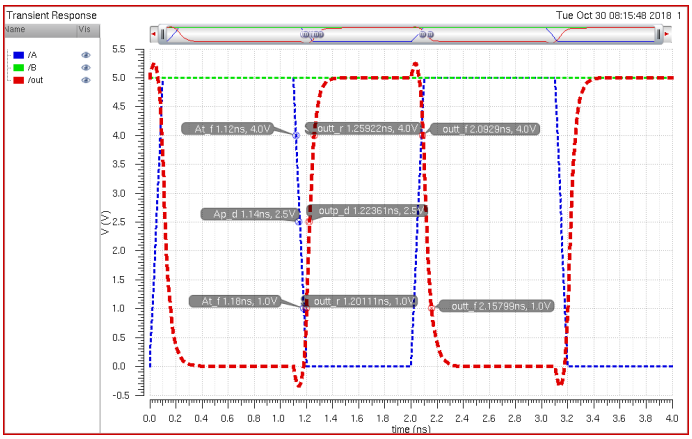

Fig. 16: Detailed output of NAND post-layout simulation.

G. Raw Data Input for Lab 5 Graph Measurements

```
------------------------------------
DATA LAB 5
------------------------------------
INV Graph
------------------
int_f @ 4 V = 1.12 ns
int_f @ 1 V = 1.18
int_r @ 4 V = 2.08 ns
int_r @ 1 V = 2.02 ns
inp_df@ 2.5 V = 1.15 ns
inp_dr@ 2.5 V = 2.05 ns

outt_r @ 4V = 1.23117 ns
outt_r @ 1V = 1.18 ns
outt_f @ 4V = 2.10161 ns
outt_f @ 1V = 2.15547 ns
outp_df @ 2.5V = 2.12574 ns
outp_dr @ 2.5V = 1.20368 ns

tpdf = 0.07574 ns
tpdr = 0.05368 ns
tpd = 0.064710 ns
------------------
Presim
------------------
outp_df @ 2.5V = 2.12574 ns
outp_dr @ 2.5V = 1.20387 ns
outt_r @ 4V = 1.23117 ns
outt_r @ 1V = 1.18 ns
outt_f @ 4V = 2.10161 ns
outt_f @ 1V = 2.15547 ns

inp_df@ 2.5 V = 1.15 ns
inp_dr@ 2.5 V = 2.05 ns
int_f @ 4 V = 1.12 ns
int_f @ 1 V = 1.18
int_r @ 4 V = 2.08 ns
int_r @ 1 V = 2.02 ns

tpdf = 0.07574 ns
tpdr = 0.05387 ns
tpd = 0.064805 ns

--------------------
NAND GRAPH
--------------------

At_f @ 4 V = 1.12ns
At_f @ 1 V = 1.18ns

Ap_df@ 2.5 V = 1.14ns
Ap_dr@ 2.5 V = 2.05ns

outt_r @ 4V = 1.25922ns
outt_r @ 1V = 1.20111ns

outt_f @ 4V = 2.09290ns
outt_f @ 1V = 2.15799ns

outp_df @ 2.5V = 1.22361ns
outp_dr @ 2.5V = 2.11720ns
size  = 9.6 x 18.9
--------------------
Presim
--------------------

outt_r @ 4V = 1.39408ns
outt_r @ 1V = 1.24519ns
tr_out = 0.07146
outt_f @ 4V = 2.13035ns
outt_f @ 1V = 2.26974ns
t_f_out = 0.12005
tpdf = 1.22066-1.15
tpdr = 2.17913-2.05
tpd = 0.099895
```

H. LVS Text Output for Inverter Design

```
    @(#)$CDS: LVS version 6.1.6 09/01/2015 15:36 (sjfnl125) $

Command line: /opt/cadence/installs/IC616/tools.lnx86/dfII/bin/32bit/...
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/gouldj5/cadence/LVS/layout/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos

    Net-list summary for /home/gouldj5/cadence/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N0        N0        gnd!
    N3        N5        in
    N2        N3        out
    N1        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 2       2
        total                  2       2

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 4       4
        total                  4       4

                               terminals
```

```
        un-matched              0       0
        matched but
        different type          0       0
        total                   4       4


Probe files from /home/gouldj5/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /home/gouldj5/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

I. NAND LVS Detailed View

```
@(#)$CDS: LVS version 6.1.6 09/01/2015 15:36 (sjfnl125) $

Command line: /opt/cadence/.../gouldj5/cadence/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/gouldj5/cadence/LVS/layout/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos
```

```
    Net-list summary for /home/gouldj5/cadence/LVS/schematic/netlist
       count
         6               nets
         5               terminals
         2               pmos
         2               nmos


    Terminal correspondence points
    N3        N6        A
    N2        N7        B
    N1        N0        gnd!
    N5        N2        out
    N4        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                             layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  6       6
        total                   6       6

                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   5       5


Probe files from /home/gouldj5/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:
```

prunedev.out:

audit.out:

Probe files from /home/gouldj5/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out: