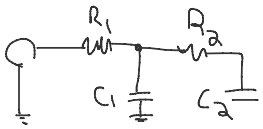
Midterm Study

Monday, November 5, 2018 12:53 PM

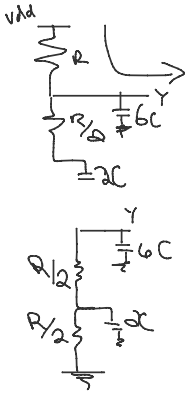
(1) Elmore Delay

$t_{pd_{0\to i}} = \sum R_{ij}C_j$



$t_{pd_{@v1}} = \sum R_{1j}C_j = R_1C_1 + R_1C_2$
$t_{pd_{@v2}} = R_1C_1 + (R_1 + R_2)C_2$

Parallel → R
Series → $R/2$



Worst case delay = filled "buckets" capacitors at max.

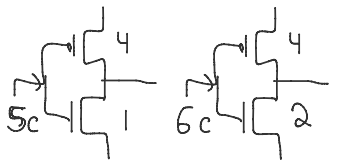
charging $(V_{dd} \to Y) = t_{pdr} = 6C * R + (2C)\left(\frac{R}{2}\right)$

discharg(gnd → Y) $= t_{pdf} = \left(\frac{R}{2}\right)(2C) + R(6C)$

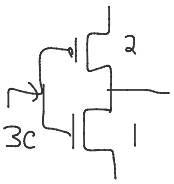
$t_{pd_{avg}} = (t_{pdr} + t_{pdf})/2$

(2) Logical Efforts

def… measure of input capacitance for same condition (chrg/disc)



Charging



Discharging

Add capacitive values with respect to proper ratio of that logic gate

$g_c = \frac{5}{6} = \frac{g_o}{g_{dc}}$

$g_d = \frac{5}{3} = \frac{g_o}{g_{dd}}$

$g_{av} = \frac{g_c + g_d}{2} =$

(3) Power Consumption

$P_{dyn} \cong P_{sw} + P_{short}$ → 0

$P_{sw} = \alpha C V_{dd}^2 f$

$P_{static} = V_{dd} \cdot \sum I_{leak} \Rightarrow$
- gate → 50%
- subthreshold → 50%
- junction ≅ 0%

Delay

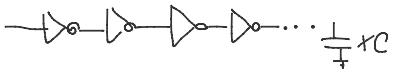
$d = gh + p$
f = effort delay = gh
g = logical delay
h = electrical effort = $\frac{C_{out}}{C_{in}}$
p = parastic delay

Logical Effort

Gate	1	2	3	N
Inv	1	-	-	-
NAND	-	4/3	5/3	(n+2)/3
NOR	-	5/3	7/3	(2n+1)/3
Mux	2	2	2	2
XOR		4,4	6,12,6	

Parasitic Delay

Gate	1	2	3	N
Inv	1	-	-	-
NAND	-	2	3	n
NOR	-	5/3	7/3	n
Mux	2	4	6	2n
XOR		4	6	



$\hat{f} = (F)^{\frac{1}{N}} = \sqrt{F}$
$N = \log_4(X) \Rightarrow$ Get N between 3 and 4 for best delay
Fanout = h = $\frac{xC}{C_{in}}$

5.1 You are synthesizing a chip composed of random logic with an average activity factor of 0.1. You are using a standard cell process with an average switching capacitance of 450 pF/mm^2. Estimate the dynamic power consumption of your chip if it has an area of 70 mm^2 and runs at 450 MHz at $V_{DD} = 0.9$ V.

$\alpha = 0.1$
$\frac{C}{mm^2} = 450 \frac{pF}{mm^2}$
$A = 70\ mm^2$
$f = 450\ MHz$
$V_{DD} = 0.9\ V$

$P_{dym} = \alpha C V_{dd}^2 f = (0.1) * \left(\frac{450pF}{mm^2} * 70mm^2\right) * (0.9^2) * (450{,}000{,}000) = \mathbf{1.15\ W}$

Example 5.4

Consider the system-on-chip from Example 5.1. Subthreshold leakage for OFF devices is 100 nA/μm for low-threshold devices and 10 nA/μm for high-threshold devices. Gate leakage is 5 nA/μm. Junction leakage is negligible. Memories use low-leakage devices everywhere. Logic uses low-leakage devices in all but 5% of the paths that are most critical for performance. Estimate the static power consumption.

$I_{low} = \frac{100nA}{\mu m}$
$I_{high} = \frac{10nA}{\mu m}$
$I_{gate} = \frac{5nA}{\mu m}$

λ= 65 nm process
Logic width = 12 λ
Memory width = 4 λ
Logic uses low in all but 5%
Channel Lengths drawn = .025 μm
$\#_{logic} = 50\ 10^6$
$\#_{mem} = 950\ 10^6$

$T_{highlog_{5\%}} = 50 * 10^6\ (0.05)(12\lambda)\left(\frac{0.025\ \mu m}{\lambda}\right) = 0.75 * 10^6 \mu m$

$T_{lowlog_{95\%}} = 50\ * 10^6(0.95)(12\lambda) + 950 * 10^6(4\lambda)(\frac{0.025\mu m}{\lambda}) = 109.25 * 10^6 \mu m$

$I_{logsub} = 0.75 * 10^6(100nA) + 109.25 * 10^6(10nA)/2 = 584mA$

$I_{gate} = 0.75 * 10^6 \mu m * \frac{100nA}{\mu m}\left(\frac{\left(5\frac{nA}{\mu m}\right)}{2}\right) = 275\text{mA}$
$P_{static} = 275 + 584 = \mathbf{859mA}$

5.10 Design a header switch for a power gating circuit in a 65 nm process. Suppose the pMOS transistor has an ON resistance of about 2.5 kΩ · μm. The block being gated has an ON current of 100 mA. How wide must the header transistor be to cause less than a 2% increase in delay?

$\lambda =$ 65 nm process
$R_{on} = 2.5\ k\Omega\ * \mu m$
$R = \frac{2.5}{0.065} = 38.46\ \text{k}\Omega$

I_{on}=100 mA
Delay increase = 0.02 = 2%
$R_{eff} = \frac{20mV}{100mA} = 0.2\Omega$

$W = 2.5k\Omega * \mu m$ / 0.0002kΩ = 12,500 $\mu m = \mathbf{12.5\ mm}$