Electronics I
Homework, Set 1

Sedra/Smith, Chapters 1 & 2

NOTE: The following problems are suggested as representing a good range of important topics and represent both examples from the chapter as well as problems at the end of the chapter. Work enough problems so you feel comfortable with the key concepts introduced (and/or reinforced) during Week 1. Problems that are to be turned in are indicated by ***BOLD**.

Exercises 1.12, 1.13, 1.14: Amplifier inputs/outputs
Example 1.5: Freq response
Exercise 2.3: Op amp model
Example 2.1: Effects of finite gain; also include A=10^6
Example 2.2: "T" fdbk network
Exercise 2.6
Example 2.3: IA

***RD-1: For a real design problem, consider an available industry IA. Referring to the circuit topology shown in the INA126 datasheet, analyze the circuit to verify the manufacturer's gain equation**

$$\boldsymbol{G = 5 + \frac{80k}{R_G}}$$

Section 2.5.2, "Miller Effect." Also read, 9.4.4
Example 9.7: Miller effect
Read 10.2, "some properties of neg fdbk"
Section 2.6.2: note i_b compensation methods

***RD-2: For modern op amps with i_b on the order of pA, do you think explicit i_b compensation—e.g., R3 in Fig 2.34, is necessary? Why or why not?**

Example 2.6: Closed loop freq response
Exercise 2.27: Freq response
Exercise 2.28: Freq response
Exercise 2.30: Full pwr bw

Chapter Problems
2.6 Common mode, differential mode signals

***2.9 Inverting Amp, resistor tolerance**

D2.2 Design an Inv Amp
2.25 Compensating for a finite A

***D2.42 Diff Amp design**

***2.43 IDAC; change to achieve $0 \leq Vo \leq -3.3V$**

D2.50 Analysis of Diff Amp using superposition

***D2.51 Var gain using pot**

2.53 Use of buffer
2.81 Miller effect

***D2.93 H(s) for op amp, Bode plot**

2.94 Eos

***2.95 Eos + signal**

2.107 Finite GBW

***D2.117 Cascading amps**

D2.118 More cascaded amps
2.125 SR

***D2.127 The compleat op amp designer**