Lab 3: Symbol Editing and Transient Simulations

Joshua Gould
VLSI 09414
Date: 10-09-2018
Emails: gouldj5@students.rowan.edu

***Abstract*—In this experiment, the schematic design of a CMOS inverter was developed in the Cadence medium to understand CMOS inverter transfer characteristics, delay characteristics, switching threshold, and the inverter oscillator. Steps in inverter simulations showed how the CMOS inverter switches depending on the voltages applied to the system and the parameters of the MOSFET. As a result, the input and output voltage curve was plotted over time to find delay parameters of rise time, fall time, and average propagation time for both the inverter and the inverter oscillator. These values increased as more inverters were added to the oscillator system showing a trend of CMOS devices increasing with delay.**

I. Introduction and Objectives

The software used in this experiment should be used to manipulate an inverter circuit through transient simulations and produce an inverter symbol for inverter software packaging of oscillator creation. After observing the behavior of an inverter circuit, the circuit of Figure 1 is packaged into a not gate symbol. The static behavior of CMOS inverter can then be put through a series of eleven circuits to derive delay properties for analysis. Over the Cadence software, output characteristics should be described for both inverter designs to be compared as a final result. It is expected for the oscillator to add a larger delay to the inverter measurements and with each inverter added to the oscillator, the time of the total delay increases for propagation, fall, and rising time delay.

II. Background and Relevant Theory

A. Metal-Oxide Semiconductor Field-effect Transistors

A MOSFET is a three-terminal semiconductor device that controls current from the gate voltage (V_{GS}). In the regions of a CMOS, MOSFETs operate as either a voltage-controlled resistor or an ideal current source respectively. Additionally, the PMOS transistor takes the opposite characteristics to the NMOS. Where, in the right region, one device would go voltage "high", the other MOSFET would go voltage "low" or 0 volts. This characteristic generates a switch or inverting circuit when used together which is detailed with background on the Voltage Transfer Curve[1].

B. The Voltage Transfer Curve & The Inverter

Transition between inverter MOSFET states occurs when voltage is applied to the gate of the CMOS device. For instance, NMOS transistor in Figure 1 would go from off to the on-state when gate voltage is more positive than NMOS threshold (V_T), intrinsic to the inverter. Similar logic is applied to PMOS transistor in negative direction. Specifically, when the voltage input is low, the NMOS in Figure 1 is off and no current can flow between the gate of the negative tranisistor and the source. At the same time, low input voltage means the VDD is transferred to gate of PMOS. Once input to the PMOS gate is set to VDD, PMOS is off and NMOS is on. NMOS in this state acts as a pull-down transistor connecting the output of the system to ground. This circuit performs as an inverter, where low input causes high output.

C. Delay

Delay within an inverter system can be measured to shown the imperfections set by a transistor used in a design or the elements surrounding the transistor. For this design, delay characteristics of concern are the rise time, fall time, and propagation delay.

D. Rise & Fall Time

Rise time and fall time is the time between 20% and the 80% of the total transfer curve values. Specifically, rise time is the difference of time between the 20% of the total value to 80% of the total value. In this example, Equation1 and Equation 2 refers to these properties. These properties are measured on the input and output signal[1].

$$t_f = |t_{VDD@80\%} - t_{VDD@20\%}| \tag{1}$$

$$t_r = |t_{VDD@20\%} - t_{VDD@80\%}| \tag{2}$$

E. Propagation Delay

Propagation delay refers to the maximum time from the input crossing signal at 50% to the output crossing signal at 50%. The average of the values at the rise and fall of the input and output signal is the propagation delay (t_{pd}) represented by Equation 3[1].

$$\frac{t_{pdf} + t_{pdr}}{2} \tag{3}$$

F. Oscillators

An electronic oscillator is a circuit that produces a periodic, oscillating signal, often a sine wave or a square wave. An N-stage ring oscillator has a period of 2N stage delays. However, since the polarity flips in one cycle around the oscillator, the period to regain polarity is $T = 2 * 2N = 4N$ where the frequency is $\frac{1}{T} = \frac{1}{4N}$. These ring oscillators are often used to judge if a particular chip is slower than expected. The oscillation frequency should be lower than the frequency of

one inverter set by the experiment as the number of inverters are added in series.

III. Procedure

In this experiment, cadence was implemented as a medium to create a transient simulation of a CMOS inverter. Specifically, the CMOS circuit was shown at the transfer of the input wave and the output, displaying the output characteristics of the inverter. Comparing these two resulting square waves allowed for the calculation of the specified delay characteristics.

In the symbol editor, the inverter circuit was tied to a not gate symbol. Each characteristic of the inverter circuit was then placed in series eleven times over to create an oscillator. These alternating curves at each not gate output was plotted for delay calculations and comparison to the original inverter delay characteristics.

IV. Results and Discussion

A. Circuit Design

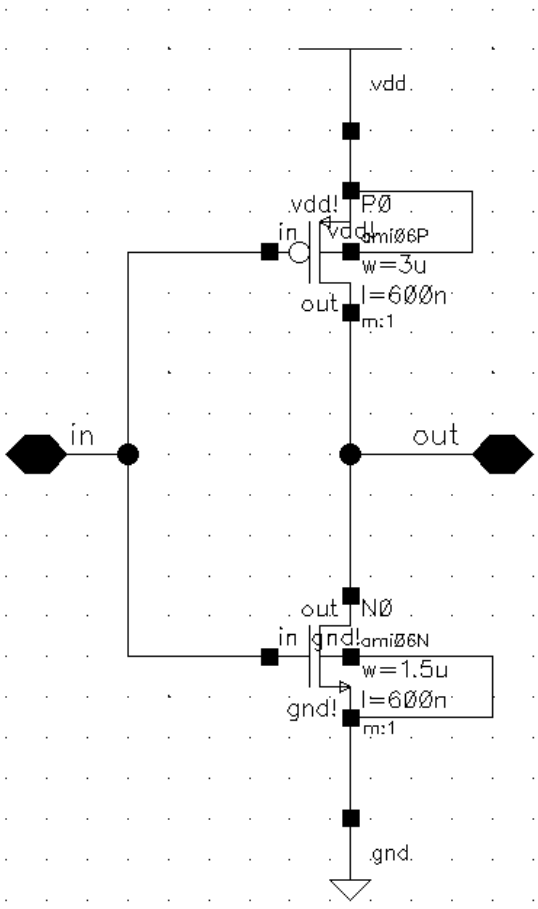

Fig. 1. Inverter schematic produce in Cadence Virtuoso IDE using an NMOS and PMOS of W/L, 3/0.6 and 1.5/0.8 respectively

B. Inverter Symbol Design

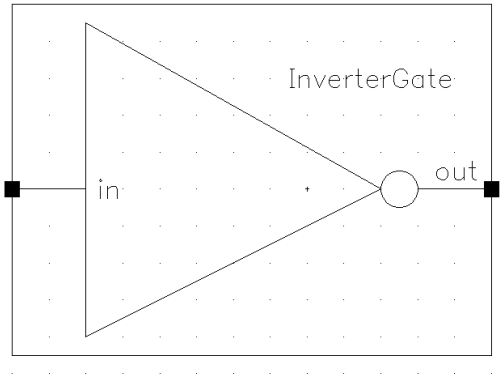

Fig. 2. Inverter circuit converted to a not gate symbol with input and output pins

C. Inverter Output

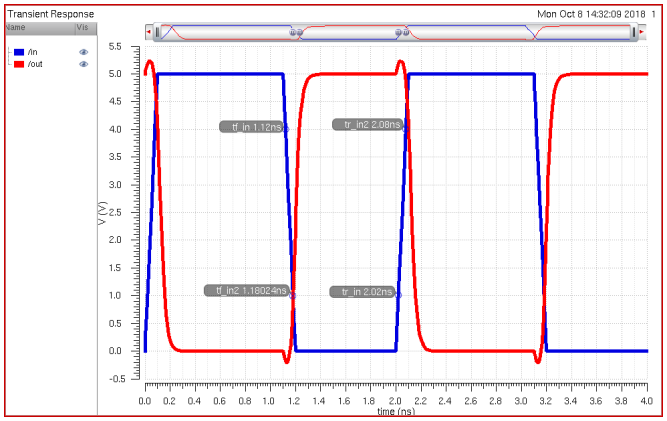

Fig. 3. Inverter circuit graphical output with plotted rise and fall time values of the input.

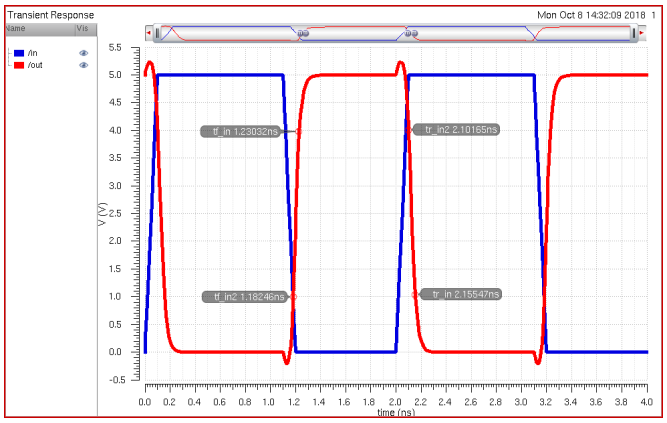

Fig. 4. Inverter circuit graphical output with plotted rise and fall time values of the output.

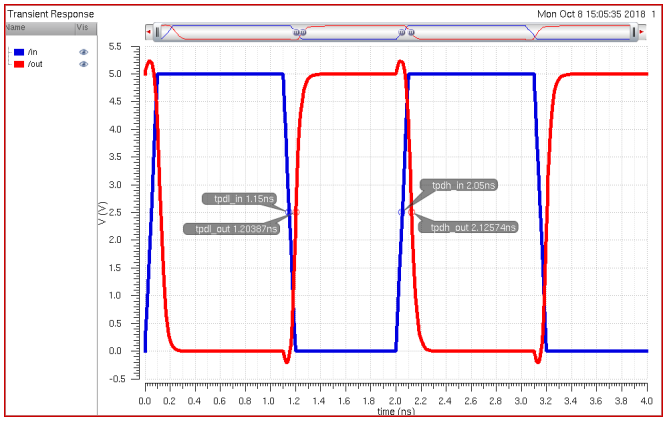

Fig. 5. Inverter circuit graphical output with plotted propagation delay values.

Figures 3 through 5 display the delay characteristics of the output signal from the original inverter. In comparison to the input, the output signal produces a maximum signal that is larger and smaller then the maximum input given by the input signal of 5V and 0V. As such, the states at each point are producing noise to raise or lower the maximum voltage. This, along with the delay, is reasons for the output to be less similar to a square wave from logical '1' to '0'.

D. Delay Calculations of Single Inverter

At the input signal, the fall time was calculated to be 0.06054 ns according to Figure 3 using Equation 1. The input signal delay was shown to compare to the output signal delay of the oscillation in Figure 7 and the inverter of Figure 4. Notably, the input rise and fall time are larger than the output of the inverter.

$$t_{fin} = |1.18054ns - 1.12ns| = 0.06054ns \quad (4)$$

Equivocally, Equation 5 finds the rise time to be 0.06ns.

$$t_{rin} = |2.02ns - 2.08ns| = 0.06ns \quad (5)$$

At the output signal, the fall time was calculated to be 0.06 ns according to Figure 4 using Equation 1.

$$t_{fout} = |1.2302ns - 1.18246ns| = 0.04774ns \quad (6)$$

Equivocally, Equation 7 finds the rise time to be 0.06ns.

$$t_{routs} = |2.10165ns - 2.15547ns| = 0.05382ns \quad (7)$$

As for propagation delay, Equation 3 is used to find the propagation of Figure 5 giving an average propagation delay of 0.06481 ns.

$$t_{tpdf} = 1.20387ns - 1.15ns = 0.05387ns \quad (8)$$

$$t_{pdr} = 2.12574ns - 2.05ns = 0.07574ns$$

It is expected for the oscillator to add a larger delay to the inverter measurements and with each inverter added to the oscillator, the time of the total delay increases for propagation, fall, and rising time delay.

$$t_{pd} = \frac{t_{pdf} + t_{pdr}}{2} = \frac{0.05387 + 0.07574}{2} = 0.064805ns$$

E. Oscillator Design

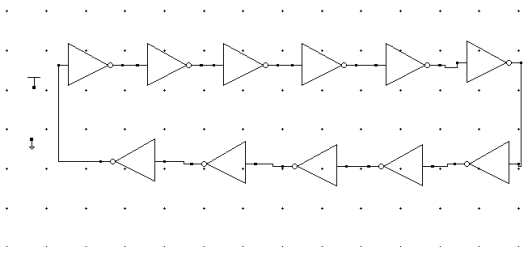

Fig. 6. Oscillator design using eleven not gates of the inverter circuit provided by Figure 1 connected in series

F. Oscillator Output

Notably, as shown by Figure 6, the inverters are connected in series to measurement nodes between each inverter channel. Figure 7 displays that these inverter outputs shift and stack on top of each other to produce a wave of inverting signal similar to Figure 4. Reasonably, the total number of output voltage plots were reduced for easier reading of the oscillator plot from 11 to 4.

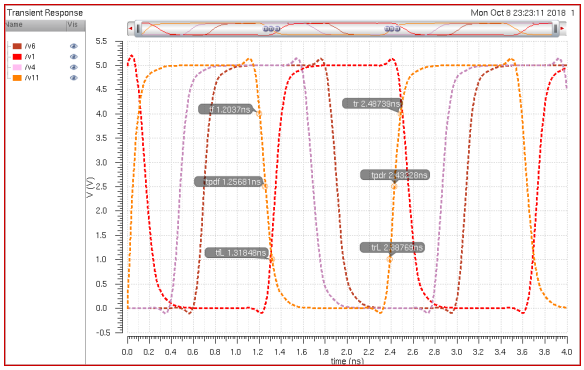

Fig. 7. Oscillator graphical output of circuit provided by Figure 6. System plotted accounted for the 1st, 4th, 6th, and 11th inverter with delay measurements respectively labeled on the 11th inverter values.

G. Delay Calculations and Comparison of Oscillator Inverter

At the output signal, the fall time was calculated to be 0.11478 ns according to Figure 4 using Equation 1.

$$t_{foutosc} = |1.2037ns - 1.31848ns| = 0.11478ns \quad (9)$$

Equivocally, Equation 7 finds the rise time to be 0.0997 ns.

$$t_{routosc} = |2.48739ns - 2.38769ns| = 0.0997ns \quad (10)$$

As for propagation delay, Equation 3 is used to find the propagation of Figure 7 giving an average propagation delay of 0.244525 ns.

$$t_{tpdf} = 1.25681ns - 1.15ns = 0.10681ns \quad (11)$$

$$t_{pdr} = 2.43224ns - 2.05ns = 0.38224ns$$

$$t_{pd} = \frac{t_{pdf} + t_{pdr}}{2} = \frac{0.10681 + 0.38224}{2} = 0.244525ns$$

In comparison, every value of delay was increased by the oscillator design. For specific comparison, fall time, rise time, and propagation delay all increased by 0.6704, 0.04588, and 0.17972 respectively. Increases in these delay parameters are due to the increase in inverter designs between the output of the last inverter node and the input voltage applied to the system. With each inverter added to the oscillator, the time of the total delay increases for propagation, fall, and rising time delay.

V. Conclusions

The experiment showed the transient characteristics of the inverter circuit through Cadence symbol design. This is shown on the plot comparison between the one inverter circuit of calculated delay and an eleven inverter oscillator delay. More specifically, the sweep of voltage showed that when the number of inverters increased, the total delay at each inverter increased.

References

[1] *N. Weste and D. Harris, Principles of CMOS VLSI design*. Reading, Mass.: Addison-Wesley Pub. Co., 1993.