Lab 4: MOSFET Layout Design

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***Abstract*—The circuit design layout design of CMOS logic circuits determines a compact architecture for physically designing a logical transistor circuit. Following design rules for NOT, NAND, and NOR logic schematics allowed to design the fabrication using the smallest area possible. Circuit layout design also displays differences in logic overview and characteristics of layer distribution. Visually, it is simple to tell that NOR logic layouts require more surface area than the NAND logic circuits. Equivocally, NAND logic design is more cost-effective and possesses a higher storage capacity in logic design for its physical layout size.**

I. Introduction and Objectives

The goal of this lab report was to introduce design layouts of transistor circuits and analyze the layers behind the logic layouts. Basic concepts were introduced with logical gate understanding of the inverter, NAND, and NOR gates. Using CMOS architecture to construct these gates, design rules must be followed to produce the smallest surface area for each design. This was done by using design rule checkers (DRC). Layered designs were introduced through stick diagrams of the circuit which gave a greater understanding of the layout architecture at each logic device.

II. Background and Relevant Theory

A. CMOS Logic

CMOS logic allows for computational commands to be carried out by the electrical properties of the transistors inside the design. Using CMOS components, the NMOS and PMOS transistors can possess complex logic functions by changing the paths between gates. When a circuit path consists of two transistors in series, the logical modelling corresponds to AND logic. In parallel, the transistor model represents OR logic. An advantage of CMOS logic against an simple NMOS or PMOS logic design is that transitions between high and low are fast since the PMOS device low resistance when switched on and the NMOS device has opposite features to pull to ground. Finally, the output signal from the CMOS logic produces full voltage between the low and high supplies[1].

B. NOT Gate

Also known as an inverter, the NOT gate flips the state of the input signal to the opposite. The NOT gate is the most basic design for CMOS logic, displaying the NMOS and PMOS pairing characteristics. The table of logic is provided in Table I.

A	Y
0	1
1	0

TABLE I
Logic table of NOT inverter circuit

Table I ,with an input (A) at ground value of 0, displays that the PMOS transistor in the circuit pulls the source voltage to the output (Y) pin to high. With input at a high value of 1, the NMOS pulls down the output to 0.

C. NAND Gate

Transistors in NAND gate have equal size where as NOR gates do not. This is illustrated in the width and length of the NMOS and PMOS of Figure 4 and 7 respectively. Which reduces manufacturing cost of NAND gate. When considering gates with more inputs, NOR gates requires transistors of 2 different sizes whose size difference is more when comparing with NAND gates. The table of logic is provided in Table II.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

TABLE II
Logic table of NAND circuit

With a 2-input NAND gate, Table II takes two inputs of A and B. Here, the output is pulled low only when both A and B are both turned high.

D. NOR Gate

Addressing the sizes of transistors in Figure 7, NOR is presently greater than that of the NAND logic circuit. With a PMOS size of 4 and NMOS size of 1 against the 2 to 2 size of the NAND increase, as the number of inputs are increased, the size of the overall silicon area design.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

TABLE III
Logic table of NOR circuit

With a 2-input NOR gate, Table III takes two inputs of A and B. Here, the output is pulled high only when both A and B are both turned low.

E. CMOS Layout Architecture

CMOS architecture and layout design can be constructed using the layers of conductive and insulating composition. The layers used in this design for all models are listed in Table IV along with the purpose of each layer.

Layer	Description
n-well	creation formed on a bare p-type silicon wafer to lay the base for NMOS transistor design
n+ diffusion	lays ground for the transistor active area of negative diffusion
p+ diffusion	lays ground for the transistor active area of negative diffusion
polysilicon	establishes connection between NMOS and PMOS through a polysilicon layer
metal	used to connect metal contact between transistors and to output, VDD, and ground pins
contact	position to distinguish connections for CMOS and provide a contact for metal layers

TABLE IV
DESCRIPTIONS OF LAYOUT DESIGN LAYERS

The inputs to the NAND are in the polysilicon layer where each polysilicon layer can represent an input channel. The CMOS transistors are formed by through polysilicon and diffusion. The output is connected through metal between the devices. Connections between metal, polysilicon, and diffusion are made through contacts. The physical layout follows the example inverter design of Figure X. The N-device is created within the P-type substrate. The P device is manufactured in the n-well. As for power, the P-type substrate connects to the source voltage and the N-type n-well is connected to drain voltage [1].

F. Design Rules

The main objectives of layout design rules are to build reliably functional circuits in as small of an area as possible. Design rules are defined regarding layer separations, feature sizes, and overlaps. A common rule set is lambda-based design rules. These rules base design on a single value Lambda that describes resolution of the design process as a unit of generally half of the transistor channel length. Total verification of a chip involves the design rule check (DRC) and layout versus schematic (LVS) along with a few other checks. For this experiment, each layout was only run under DRC. Design rules represent a compromise between chip performance and electrical yield with stricter rules producing greater opportunity for circuit improvements. A layout that violates design rules may still function correctly, however, difference from design rules can jeopardize the success of a design[1].

G. Delay

Delay of logic circuits does not hold a lot of details for layout design but provides a greater understanding for size of layouts against the performance of a given logic circuit. Comparisons between NAND and NOR logic delays can be performed using Equation 1.

$$Delay = t(gh + p) \tag{1}$$

where g is logical effort, h is electrical effort, p is parasitic delay, and t is the technology constant.

III. Procedure

Cadence Layout Design software was used to develop the layout circuit design process. As a start, an inverter was created in the Cadence software. Layers explained by Table IV were used in this design. Layers, as followed, were laid in order. The NMOS active layer, gate poly, active contacts, metal connections, n-select layer, pmos active, nwell, supply rails, substrate and well contacts, transistor nodes, rule checking DRC output, Layout of NAND and NOR DRC results

IV. Results and Discussion

A. Inverter Circuit

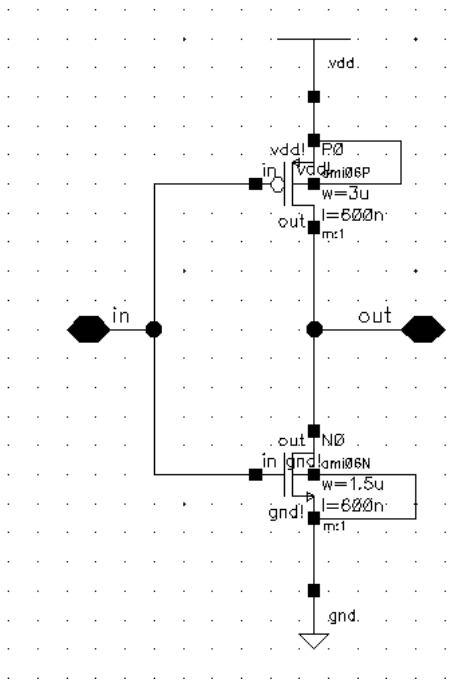

Fig. 1. Inverter circuit with CMOS size design of 2 to 1

B. Stick diagram of NOT circuit

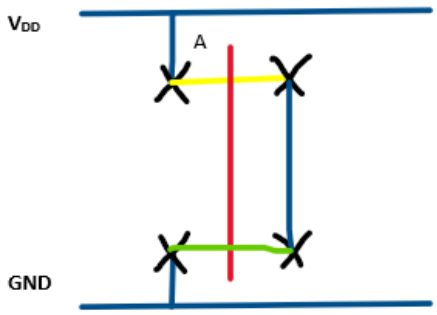

Fig. 2. Stick diagram of NOT circuit displaying circuit layers.

Stick diagrams describe a circuit topography and layer information using simple lines. In this, the colors of the diagram give a basic description of the layer location. Red lines in this diagram pertain to the polysilicon layer. Top and bottom blue lines pertain to the power and ground lines, while the middle blue line pertains to metal layering that relates to the output of the CMOS logic. Black X's provided at intersections are the contacts. Finally, yellow and green pertain to PMOS and NMOS specifications respectively. These rules apply to the stick diagrams of the NAND and NOR logic circuit of Figure 5 and 8

C. Inverter Layout

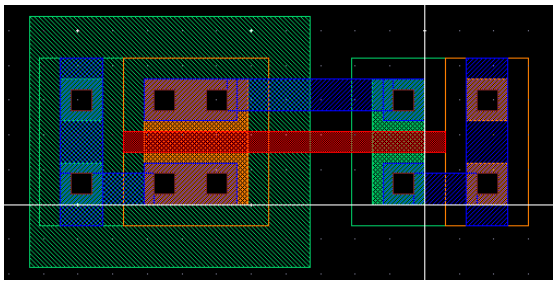

Fig. 3. Layout of Inverter NOT circuit displaying circuit layers.

For the first layout design, the inverter layout was derived from the stick design of Figure 2. Notably, the number of contacts within the PMOS layer directly corresponds to the size differential of the PMOS and NMOS W/L in the circuit Figure 1.

Design rules from this design extended to 0.3λ, which follows true for all layout grids. Using this rule, it was a possibility to create a structured and compact design.

D. NAND Circuit

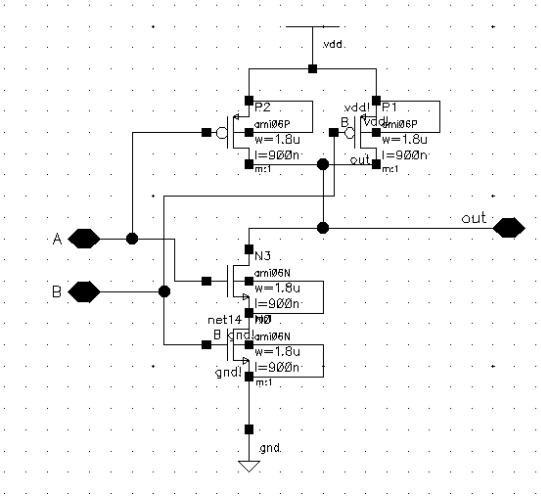

Fig. 4. NAND circuit displaying CMOS size design of 2 to 2.

E. Stick diagram of NAND

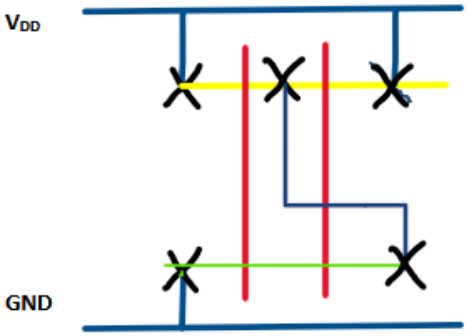

Fig. 5. NAND circuit stick diagram.

F. NAND Layout

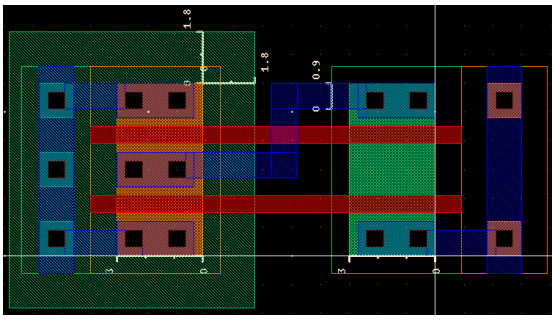

Fig. 6. Layout of NAND circuit displaying CMOS size design of 2 to 2 with measurement on layout design.

G. NOR Circuit

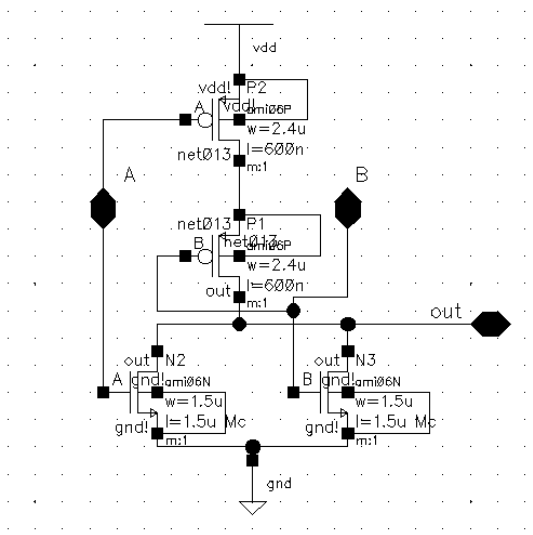

Fig. 7. NOR circuit displaying CMOS size design of 4 to 1.

The NOR layout provided an apparent increase in surface area architecture. As such, the total theoretical cost of the design would increase with area during production along with the delay. The NOR gate produces a logical effort of $\frac{5}{3}$ comparatively to the lesser $\frac{4}{3}$ logical effort of the NAND[1].

H. Stick diagram of NOR

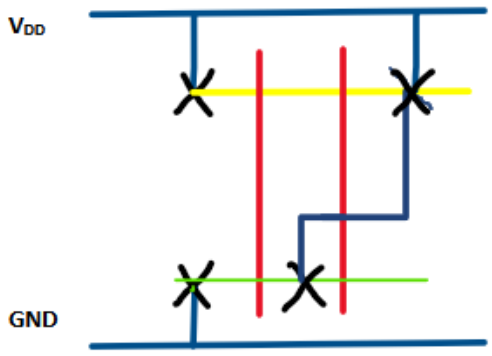

Fig. 8. NOR circuit stick diagram.

I. NOR Layout

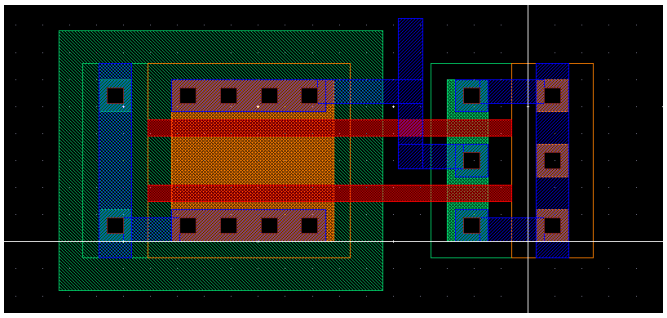

Fig. 9. Caption

V. Conclusions

In this experiment, layout design was implemented through the Cadence medium to perform a visual comparison of CMOS logic models. The NOT, NAND, and NOR layouts create a visual to show the surface area of the chip that relates to increase in production requirements and delay. DRC results of the layout circuit design, similar in given design rules, produced no errors. This verifies that the layouts followed design rules.

References

[1] *N. Weste and D. Harris, Principles of CMOS VLSI design*. Reading, Mass.: Addison-Wesley Pub. Co., 1993.

APPENDIX

A. DRC results

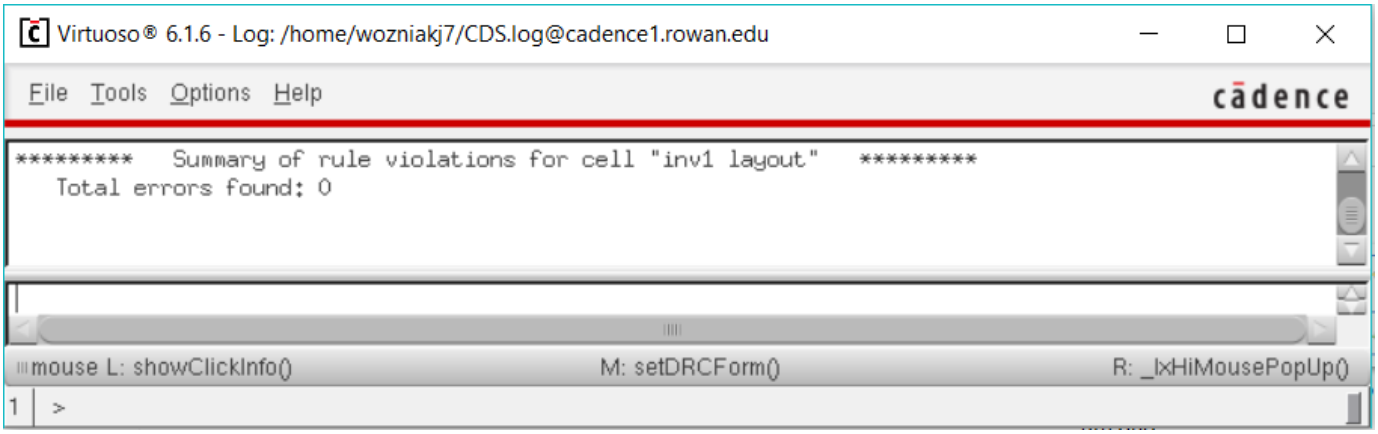

Fig. 10. DRC output check on inverter layout provided in Figure 3

Fig. 11. DRC output check on NAND layout provided in Figure 6

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DRC started.....Fri Oct 19 19:13:39 2018
    completed ....Fri Oct 19 19:13:39 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "nor2_4 layout"   *********
   Total errors found: 0
```

Fig. 12. DRC output check on NOR layout provided in Figure 9