Lab 2: Design and DC Simulation of an Inverter

Joshua Gould
VLSI 09414
Date: 9-21-2018
Emails: gouldj5@students.rowan.edu

***Abstract*—In this experiment, the schematic design of a CMOS inverter was shown through the Cadence medium to understand CMOS inverter static voltage transfer characteristics, switching threshold, noise margins, and the relationships between VTC, Noise margin variables, and the width of a transistor. Steps in DC simulations showed how the CMOS inverter switches depending on the voltages applied to the system and the parameters of the MOSFET. As a result, a Voltage Transfer Curve (VTC) was generated for analysis to compare between trends in the noise margin input, output, highs, and lows.**

I. Introduction and Objectives

After gaining access and familiarity with Linux-based design, the software is used to manipulate inverter design with DC simulation. After observing the behavior of an inverter circuit, more complex digital logic gates can be derived. In this, the static behavior of CMOS inverter is understood by using simple switch model of MOSFET transistors. Understanding the DC characteristics and parameter effects on the output of the circuit led to the better understanding of the circuit.

II. Background and Relevant Theory

A. Metal-Oxide Semiconductor Field-effect Transistors

A MOSFET is a three-terminal semiconductor device that controls current from the gate voltage (V_{GS}). A NMOS device was implemented for circuit analysis. There are two regions that the transistor operates depending on the voltage applied. The first region is called the "triode" region while the second is called "saturation" region. In these regions, MOSFETs operate as either a voltage-controlled resistor or an ideal current source respectively. Additionally, the PMOS transistor takes the opposite characteristics to the NMOS. Where, in the right region, one device would go voltage "high", the other MOSFET would go voltage "low" or 0 volts. This characteristic generates a switch or inverting circuit when used together which is detailed with background on the Voltage Transfer Curve.[2]

B. The Voltage Transfer Curve

The transition between inverter states occurs when voltage is applied to the gate of the CMOS device. For instance, NMOS transistor in Figure 2 would go from off to the on-state when gate voltage is more positive than NMOS threshold (V_T). The same logic is applied to PMOS transistor in the opposite direction. Thus, when the input voltage is low, the NMOS in Figure 2 is off and no current can flow between its gate and source. At the same time, low input voltage means the VDD is applied to gate of PMOS. Once input is at VDD, PMOS is off and NMOS is on. Now, NMOS acts as a pull-down transistor connecting output to ground. This circuit performs as an inverter, where low input causes high output and vice versa.[2]

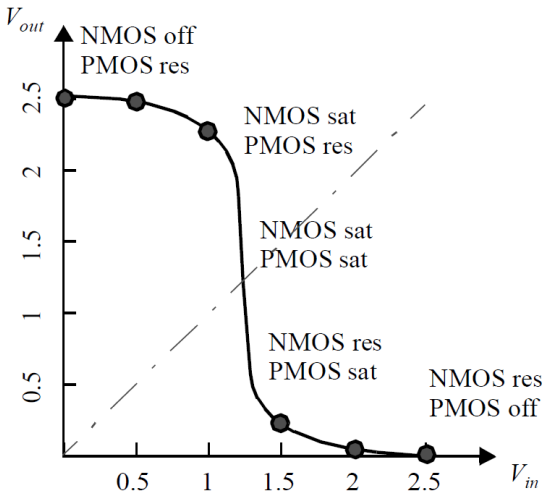

Fig. 1. Inverter circuit voltage transfer output example with CMOS states [1]

C. Noise Margins

The transition state between on and off-state of the inverter, ideally, should be equivalent to a digital clock with vertical states. With noise margins however, the inverter system behaves similarly to the system provided in Figure 1 above. Noise margins determine the range for input signal to be considered low or high (VIH or VIL). Noise margins are considered according to the equations below.

$$NM_H = V_{DD} - V_{IH} \tag{1}$$

$$NM_L = V_{IL} \tag{2}$$

$$V_{IH} = V_M - \frac{V_M}{g} \tag{3}$$

$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g} \tag{4}$$

The input voltage ranges show the indeterminate range between the on and off-states of the inverter which finds the noise margins. The noise margin system shows a ratio of the minimum accepted noise. As the ratio increases, the acceptable noise increases, meaning at a certain voltage and MOSFET state, the system will not change with more noise.

D. Circuit Design

This circuit includes voltage supplies at the gate and source terminals, where, at the gate, the voltage is supplied in parallel, and in series at the source of the PMOS. Because the changing voltage at the gates of the MOSFETs, the characteristics of the CMOS inverter can be displayed at the output graphically between each CMOS device..

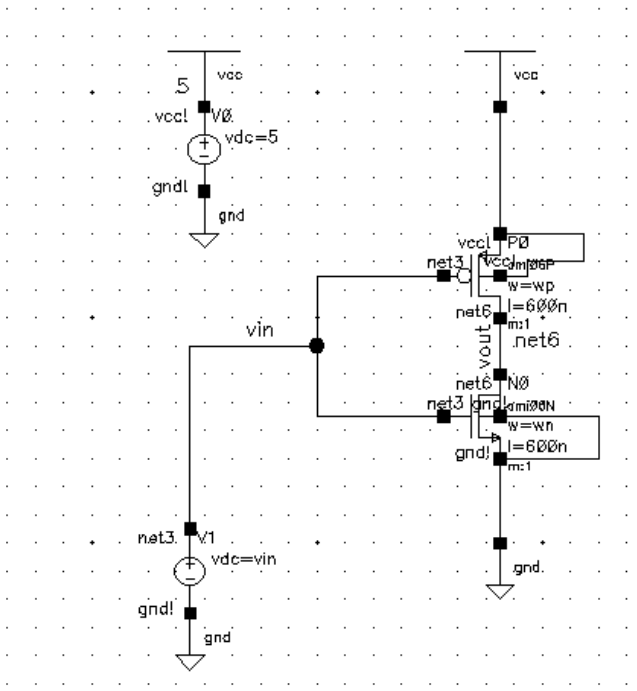

Fig. 2. Inverter circuit designed in Virtuoso Cadence for DC and parametric analysis using a NMOS and PMOS transistor labeled with respective length and width of transistors

III. Procedure

In this experiment, cadence was implemented as a medium to create a DC simulation of a CMOS inverter. Specifically, the CMOS circuit was analyzed to show the voltage transfer curve along with the derivation of the curve's output. Comparing these two results led to a parametric analysis to show the varying VTC curves at a different width of the PMOS transistor from 1.5u - 6u. Each characteristic of the noise margin was then calculated using these curves to determine a final graphical output determining the DC characteristics of the CMOS inverter.

IV. Results and Discussion

A. Presenting Results

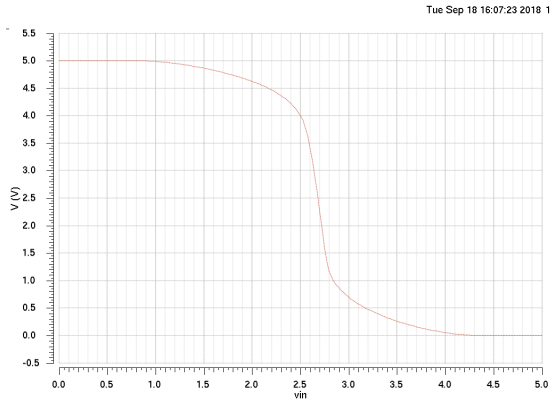

Fig. 3. Output of voltage transfer curve from the CMOS inverter circuit of Figure 2 from a V_{in} of 0 to 5V displaying the switching characteristics of the NMOS and PMOS transistor

The visual output of the circuit design displays the current-voltage characteristics of the CMOS inverter device. As referenced in Figure 1, the transition between inverter states occurs when voltage is applied to the gate. Similarly to the figure referenced, the NMOS starts in an off state as the PMOS is in the on state. As both transistors reach saturation they reach the mid-state of the inverter. As shown in Figure 3, both transistors reach this state and then switch to a point where NMOS turns on as PMOS reaches the off state, reflecting the Figure 1 VTC model.

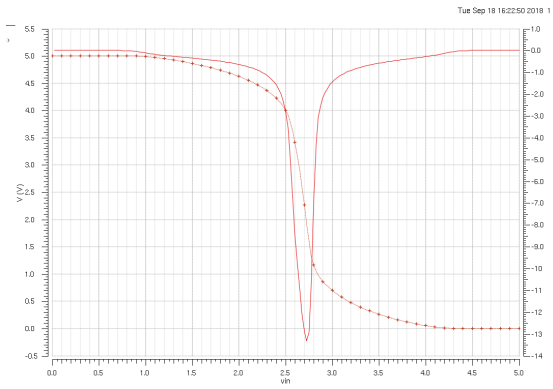

Fig. 4. Output of VTC against the dV_{out} plot from the CMOS inverter circuit of Figure 2 displaying a comparison between the CMOS states and the output of the inverter circuit.

Figure 4 references the derivation of vout (dV_{out}) against the VTC. As shown by the figure, the derivative of V_{out} decreases as the CMOS devices reach saturation and increase as the respective devices switch states. This case displays that, as both CMOS devices reach a mid-way voltage (V_m), the overall output of the device will lose data on the output.

Parametric analysis is shown to analyze the inverter system as the width of the PMOS (w_p) was put in a parametric sweep.

Here, as the width increased, the total input voltage required for the PMOS to switch to the off-state increased. In this case

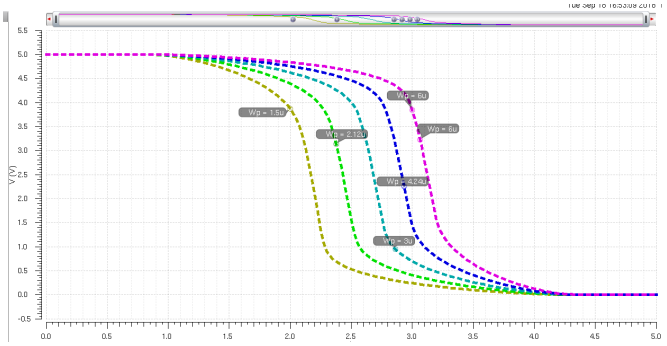

Fig. 5. Output of VTC from the CMOS inverter circuit of Figure 2 as the w_p increased from 1.5u to 6u

This response, shown in Figure 5 entails the property that the width of the transistor is directly proportional to the input voltage required at the respective gate to change the state of the inverter. Similarly, Figure 6 displays a proportional characteristic between the width and derivative of the output voltage. As the transistor width increases, the output derivation increases.

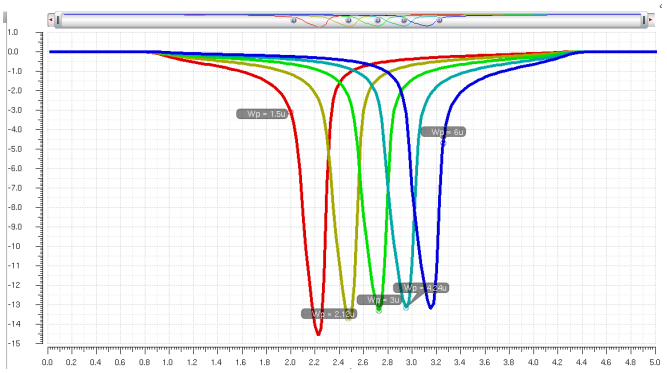

Fig. 6. Output of output voltage derivative (dV_{out}) from the CMOS inverter circuit of Figure 2 as the w_p increased from 1.5u to 6u

Determining the dV_{out} of the circuit can be found by deriving the output given by Figure 5.

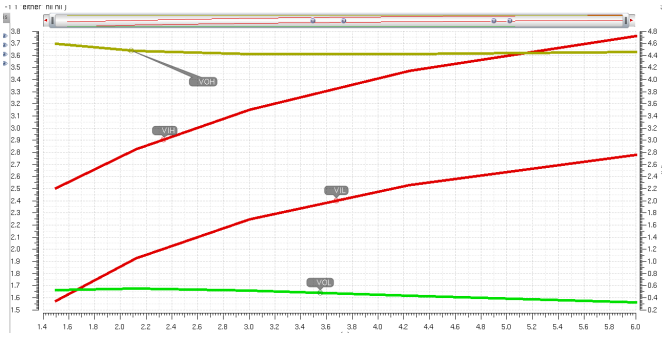

Fig. 7. Output of V_{IH},V_{IL},V_{OH}, and V_{OL} from the CMOS inverter circuit of Figure 2 as the w_p increased from 1.5u to 6u with respect to noise ratio.

V_{OH} and V_{OL} change less drastically with increasing PMOS width. As shown by Figure 7, both characteristics have a more steady slope with a inverse proportional characteristic.

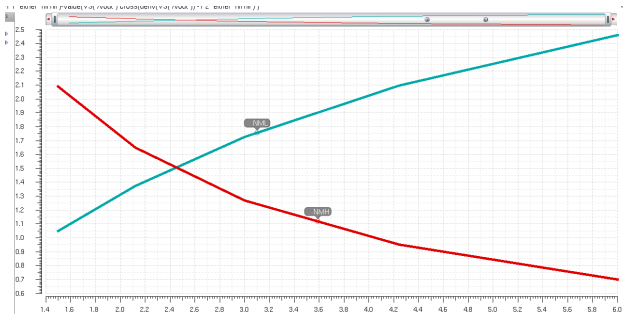

Fig. 8. Output of NM_L and NM_H from the CMOS inverter circuit of Figure 2 as the w_p increased from 1.5u to 6u with respect to noise ratio.

Figure 8 displays the trend with Noise margin high and low, against the width of the PMOS transistor. In this case, NM_H is inversely proportional, where NM_L is directly proportional to the width. Here the noise margin system shows the ratio of the minimum accepted noise. As the ratio increases, the acceptable noise increase or decreases depending on the high or low. This is reflecting the ratio shown in Equation 1-4.

V. Conclusions

The experiment showed the DC characteristics of the inverter circuit through Cadence. This is shown on the plot comparison between the VTC and noise margin characteristics. More specifically, a parametric sweep was used to show the varying inverter specifications when the width of the PMOS transistor increased. This showed trends and relationships between the values in question within each transistor and the inverter circuit as a whole. Such examples include the required increase of input voltage as width increases or noise margins ratio decreasing minimum values when both CMOS devices are in saturation. Summation of all findings can be found in Figure 9 of Appendix B.

References

[1] *Quantification of integrity, performance, and energy metrics of an inverter. Optimization of an inverter design*[Online]. Available: http://bwrcs.eecs.berkeley.edu/Classes/icdesign/chapter5.pdf

[2] *N. Weste and D. Harris, Principles of CMOS VLSI design*. Reading, Mass.: Addison-Wesley Pub. Co., 1993.

APPENDIX

A. Netlist

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// Generated on: Sep 18 16:53:47 2018
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// Design cell name: invx
// Design view name: schematic
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include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: tutorials
// Cell name: invx
// View name: schematic
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         ps=(2 * wn) + (5 * (600n)) pd=(2 * wn) + (5 * (600n)) m=1 \
        region=sat
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         ps=(2 * wp) + (5 * (600n)) pd=(2 * wp) + (5 * (600n)) m=1 \
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V0 (vcc! 0) vsource type=dc dc=5
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element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
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saveOptions options save=allpub
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B. CMOS Inverter VTC, Derivative of Vout, VIH/VOH, and NML/NMH

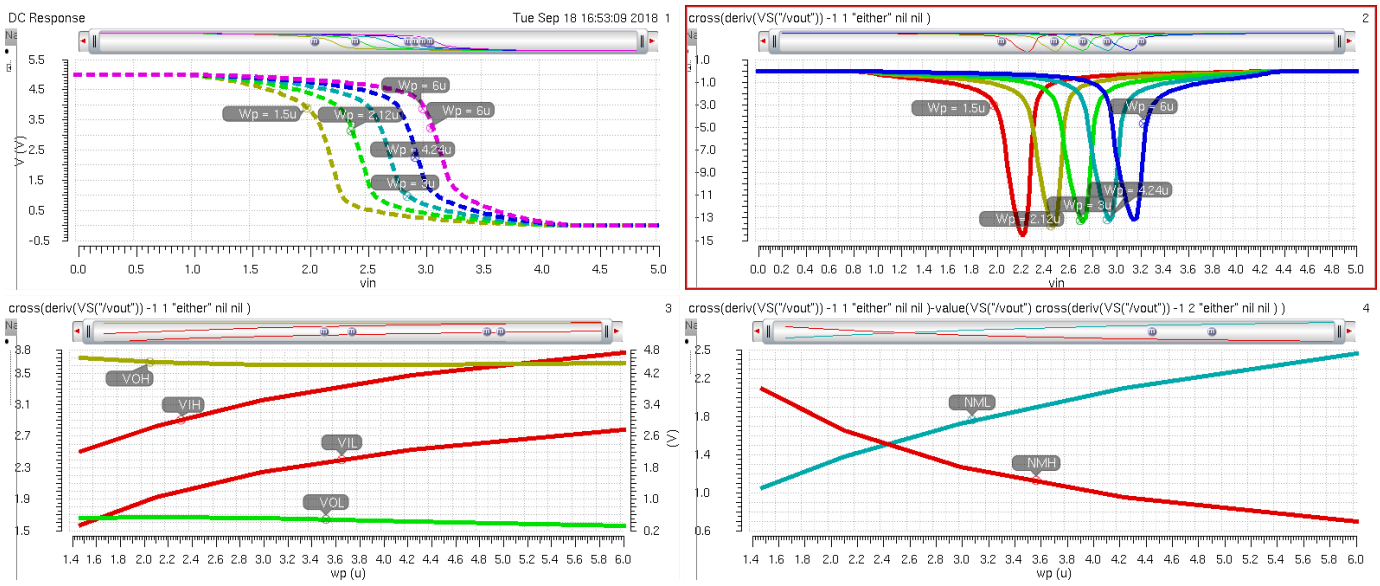

Fig. 9. Output of VTC, voltage derivative output, noise margin plot, voltage input and output, and Noise Margin High and Low plot from the CMOS inverter circuit of Figure 2 based on the varying width of the system