Layout and Design Rule Check

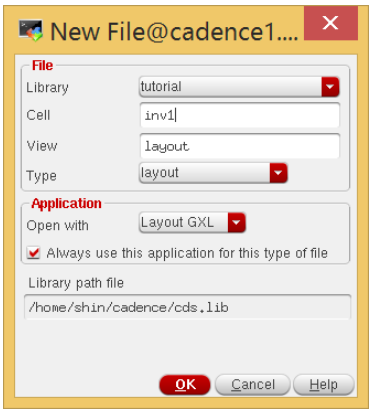
During the last labs you created a schematic view for the inverter and verified that it functions as an inverter. In this Lab we are going to create a layout view of the inverter schematic. Before getting start with your layout, you may want to review on the CMOS chip fabrication process and layout (textbook Chapters 1&3), particularly for the cross-sectional view of an inverter. Having cross-sectional views in mind helps understand layout design rules and do better layout. Objectives of this lab are to:

- Get to know how to create/edit a layout
- Understand layout design rules
- How to engage a stick diagram with its physical layout
- Experience with physical layout and Design Rule Check (DRC)

For layout we are going to use the MOSIS's SCMOS_SUBM scalable CMOS design rules for submicron processes. Please refer the MOSIS web page for design rules of AMI C5N process at https://www.mosis.com/pages/Technical/Layermaps/lm-scmos_scn3m.html, and more details about the SCMOS design rules at https://www.mosis.com/files/scmos/scmos.pdf.
The AMI C5N process we're going for our labs uses λ of 0.3um which is the half pitch of 0.6um. With the λ-based design rule, all the dimensions or sizes in the design need to be integer multiples of 0.5λ (=0.15um) which is the grid unit of layout.

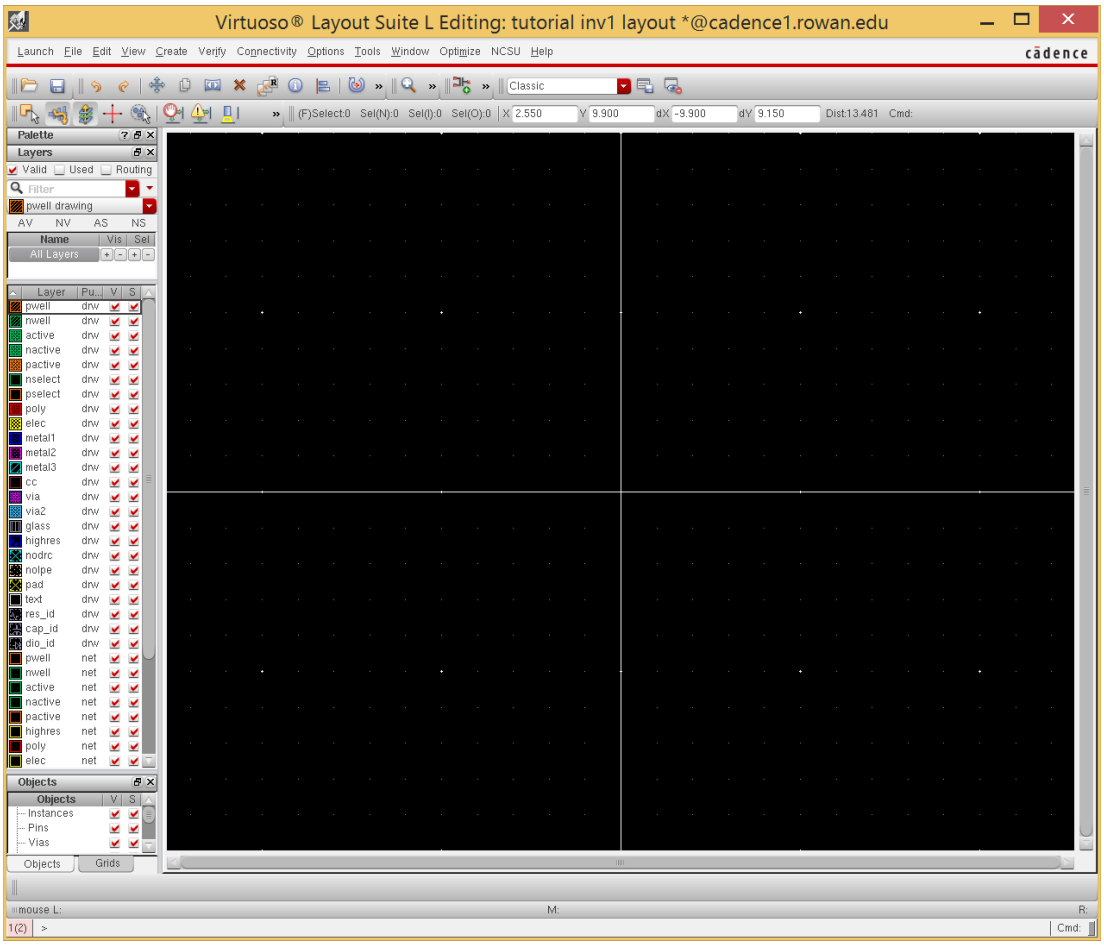
1) **Schematic View** of an inverter:
   a. You should have a verified functional schematic before beginning layout, then the layout will have the exactly same pin names and the transistors with the same sizes as in the schematic. Check your inverter schematic, ***inv1*** from the last lab, and make sure that the transistor sizes are expressed both in microns and in grid units (0.5λ). Set the lengths of both pMOS and nMOS to 0.6um (2λ, or 4 grid units), and the width of the nMOS to 1.5um (5λ, or 10 units) and that of the pMOS to 3um (10λ, or 20 units).
      Check and Save and make sure there is no error or warning.
   b. Plan on your layout!
      From the schematic diagram, you should have a strategy how you deploy the transistors and how you route and assign pins. Drawing a stick diagram will help you prepared. You will need to use a pencil and paper and make a simple sketch of the layout, to decide the position and orientation of all transistors, the orientation and layer of supply lines, the position and layer of the input and output pins, etc.

2) **Create a Layout View** of an inverter:
   a. **Create a new layout view**: From the **Library Manager**, select your inverter cell under your work library, and choose *File->New->Cell View...*. (You can do the same thing simply by typing "**layout**" under View section of the ***inv1*** cell, from the Library Manager.) Since we are going to create a layout view of the inverter, select ***layout*** for the *Type* and **Layout GXL** for *Open with*. Check for the check box and then click **OK**.



You should get two windows pop up, one for the schematic view and the other one for the blank layout view. The **Virtuoso** is the main design suite, where the **L**ayer **S**election **W**indow (**LSW**) is on the left and it lets the user select different layers of the mask layout. Main layout window will always use the layer selected in the **LSW** for viewing and/or editing. The **LSW** can also be used to determine which layers will be visible and which layers will be selectable.

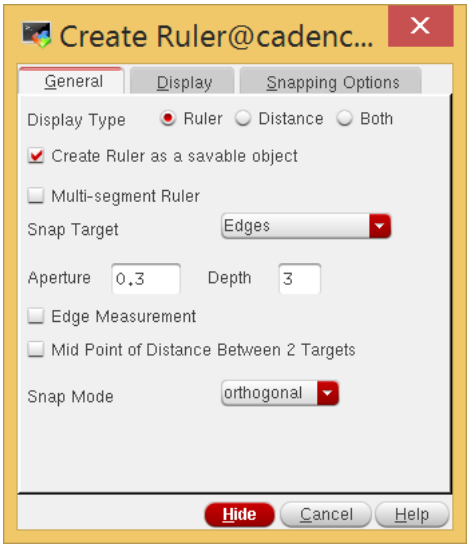
To select a layer, simply click on the desired layer within the LSW. Virtuoso is the main layout editor of Cadence design tools. Commonly used functions can be accessed by pressing the buttons/icons of the toolbar on the top of this window. There is an information line at the top of the window which shows (from left to right) number of selected objects, the X and Y coordinates of the cursor, the distance traveled in the X and Y directions, the total distance, and the command currently in use. This information can be very handy while editing. At the bottom of the window, another line shows the function of each mouse button. Note that the mouse button functions will change according to the command you are currently executing. The default mouse mode is selection, and as long as you do not choose a new mode you will remain in that mode. To quit from any mode or command and return to the default selection mode, the '**ESC**' key can be used.



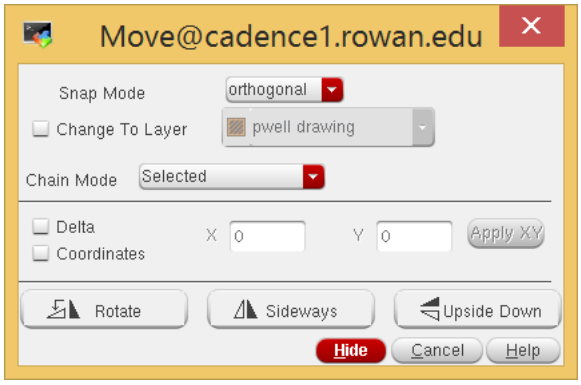
Useful Editing Tools

(i) **Ruler**: The ruler is very useful to place objects and measure the distance between the objects.

- To start the ruler, from the **toolbar**, select *Tools -> Create Ruler* (hotkey '**k**').
- Click the start and end point in the window; a ruler is created showing the distance between the two points.
- Hit the 'ESC' key to exit the ruler command.
- To remove all ruler markers on your layout, press '**Shift+K**'.

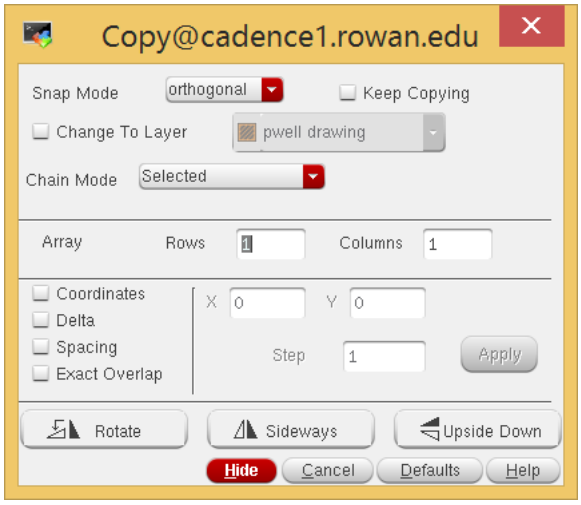


(ii) **Move**: If you place the objects on the wrong place, you can use move function to adjust the location of the object.



- To get into the ***move*** mode, select *Edit -> Move* (or using its hotkey '**m**'). Then, a window will pop-up.
- The *Snap Mode* is an interesting option. When this is in orthogonal setting, the copied objects will move only along one axis. This is a good feature to help you avoid alignment problems.
- When you have finished the move operation, hit the 'ESC' key to exit the move command.

(iii) **Copy**: If you want to create the same object repeatedly, you can use the copy function.



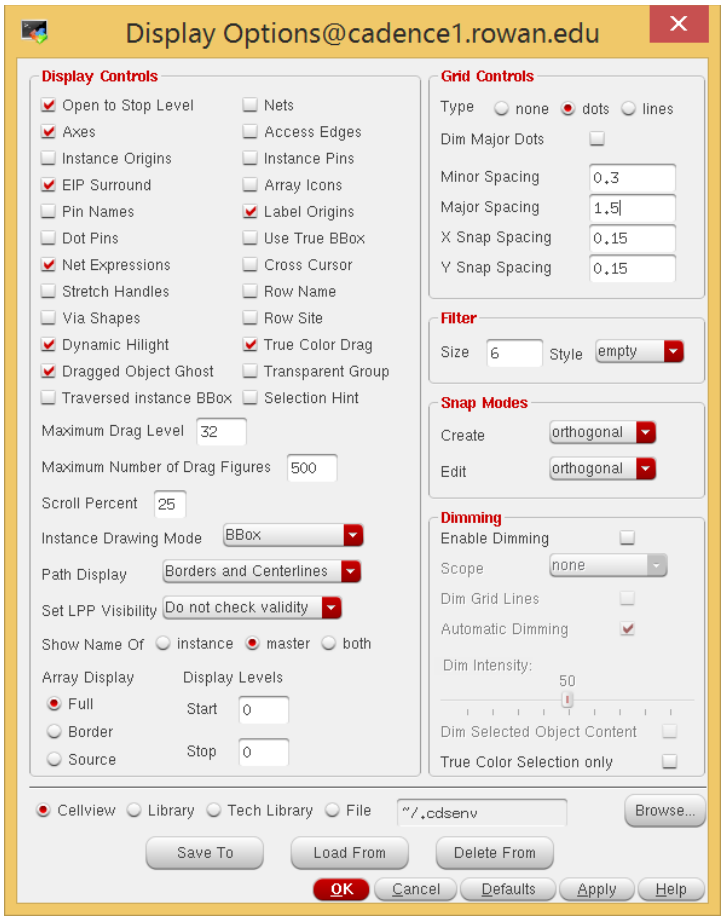
- To get into the ***copy*** mode, select *Edit -> Copy* (or using its hotkey '**c**'), and the copy dialog box will pop-up.
- Click in an object. Notice that an outline of the object will attach to your mouse cursor. Move your mouse and click when you get to the location to place a copy of the object.

(iv) **Delete:** To delete an object you have drawn, click on the object to select it, then press the *Delete* key on the keyboard.

(v) **Undo**: When you make a mistake (accidentally delete a component, etc.), you can undo the action by click on the Undo icon in the toolbar (or using its hotkey '**u**').

b. **Display Setup**: Before starting layout, you should always check the grid properties. From the **Layout Editing** window, select *Options -> Display* (or type its hotkey '**e**') to bring up the **Display Options** window. Type in the following settings, then click **OK**.

- Minor Spacing **0.3** (=1λ)
- Major Spacing **1.5** (=5λ)
- X Snap Spacing **0.15** (=0.5λ)
- Y Snap Spacing **0.15** (=0.5λ)



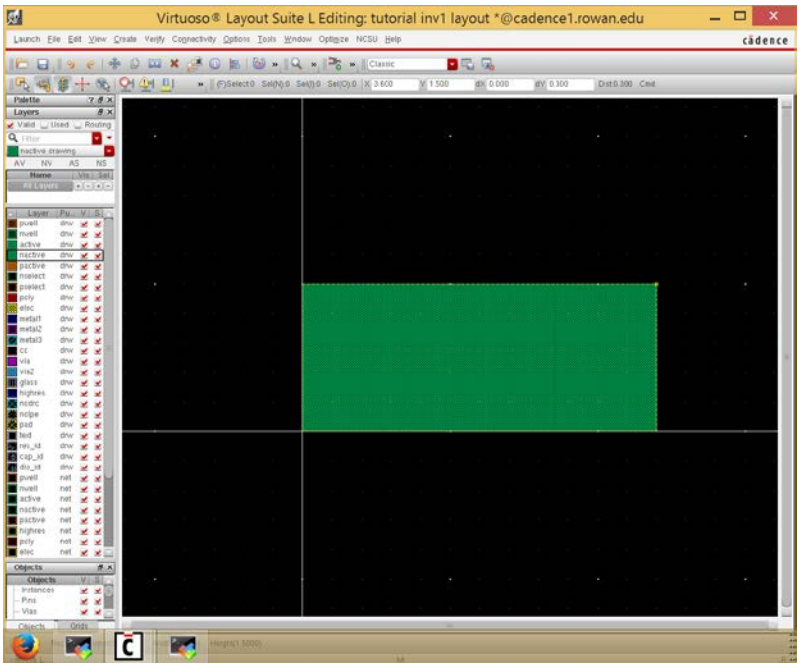
c. Creating an nMOS active layer

Let us consider the following layout strategy, for an example:

- All Metal 1 lines will be in minimum width (3λ=0.9um, or 6 grid units), except for vdd and gnd which will be 6λ wide (=1.8um).
- Horizontal supply rails with vdd rail on top and gnd rail at bottom, both in Metal 1
- Pins IN on the left and OUT on the right, all in Metal 1
- The two transistors will be aligned vertically horizontally.
- The layout will be made as compact as possible (i.e. use minimum distances as allowed by DRC wherever possible).

The first step of drawings can be for nMOS active layer. Normally the pMOS transistors are at the top near the vdd rail and the nMOS transistors are at the bottom of the layout near the gnd rail. From the schematic we know that the nMOS transistor has a channel width of 1.5um. The width of the transistor (W) will correspond to the width of the active area. We want to draw a horizontal transistor so the channel width will be measured top-to-bottom of the active layer (Y-dimension of the information bar).

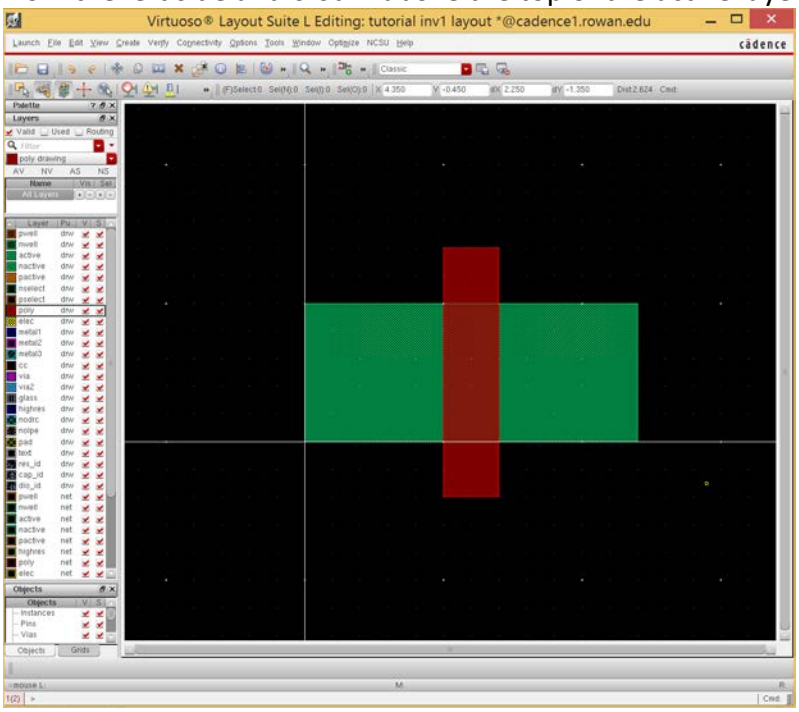
- From the **LSW**, select **nactive layer**.
- In the **Layout Editor**, select Create -> Rectangle (or its hotkey '**r**')
- Draw a rectangle that is 3.6um x 1.5um.



d. <u>Creating the Gate Poly</u>

We will use a vertical polysilicon rectangle to create the gate of the nMOS transistor. Note that the length of the transistor channel (L) will be determined by the width of this poly rectangle.

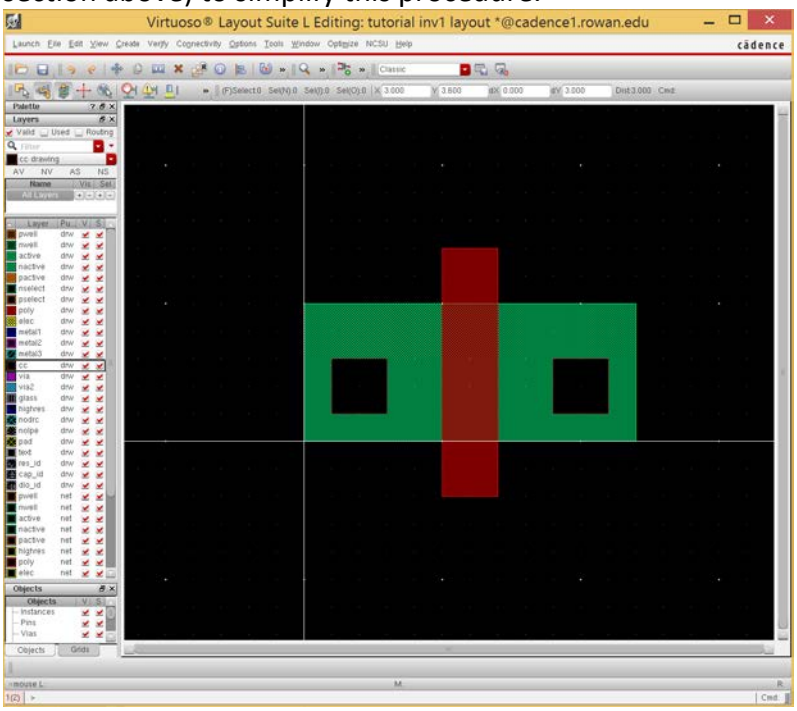
- Select ***poly*** layer from the **LSW**.
- In the **Layout Editor**, draw poly rectangle that is 0.6um x 2.7um over the center of the nactive as shown in the figure below. Start drawing the poly rectangle 1.5um from the left side and 0.6um above the top of the active layer.



e. <u>Active Contacts</u>

Contacts provide electrical connections between the Metal-1 layer and the Active layer, which in this case is the drain and source regions of the nMOS transistor.

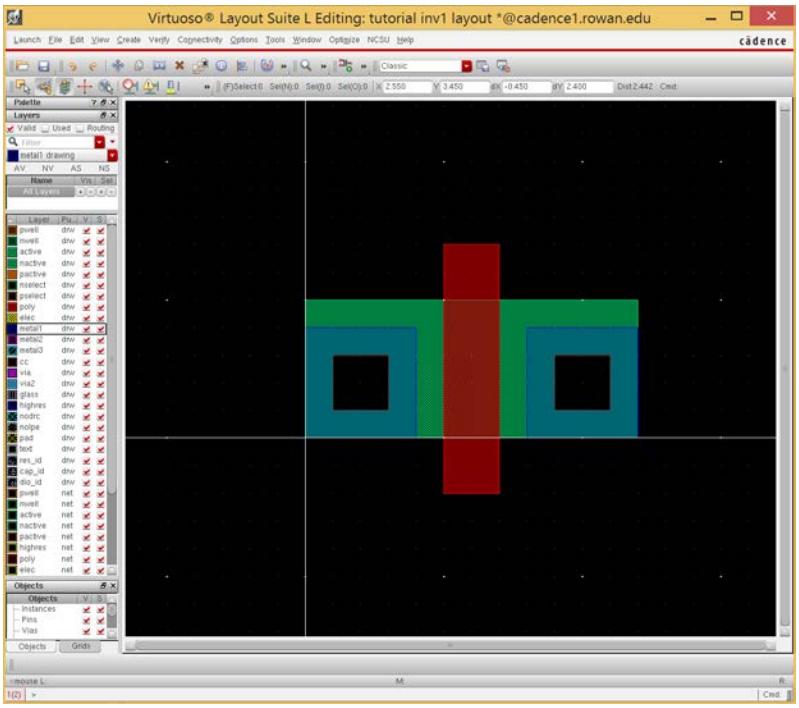
- Select the ***cc*** layer from the **LSW**.
- In the Layout Edior, draw a rectangular box that is 0.6x 0.6 um within the active area. Start drawing the contact at 0.3um away from the bottom-left corner of the nactive layer.
- Draw the second contact on the right side of the nactive layer as shown below. As set by the Design Rules, the contacts must be at least 0.3um from the edge of the active layer. You might want to use the Copy command (see Useful Editing Tools section above) to simplify this procedure.



f. <u>Covering Contacts with Metal-1</u>

The Active Contact layer defines where a via hole will be formed in the oxide that separates the active region from the Metal-1 layer. To complete the contact, we must ALWAYS cover the contact with a Metal-1 layer.

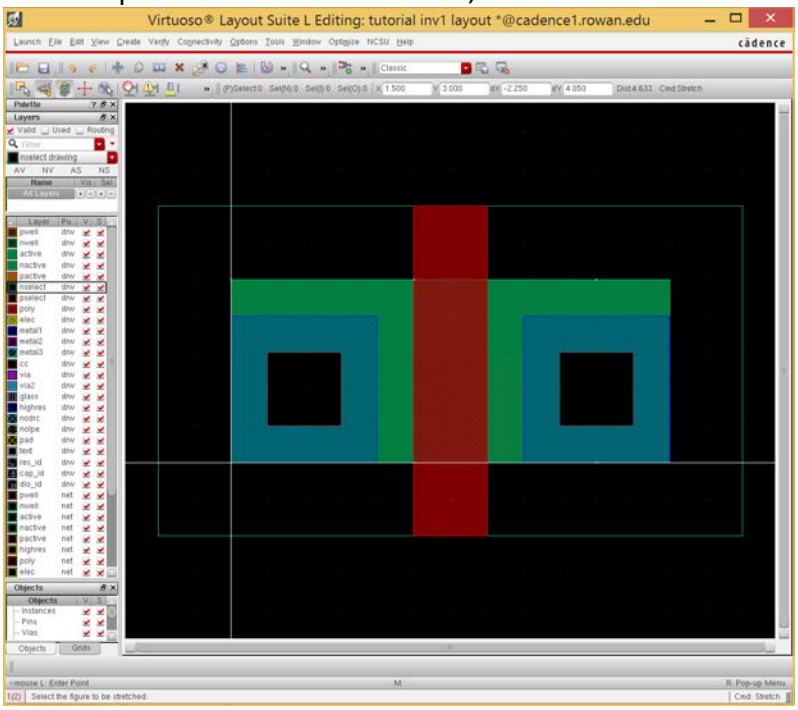
- Select layer **Metal-1** from the **LSW**.
- In the **Layout Editor**, draw a 1.2um square to cover each contact. (From the Design Rules, the Metal-1 layer must extend the contacts by at least 0.3um which is 1λ.)



g. <u>Create N-Select Layer</u>

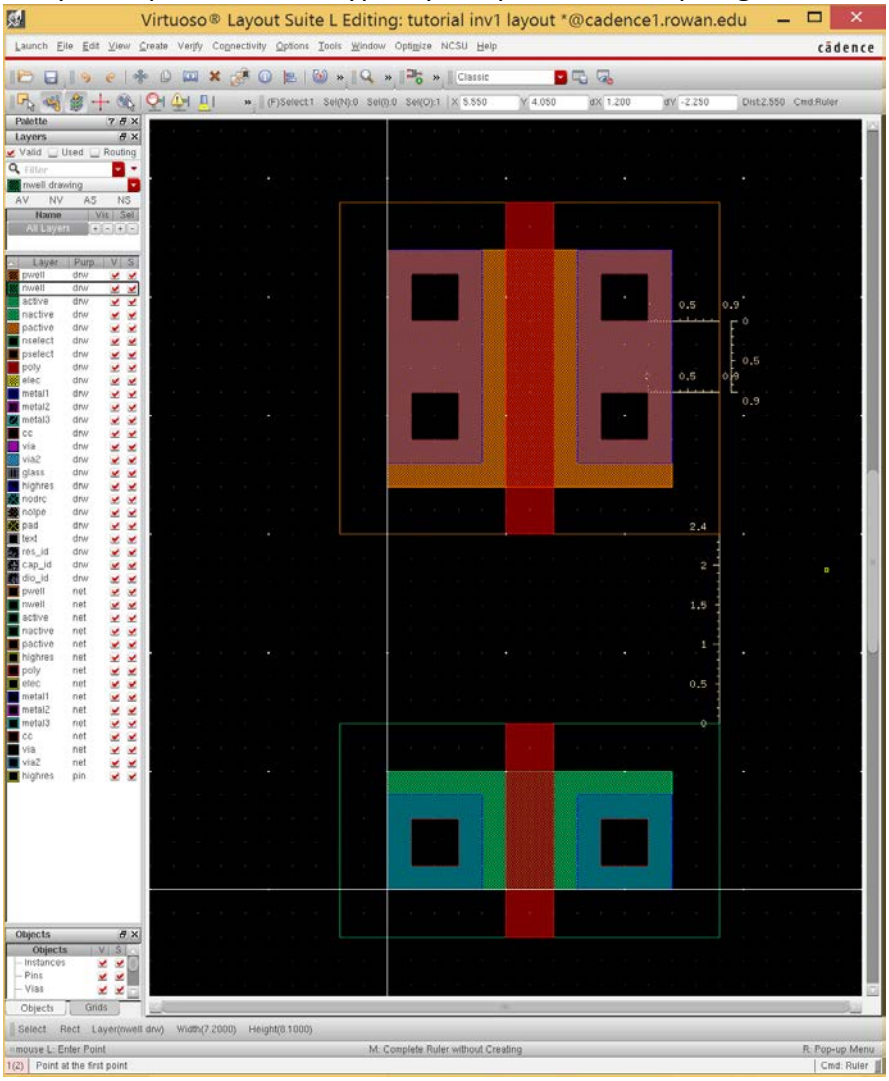
Each diffusion (active) area must be specified as being of n-type or p-type. This is accomplished by a defining layer of n-select (or p-select) around each n-type (or p-type) transistor. Since we are making an nMOS now, we will choose the nselect layer.

- Select **nselect** layer from the **LSW**.
- Draw a rectangle extending over the active area by 0.6um (=2λ) in all directions. This completes the nMOS transistor, which should look like the following.



h. Drawing pMOS

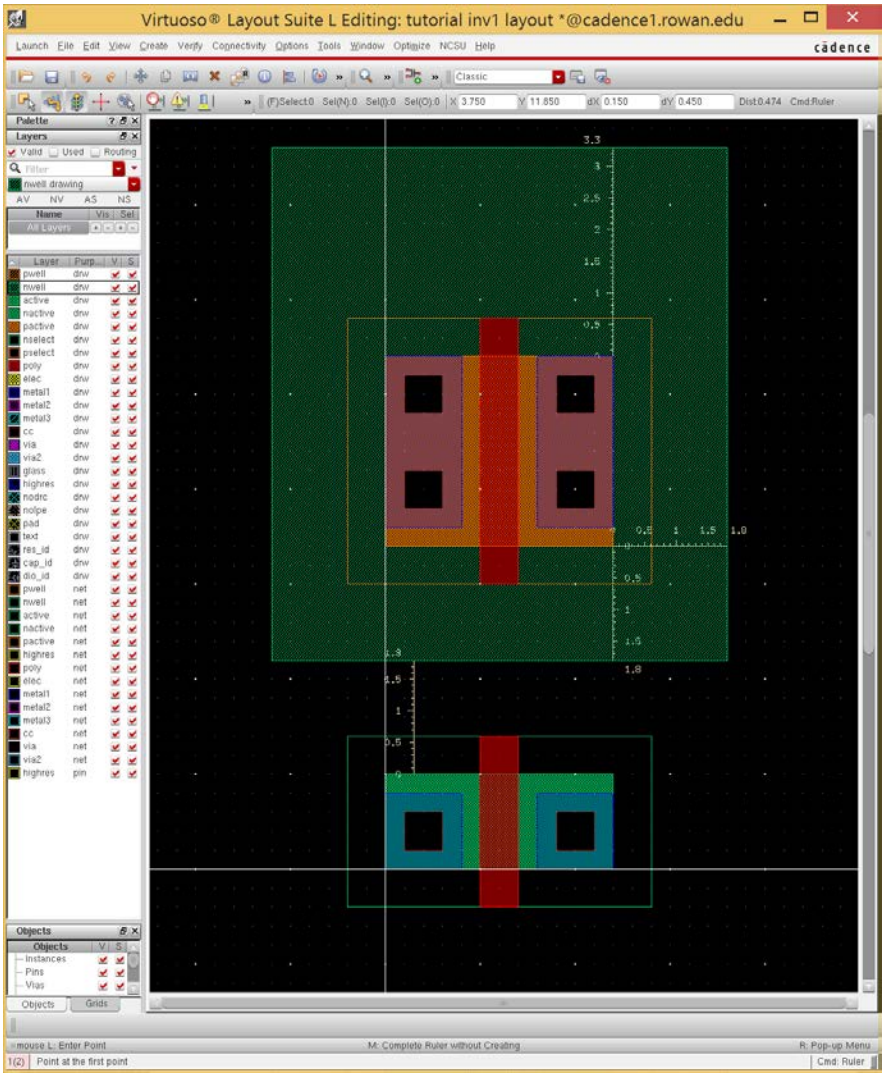
Repeat steps ***c*** through ***g*** to make a pMOS transistor at the top of your cell. The only difference between drawing nMOS and pMOS is that you will be using **pactive** and **pselect** layers in place of the n-type layers specified in steps ***c-g***.



i. Drawing N-WELL

The selected process, AMI C5N, uses a p-type substrate, where nMOS transistors can be formed, and requires an n-well, where pMOS transistors can be formed. We must add an n-well to our cell to form an local n-type substrate (body terminal) for pMOS transistors.

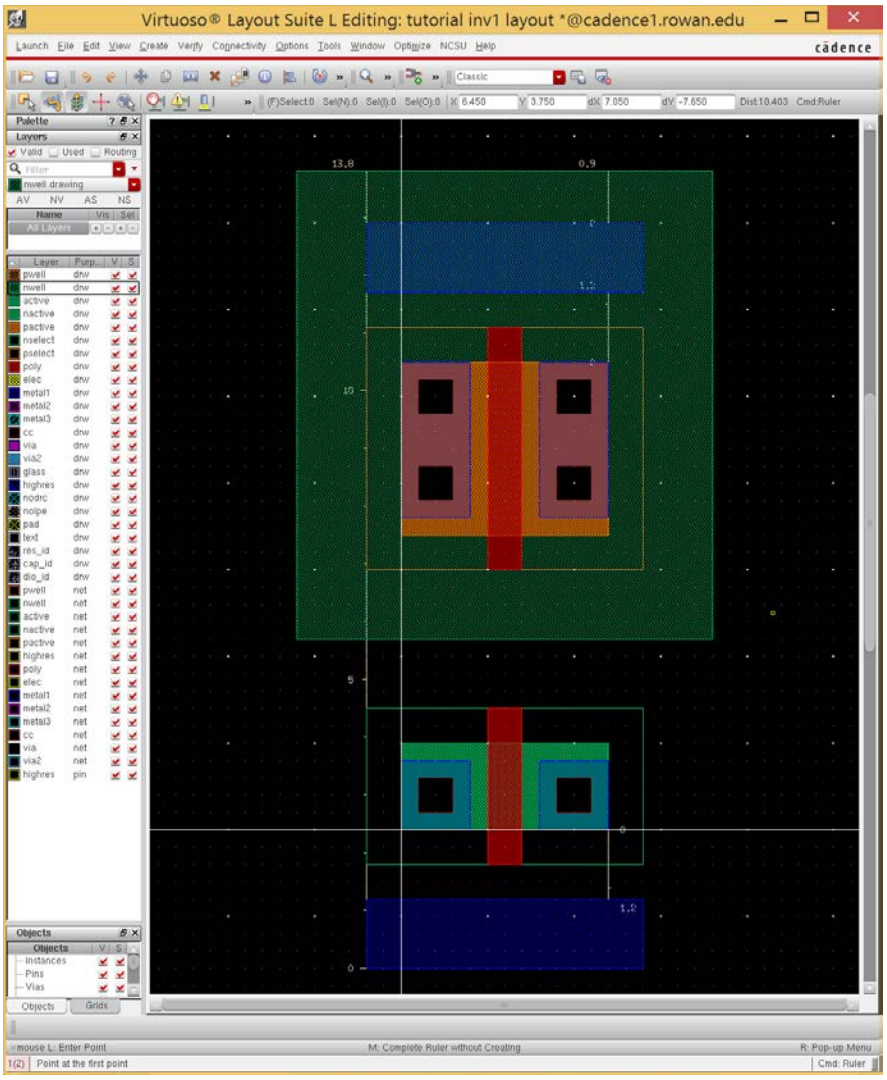
- Select the **nwell** layer from the **LSW**.
- Draw a large n-well rectangle around the **pactive** area. The n-well must extend over the pMOS active area by a large margin, at least **1.8um** (=6λ).



j. Creating Supply Rails (vdd & gnd)

Usually a circuit will consist of a large number of cells, all of which need power and ground connections. Therefore it is common to design cells with the same spacing between the power and ground so that they can easily be connected together when the cells are placed side by side. This vertical spacing is called the **cell pitch** and it is generally standardized for all cells in the same library to facilitate combining cells in higher-level circuits. For this lab, however, we will make the supply rails with 1.2um in width (=4λ) using the Metal- 1 layer and with the minimum pitch available (height from bottom of the gnd rail to top of the vdd rail).

- Select **metal1** layer from the **LSW**.
- In the **Layout Editor**, click *Create -> Rectangle* (or use it hotkey '**r**').
- Place the gnd rail below the nMOS and vdd rail on top of the pMOS.

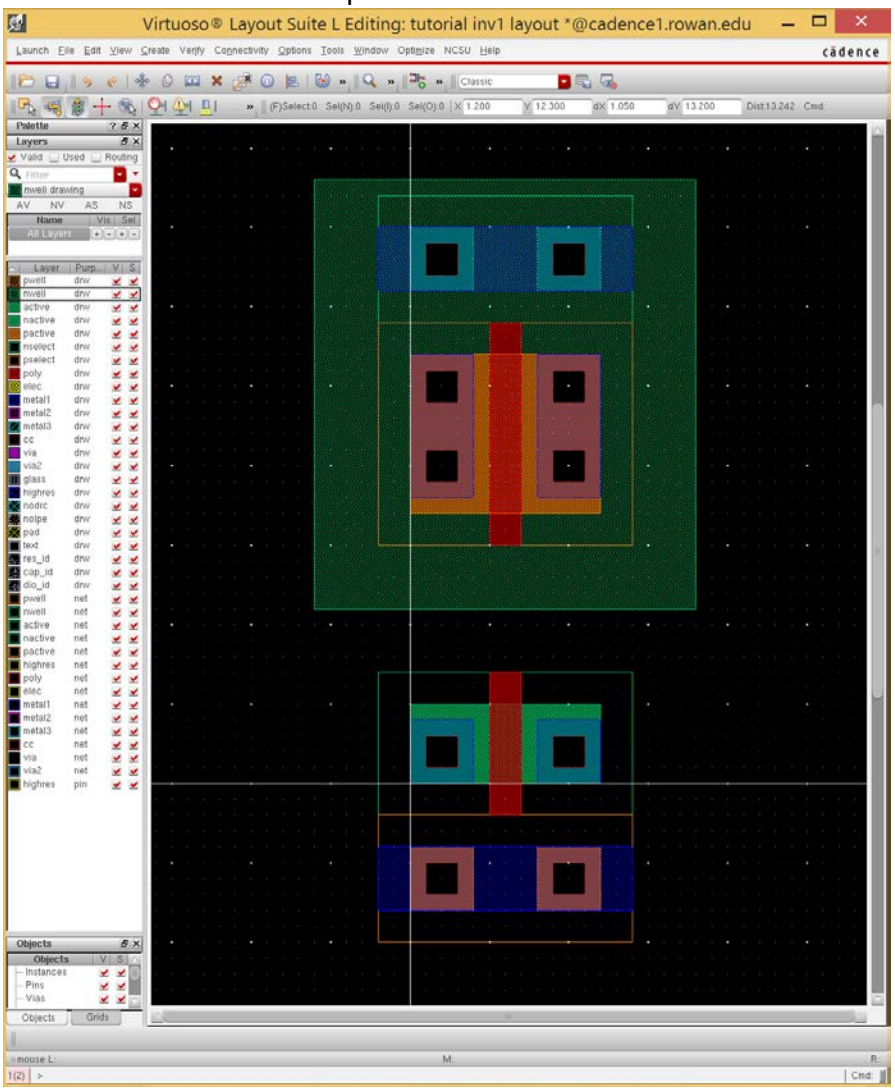


k. <u>Creating substrate/well contacts</u>

The body terminals of the nMOS and pMOS transistors are the substrate and n-well, respectively. These terminals must be tied to the proper supply rail, substrate to gnd and n-well to vdd. To simplify this connection, we can place Active Contacts directly on the existing supply rails. This will require adding active, contact, and select layers on top of the existing metal-1 layer.

- Select the **pactive** layer from the **LSW**
- Draw a 1.2um x 1.2um square placed in the center of the GND rail directly beneath the Active contact on the nMOS transistor. Repeat to add a contact beneath the second nMOS active contact.
- Select the **cc** layer from the **LSW**, and place 0.6um x 0.6um **contacts** inside the **pactive** squares.
- Select **pselect** layer from the **LSW**, and draw a box extending over both pactive squares by 0.6um on each side.

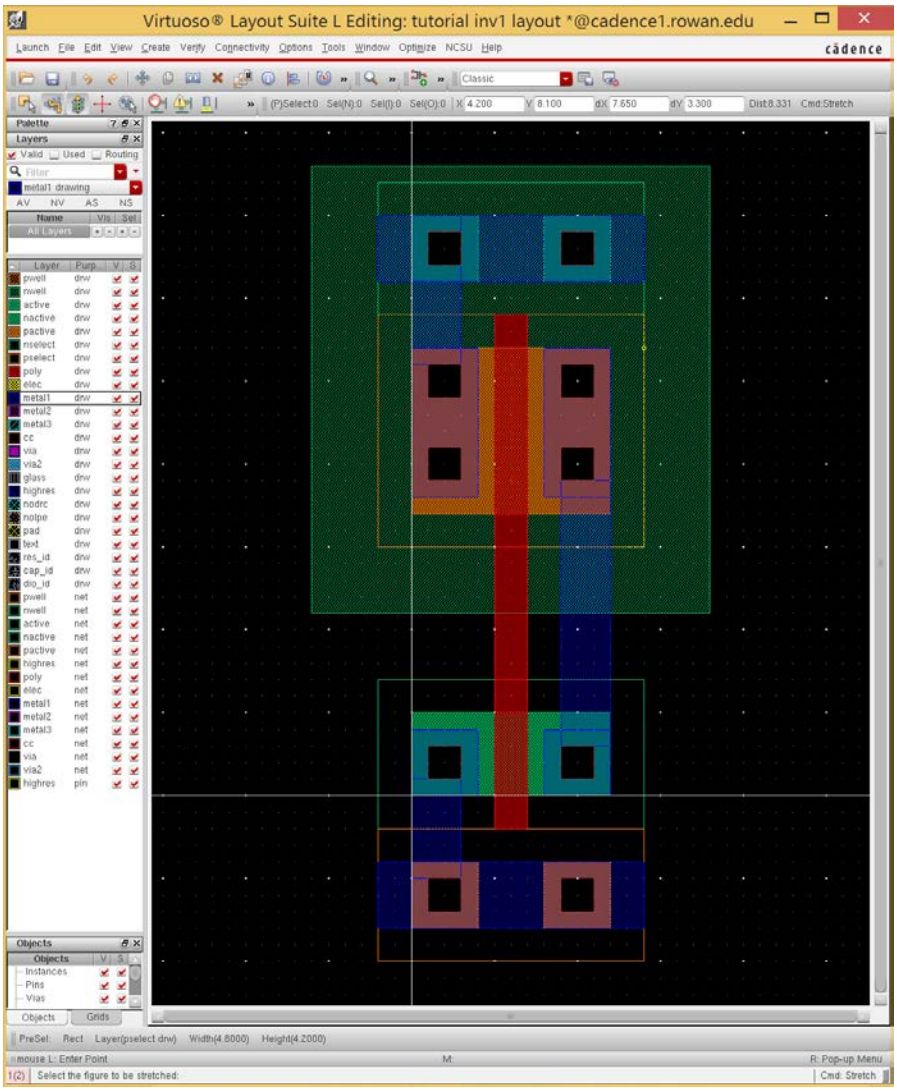
- Repeat this process using complementary layers (**nactive**, **nselect**) to add n-type active contacts to the vdd power rail.



I. Connect Transistor Nodes

Now we are to connect all the transistor nodes for the layout to be matched the inverter schematic.

- Select **poly** layer from the **LSW**.
- Draw a rectangle to connect the poly gate inputs of nMOS and pMOS transistors. **Note**: To connect polygons of the same layer (eg., poly) you simply need to add another polygon that makes contact to each of the original layers. If the layers touch or overlap, they will form a continuous shape for fabrication.
- Select layer **Metal-1** from the **LSW**.
- Draw rectangles to connect the source of the nMOS (pMOS) to gmd (vdd) rail.
- Draw a rectangle to connect the drains of the nMOS and pMOS transistors together. This is the inverter output node.

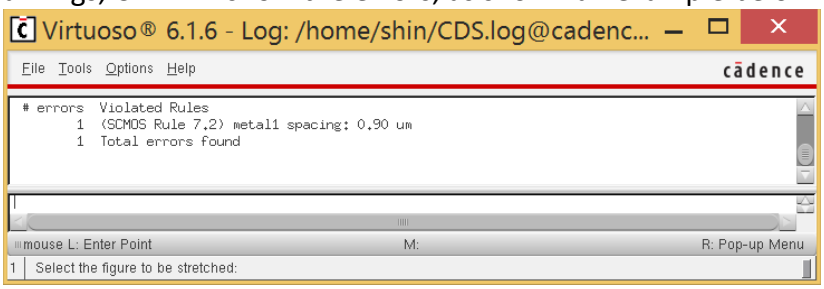


3) **Design Rule Checking**

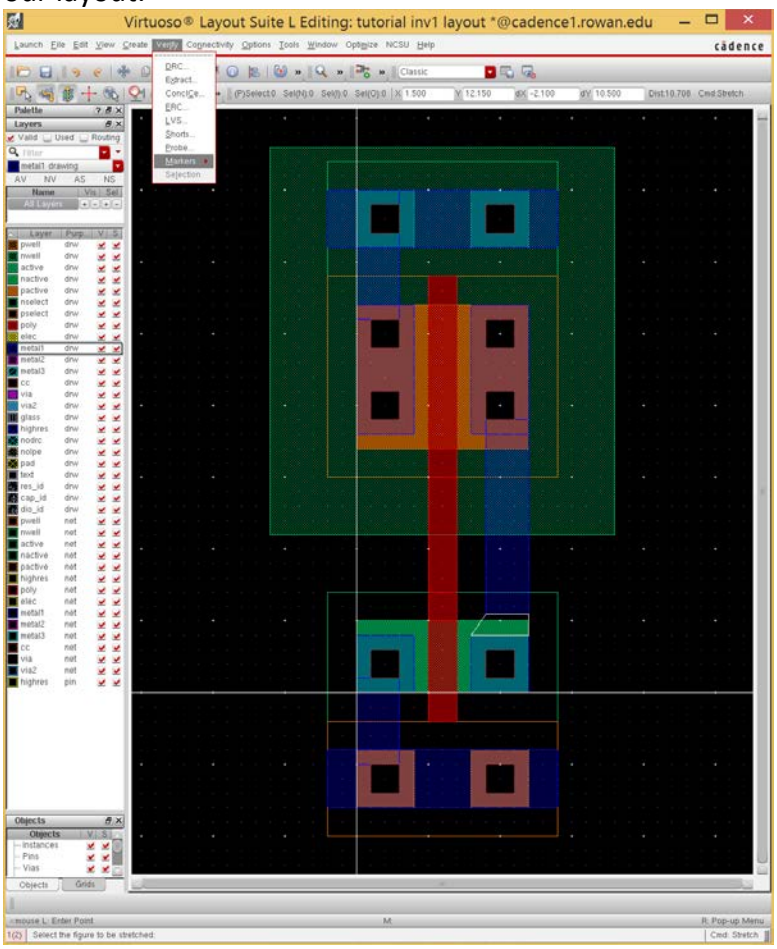
Layout must be drawn according to strict design rules. While you're working on the layout, you will like to check as frequently as possible if your drawing satisfies the design rule. Also after you have finished your layout, you should do check your drawing against the design rules. An automatic program called DRC (Design Rule Check) will check each and every polygon in your design against these design rules.

Select ***Verity->DRC***, from the **Layout Editor**, then the DRC options window will be pop up. The default options for the DRC are adequate for most situations. If okay with the settings, click OK to start DRC. DRC results and progress will be displayed in the CIW (Command Interpreter Window) .

If all the drawings are compliant to the design rules, CIW will display no error. If there are errors or warnings, CIW will show the errors, as shown an example below:



You can locate the error in your layout by selecting Verify->Markers->Find, or get explanation of the error by selecting Verify->Markers->Explain and then clicking on the error marker being highlighted on the layout. Correcting all the errors and warnings will complete your layout.



4) **Activity**

Design a layout of 2-input NAND gate and 2-input NOR gate, with transistor sizes chosen to have the same effective resistances as the designed inverter.

Follow the same strategy used in this lab, and report with layout diagrams and DRC results.