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1 "C:\Users\GOURAV ANIRUDH B J\AppData\Local\Microsoft\WindowsApps\python3.11.exe" "C:\Users\GOURAV ANIRUDH B J\Desktop\Gourav IIITB\CA project\processor.py"
2 START:
3
4
5 CLOCK CYCLE= 1
6
7 Entering fetch stage:
8 Instruction fetched =
00100100000100000000000000000000
9 PC updated to
10 PC = 0000000010000000000000000000100
11 Fetch stage completed
12
13 Entering Decode stage
14 Opcode=001001
15 Instruction is decoded as add type instruction(addi or addiu)
16 RS=00000
17 RT=10000
18 Immediate value=0
19
20 Setting all control Signals
21 Alusrc:1
22 Zero_flag:0
23 MemWr:0
24 MemRd:0
25 Mem2Reg:0
26 jump:0
27 branch:0
28 branch_ne:0
29 PCsrc0
30 lui:0
31 Decode stage completed
32
33 Entering Execute stage
34 ALU_ctrl lines: 0 0 1 0
35 Sign extended value:00000000000000000000000000000000
36 ALU operands:
37 Operand1=0
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38 Operand2=0
39 ALU ADD operation is performed
40 Execute stage completed
41
42 Entering Memory access stage
43 Mem2Reg=0
44 Value from ALU is passed to write port of register
  file
45 Memory access stage completed
46
47 Entering writeback stage
48 RegWr=1
49 Register file is being written back
50 Writing back to register number :16
51 Value written back to register= 0
52 Writeback stage completed
53
54
55
56 CLOCK CYCLE= 2
57
58 Entering fetch stage:
59 Instruction fetched =
  00111100000000010001000000000001
60 PC updated to
61 PC = 000000001000000000000000000000001000
62 Fetch stage completed
63
64 Entering Decode stage
65 Opcode=001111
66 Instruction is decoded as lui
67 RS=00000
68 RT=00001
69 Immediate value=4097
70
71 Setting all control Signals
72 Alusrc:1
73 Zero_flag:0
74 MemWr:0
75 MemRd:0
76 Mem2Reg:0
```

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77 jump:0
78 branch:0
79 branch_ne:0
80 PCsrc0
81 lui:1
82 Decode stage completed
83
84 Entering Execute stage
85 ALU_ctrl lines: 0 0 0 0
86 LUI instruction executed
87 Execute stage completed
88
89 Entering Memory access stage
90 Mem2Reg=0
91 Value from ALU is passed to write port of register
file
92 Memory access stage completed
93
94 Entering writeback stage
95 RegWr=1
96 Register file is being written back
97 Writing back to register number :1
98 Value written back to register= 268500992
99 Writeback stage completed
100
101
102
103 CLOCK CYCLE= 3
104
105 Entering fetch stage:
106 Instruction fetched =
10001100001100010000000000000000
107 PC updated to
108 PC = 0000000010000000000000001100
109 Fetch stage completed
110
111 Entering Decode stage
112 Opcode=100011
113 Instruction is decoded as LW
114 RS=00001
115 RT=10001
```

```
116 Immediate value=0
117
118 Setting all control Signals
119 Alusrc:1
120 Zero_flag:0
121 MemWr:0
122 MemRd:1
123 Mem2Reg:1
124 jump:0
125 branch:0
126 branch_ne:0
127 PCsrc0
128 lui:0
129 Decode stage completed
130
131 Entering Execute stage
132 ALU_ctrl lines: 0 0 1 0
133 Sign extended value:00000000000000000000000000000000
134 ALU operands:
135 Operand1=268500992
136 Operand2=0
137 ALU ADD operation is performed
138 Execute stage completed
139
140 Entering Memory access stage
141 MemRd=1
142 Data Memory is being Read
143 Value read from the memory=7
144 Mem2Reg=1
145 Value from Memory is passed to write port of
register file
146 Memory access stage completed
147
148 Entering writeback stage
149 RegWr=1
150 Register file is being written back
151 Writing back to register number :17
152 Value written back to register= 7
153 Writeback stage completed
154
155
```

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156
157 CLOCK CYCLE= 4
158
159 Entering fetch stage:
160 Instruction fetched =
    0010000000000010000000000000001
161 PC updated to
162 PC = 00000000100000000000000010000
163 Fetch stage completed
164
165 Entering Decode stage
166 Opcode=001000
167 Instruction is decoded as add type instruction(addi
    or addiu)
168 RS=00000
169 RT=00001
170 Immediate value=1
171
172 Setting all control Signals
173 Alusrc:1
174 Zero_flag:0
175 MemWr:0
176 MemRd:0
177 Mem2Reg:0
178 jump:0
179 branch:0
180 branch_ne:0
181 PCsrc0
182 lui:0
183 Decode stage completed
184
185 Entering Execute stage
186 ALU_ctrl lines: 0 0 1 0
187 Sign extended value:00000000000000000000000000000001
188 ALU operands:
189 Operand1=0
190 Operand2=1
191 ALU ADD operation is performed
192 Execute stage completed
193
194 Entering Memory access stage
```

```
195 Mem2Reg=0
196 Value from ALU is passed to write port of register
    file
197 Memory access stage completed
198
199 Entering writeback stage
200 RegWr=1
201 Register file is being written back
202 Writing back to register number :1
203 Value written back to register= 1
204 Writeback stage completed
205
206
207
208 CLOCK CYCLE= 5
209
210 Entering fetch stage:
211 Instruction fetched =
    00000010001000011001000000100010
212 PC updated to
213 PC = 00000000100000000000000010100
214 Fetch stage completed
215
216 Entering Decode stage
217 Opcode=000000
218 Instruction is decoded as R format
219 RS=10001
220 RT=00001
221 RD=10010
222 Function field=100010
223 Shift amount=00000
224
225 Setting all control Signals
226 Alusrc:0
227 Zero_flag:0
228 MemWr:0
229 MemRd:0
230 Mem2Reg:0
231 jump:0
232 branch:0
233 branch_ne:0
```

```
234 PCsrc0
235 lui:0
236 Decode stage completed
237
238 Entering Execute stage
239 ALU_ctrl lines: 0 1 1 0
240 ALU operands:
241 Operand1=7
242 Operand2=1
243 ALU SUBTRACT operation is performed
244 Execute stage completed
245
246 Entering Memory access stage
247 Mem2Reg=0
248 Value from ALU is passed to write port of register
file
249 Memory access stage completed
250
251 Entering writeback stage
252 RegWr=1
253 Register file is being written back
254 Writing back to the register number:18
255 Value written back to register= 6
256 Writeback stage completed
257
258
259
260 CLOCK CYCLE= 6
261
262 Entering fetch stage:
263 Instruction fetched =
00111100000000010001000000000001
264 PC updated to
265 PC = 00000000100000000000000011000
266 Fetch stage completed
267
268 Entering Decode stage
269 Opcode=001111
270 Instruction is decoded as lui
271 RS=00000
272 RT=00001
```

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273 Immediate value=4097
274
275 Setting all control Signals
276 Alusrc:1
277 Zero_flag:0
278 MemWr:0
279 MemRd:0
280 Mem2Reg:0
281 jump:0
282 branch:0
283 branch_ne:0
284 PCsrc0
285 lui:1
286 Decode stage completed
287
288 Entering Execute stage
289 ALU_ctrl lines: 0 0 0 0
290 LUI instruction executed
291 Execute stage completed
292
293 Entering Memory access stage
294 Mem2Reg=0
295 Value from ALU is passed to write port of register
    file
296 Memory access stage completed
297
298 Entering writeback stage
299 RegWr=1
300 Register file is being written back
301 Writing back to register number :1
302 Value written back to register= 268500992
303 Writeback stage completed
304
305
306
307 CLOCK CYCLE= 7
308
309 Entering fetch stage:
310 Instruction fetched =
    1000110000110011000000000100000
311 PC updated to
```

```
312 PC = 0000000001000000000000000000000011100
313 Fetch stage completed
314
315 Entering Decode stage
316 Opcode=100011
317 Instruction is decoded as LW
318 RS=00001
319 RT=10011
320 Immediate value=32
321
322 Setting all control Signals
323 Alusrc:1
324 Zero_flag:0
325 MemWr:0
326 MemRd:1
327 Mem2Reg:1
328 jump:0
329 branch:0
330 branch_ne:0
331 PCsrc0
332 lui:0
333 Decode stage completed
334
335 Entering Execute stage
336 ALU_ctrl lines: 0 0 1 0
337 Sign extended value:00000000000000000000000000000000100000
338 ALU operands:
339 Operand1=268500992
340 Operand2=32
341 ALU ADD operation is performed
342 Execute stage completed
343
344 Entering Memory access stage
345 MemRd=1
346 Data Memory is being Read
347 Value read from the memory=18
348 Mem2Reg=1
349 Value from Memory is passed to write port of
    register file
350 Memory access stage completed
351
```

```
352 Entering writeback stage
353 RegWr=1
354 Register file is being written back
355 Writing back to register number :19
356 Value written back to register= 18
357 Writeback stage completed
358
359
360
361 CLOCK CYCLE= 8
362
363 Entering fetch stage:
364 Instruction fetched =
    00000010010100000000100000101010
365 PC updated to
366 PC = 000000000100000000000000000000100000
367 Fetch stage completed
368
369 Entering Decode stage
370 Opcode=000000
371 Instruction is decoded as R format
372 RS=10010
373 RT=10000
374 RD=00001
375 Function field=101010
376 Shift amount=00000
377
378 Setting all control Signals
379 Alusrc:0
380 Zero_flag:0
381 MemWr:0
382 MemRd:0
383 Mem2Reg:0
384 jump:0
385 branch:0
386 branch_ne:0
387 PCsrc0
388 lui:0
389 Decode stage completed
390
391 Entering Execute stage
```

```
392 ALU_ctrl lines: 0 1 1 1
393 ALU operands:
394 Operand1=6
395 Operand2=0
396 ALU SLT operation is performed
397 Execute stage completed
398
399 Entering Memory access stage
400 Mem2Reg=0
401 Value from ALU is passed to write port of register
    file
402 Memory access stage completed
403
404 Entering writeback stage
405 RegWr=1
406 Register file is being written back
407 Writing back to the register number:1
408 Value written back to register= 0
409 Writeback stage completed
410
411
412
413 CLOCK CYCLE= 9
414
415 Entering fetch stage:
416 Instruction fetched =
    000101000010000000000000000010101
417 PC updated to
418 PC = 000000001000000000000000100100
419 Fetch stage completed
420
421 Entering Decode stage
422 Opcode=000101
423 Instruction is decoded as BNE
424 RS=00001
425 RT=00000
426 Immediate value=21
427
428 Setting all control Signals
429 Alusrc:0
430 Zero_flag:0
```

```
431 MemWr:0
432 MemRd:0
433 Mem2Reg:0
434 jump:0
435 branch:0
436 branch_ne:1
437 PCsrc0
438 lui:0
439 Decode stage completed
440
441 Entering Execute stage
442 ALU_ctrl lines: 0 1 1 0
443 ALU operands:
444 Operand1=0
445 Operand2=0
446 ALU SUBTRACT operation is performed
447 Execute stage completed
448
449 Entering Memory access stage
450 Mem2Reg=0
451 Value from ALU is passed to write port of register
    file
452 Memory access stage completed
453
454 Entering writeback stage
455 Writeback stage completed
456
457
458
459 CLOCK CYCLE= 10
460
461 Entering fetch stage:
462 Instruction fetched =
    0000000000100000100000010000000
463 PC updated to
464 PC = 000000000100000000000000101000
465 Fetch stage completed
466
467 Entering Decode stage
468 Opcode=000000
469 Instruction is decoded as R format
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```
470 RS=00000
471 RT=10000
472 RD=01000
473 Function field=000000
474 Shift amount=00010
475
476 Setting all control Signals
477 Alusrc:0
478 Zero_flag:0
479 MemWr:0
480 MemRd:0
481 Mem2Reg:0
482 jump:0
483 branch:0
484 branch_ne:0
485 PCsrc0
486 lui:0
487 Decode stage completed
488
489 Entering Execute stage
490 ALU_ctrl lines: 0 1 0 0
491 ALU operands:
492 Operand1=0
493 Operand2=2
494 ALU SLL operation is performed
495 Execute stage completed
496
497 Entering Memory access stage
498 Mem2Reg=0
499 Value from ALU is passed to write port of register
file
500 Memory access stage completed
501
502 Entering writeback stage
503 RegWr=1
504 Register file is being written back
505 Writing back to the register number:8
506 Value written back to register= 0
507 Writeback stage completed
508
509
```

```
510
511 CLOCK CYCLE= 11
512
513 Entering fetch stage:
514 Instruction fetched =
    0000000000100100100100010000000
515 PC updated to
516 PC = 00000000100000000000000101100
517 Fetch stage completed
518
519 Entering Decode stage
520 Opcode=000000
521 Instruction is decoded as R format
522 RS=00000
523 RT=10010
524 RD=01001
525 Function field=000000
526 Shift amount=00010
527
528 Setting all control Signals
529 Alusrc:0
530 Zero_flag:0
531 MemWr:0
532 MemRd:0
533 Mem2Reg:0
534 jump:0
535 branch:0
536 branch_ne:0
537 PCsrc0
538 lui:0
539 Decode stage completed
540
541 Entering Execute stage
542 ALU_ctrl lines: 0 1 0 0
543 ALU operands:
544 Operand1=6
545 Operand2=2
546 ALU SLL operation is performed
547 Execute stage completed
548
549 Entering Memory access stage
```

```
550 Mem2Reg=0
551 Value from ALU is passed to write port of register
    file
552 Memory access stage completed
553
554 Entering writeback stage
555 RegWr=1
556 Register file is being written back
557 Writing back to the register number:9
558 Value written back to register= 24
559 Writeback stage completed
560
561
562
563 CLOCK CYCLE= 12
564
565 Entering fetch stage:
566 Instruction fetched =
    0011110000000010001000000000001
567 PC updated to
568 PC = 000000001000000000000000110000
569 Fetch stage completed
570
571 Entering Decode stage
572 Opcode=001111
573 Instruction is decoded as lui
574 RS=00000
575 RT=00001
576 Immediate value=4097
577
578 Setting all control Signals
579 Alusrc:1
580 Zero_flag:0
581 MemWr:0
582 MemRd:0
583 Mem2Reg:0
584 jump:0
585 branch:0
586 branch_ne:0
587 PCsrc0
588 lui:1
```

```
589 Decode stage completed
590
591 Entering Execute stage
592 ALU_ctrl lines: 0 0 0 0
593 LUI instruction executed
594 Execute stage completed
595
596 Entering Memory access stage
597 Mem2Reg=0
598 Value from ALU is passed to write port of register
  file
599 Memory access stage completed
600
601 Entering writeback stage
602 RegWr=1
603 Register file is being written back
604 Writing back to register number :1
605 Value written back to register= 268500992
606 Writeback stage completed
607
608
609
610 CLOCK CYCLE= 13
611
612 Entering fetch stage:
613 Instruction fetched =
  0000000001010000000100000100001
614 PC updated to
615 PC = 00000000100000000000000110100
616 Fetch stage completed
617
618 Entering Decode stage
619 Opcode=000000
620 Instruction is decoded as R format
621 RS=00001
622 RT=01000
623 RD=00001
624 Function field=100001
625 Shift amount=00000
626
627 Setting all control Signals
```



```
707 Entering writeback stage
708 RegWr=1
709 Register file is being written back
710 Writing back to register number :8
711 Value written back to register= 1
712 Writeback stage completed
713
714
715
716 CLOCK CYCLE= 15
717
718 Entering fetch stage:
719 Instruction fetched =
    0011110000000010001000000000001
720 PC updated to
721 PC = 000000001000000000000000111100
722 Fetch stage completed
723
724 Entering Decode stage
725 Opcode=001111
726 Instruction is decoded as lui
727 RS=00000
728 RT=00001
729 Immediate value=4097
730
731 Setting all control Signals
732 Alusrc:1
733 Zero_flag:0
734 MemWr:0
735 MemRd:0
736 Mem2Reg:0
737 jump:0
738 branch:0
739 branch_ne:0
740 PCsrc0
741 lui:1
742 Decode stage completed
743
744 Entering Execute stage
745 ALU_ctrl lines: 0 0 0 0
746 LUI instruction executed
```

```
747 Execute stage completed
748
749 Entering Memory access stage
750 Mem2Reg=0
751 Value from ALU is passed to write port of register
    file
752 Memory access stage completed
753
754 Entering writeback stage
755 RegWr=1
756 Register file is being written back
757 Writing back to register number :1
758 Value written back to register= 268500992
759 Writeback stage completed
760
761
762
763 CLOCK CYCLE= 16
764
765 Entering fetch stage:
766 Instruction fetched =
    0000000001010010000100000100001
767 PC updated to
768 PC = 00000000010000000000000000001000000
769 Fetch stage completed
770
771 Entering Decode stage
772 Opcode=000000
773 Instruction is decoded as R format
774 RS=00001
775 RT=01001
776 RD=00001
777 Function field=100001
778 Shift amount=00000
779
780 Setting all control Signals
781 Alusrc:0
782 Zero_flag:0
783 MemWr:0
784 MemRd:0
785 Mem2Reg:0
```

```
786 jump:0
787 branch:0
788 branch_ne:0
789 PCsrc0
790 lui:0
791 Decode stage completed
792
793 Entering Execute stage
794 ALU_ctrl lines: 0 0 1 0
795 ALU operands:
796 Operand1=268500992
797 Operand2=24
798 ALU ADD operation is performed
799 Execute stage completed
800
801 Entering Memory access stage
802 Mem2Reg=0
803 Value from ALU is passed to write port of register
file
804 Memory access stage completed
805
806 Entering writeback stage
807 RegWr=1
808 Register file is being written back
809 Writing back to the register number:1
810 Value written back to register= 268501016
811 Writeback stage completed
812
813
814
815 CLOCK CYCLE= 17
816
817 Entering fetch stage:
818 Instruction fetched =
10001100001010010000000000000000100
819 PC updated to
820 PC = 0000000010000000000000001000100
821 Fetch stage completed
822
823 Entering Decode stage
824 Opcode=100011
```

```
825 Instruction is decoded as LW
826 RS=00001
827 RT=01001
828 Immediate value=4
829
830 Setting all control Signals
831 Alusrc:1
832 Zero_flag:0
833 MemWr:0
834 MemRd:1
835 Mem2Reg:1
836 jump:0
837 branch:0
838 branch_ne:0
839 PCsrc0
840 lui:0
841 Decode stage completed
842
843 Entering Execute stage
844 ALU_ctrl lines: 0 0 1 0
845 Sign extended value:0000000000000000000000000000000100
846 ALU operands:
847 Operand1=268501016
848 Operand2=4
849 ALU ADD operation is performed
850 Execute stage completed
851
852 Entering Memory access stage
853 MemRd=1
854 Data Memory is being Read
855 Value read from the memory=22
856 Mem2Reg=1
857 Value from Memory is passed to write port of
register file
858 Memory access stage completed
859
860 Entering writeback stage
861 RegWr=1
862 Register file is being written back
863 Writing back to register number :9
864 Value written back to register= 22
```

```
865 Writeback stage completed
866
867
868
869 CLOCK CYCLE= 18
870
871 Entering fetch stage:
872 Instruction fetched =
    00000001000010010101000000100000
873 PC updated to
874 PC = 0000000001000000000000001001000
875 Fetch stage completed
876
877 Entering Decode stage
878 Opcode=000000
879 Instruction is decoded as R format
880 RS=01000
881 RT=01001
882 RD=01010
883 Function field=100000
884 Shift amount=00000
885
886 Setting all control Signals
887 Alusrc:0
888 Zero_flag:0
889 MemWr:0
890 MemRd:0
891 Mem2Reg:0
892 jump:0
893 branch:0
894 branch_ne:0
895 PCsrc0
896 lui:0
897 Decode stage completed
898
899 Entering Execute stage
900 ALU_ctrl lines: 0 0 1 0
901 ALU operands:
902 Operand1=1
903 Operand2=22
904 ALU ADD operation is performed
```

```
905 Execute stage completed
906
907 Entering Memory access stage
908 Mem2Reg=0
909 Value from ALU is passed to write port of register
    file
910 Memory access stage completed
911
912 Entering writeback stage
913 RegWr=1
914 Register file is being written back
915 Writing back to the register number:10
916 Value written back to register= 23
917 Writeback stage completed
918
919
920
921 CLOCK CYCLE= 19
922
923 Entering fetch stage:
924 Instruction fetched =
    0001010101001100000000000000100
925 PC updated to
926 PC = 0000000010000000000000001001100
927 Fetch stage completed
928
929 Entering Decode stage
930 Opcode=000101
931 Instruction is decoded as BNE
932 RS=01010
933 RT=10011
934 Immediate value=4
935
936 Setting all control Signals
937 Alusrc:0
938 Zero_flag:0
939 MemWr:0
940 MemRd:0
941 Mem2Reg:0
942 jump:0
943 branch:0
```

```
944 branch_ne:1
945 PCsrc0
946 lui:0
947 Decode stage completed
948
949 Entering Execute stage
950 ALU_ctrl lines: 0 1 1 0
951 ALU operands:
952 Operand1=23
953 Operand2=18
954 ALU SUBTRACT operation is performed
955 Execute stage completed
956
957 Entering Memory access stage
958 Mem2Reg=0
959 Value from ALU is passed to write port of register
file
960 Memory access stage completed
961
962 Entering writeback stage
963 Writeback stage completed
964
965
966
967 CLOCK CYCLE= 20
968
969 Entering fetch stage:
970 Instruction fetched =
00000010011010100000100000101010
971 PC updated to
972 PC = 0000000010000000000000001100000
973 Fetch stage completed
974
975 Entering Decode stage
976 Opcode=000000
977 Instruction is decoded as R format
978 RS=10011
979 RT=01010
980 RD=00001
981 Function field=101010
982 Shift amount=00000
```

```
983
984 Setting all control Signals
985 Alusrc:0
986 Zero_flag:0
987 MemWr:0
988 MemRd:0
989 Mem2Reg:0
990 jump:0
991 branch:0
992 branch_ne:0
993 PCsrc0
994 lui:0
995 Decode stage completed
996
997 Entering Execute stage
998 ALU_ctrl lines: 0 1 1 1
999 ALU operands:
1000 Operand1=18
1001 Operand2=23
1002 ALU SLT operation is performed
1003 Execute stage completed
1004
1005 Entering Memory access stage
1006 Mem2Reg=0
1007 Value from ALU is passed to write port of register
    file
1008 Memory access stage completed
1009
1010 Entering writeback stage
1011 RegWr=1
1012 Register file is being written back
1013 Writing back to the register number:1
1014 Value written back to register= 1
1015 Writeback stage completed
1016
1017
1018
1019 CLOCK CYCLE= 21
1020
1021 Entering fetch stage:
1022 Instruction fetched =
```



```
1062
1063
1064
1065 CLOCK CYCLE= 22
1066
1067 Entering fetch stage:
1068 Instruction fetched =
    00100000000000100000000000000001
1069 PC updated to
1070 PC = 000000000100000000000000000000001110000
1071 Fetch stage completed
1072
1073 Entering Decode stage
1074 Opcode=001000
1075 Instruction is decoded as add type instruction(addi
    or addiu)
1076 RS=00000
1077 RT=00001
1078 Immediate value=1
1079
1080 Setting all control Signals
1081 Alusrc:1
1082 Zero_flag:0
1083 MemWr:0
1084 MemRd:0
1085 Mem2Reg:0
1086 jump:0
1087 branch:0
1088 branch_ne:0
1089 PCsrc0
1090 lui:0
1091 Decode stage completed
1092
1093 Entering Execute stage
1094 ALU_ctrl lines: 0 0 1 0
1095 Sign extended value:
    00000000000000000000000000000001
1096 ALU operands:
1097 Operand1=0
1098 Operand2=1
1099 ALU ADD operation is performed
```

```
1100 Execute stage completed
1101
1102 Entering Memory access stage
1103 Mem2Reg=0
1104 Value from ALU is passed to write port of register
    file
1105 Memory access stage completed
1106
1107 Entering writeback stage
1108 RegWr=1
1109 Register file is being written back
1110 Writing back to register number :1
1111 Value written back to register= 1
1112 Writeback stage completed
1113
1114
1115
1116 CLOCK CYCLE= 23
1117
1118 Entering fetch stage:
1119 Instruction fetched =
    00000010010000011001000000100010
1120 PC updated to
1121 PC = 000000000100000000000001110100
1122 Fetch stage completed
1123
1124 Entering Decode stage
1125 Opcode=000000
1126 Instruction is decoded as R format
1127 RS=10010
1128 RT=00001
1129 RD=10010
1130 Function field=100010
1131 Shift amount=00000
1132
1133 Setting all control Signals
1134 Alusrc:0
1135 Zero_flag:0
1136 MemWr:0
1137 MemRd:0
1138 Mem2Reg:0
```

```
1139 jump:0
1140 branch:0
1141 branch_ne:0
1142 PCsrc0
1143 lui:0
1144 Decode stage completed
1145
1146 Entering Execute stage
1147 ALU_ctrl lines: 0 1 1 0
1148 ALU operands:
1149 Operand1=6
1150 Operand2=1
1151 ALU SUBTRACT operation is performed
1152 Execute stage completed
1153
1154 Entering Memory access stage
1155 Mem2Reg=0
1156 Value from ALU is passed to write port of register
    file
1157 Memory access stage completed
1158
1159 Entering writeback stage
1160 RegWr=1
1161 Register file is being written back
1162 Writing back to the register number:18
1163 Value written back to register= 5
1164 Writeback stage completed
1165
1166
1167
1168 CLOCK CYCLE= 24
1169
1170 Entering fetch stage:
1171 Instruction fetched =
    000010000001000000000000000000111
1172 PC updated to
1173 PC = 000000000100000000000000001111000
1174 Fetch stage completed
1175
1176 Entering Decode stage
1177 Opcode=000010
```

```
1178 Instruction is decoded as jump
1179 Jump target address=4194332
1180
1181 Setting all control Signals
1182 Alusrc:0
1183 Zero_flag:0
1184 MemWr:0
1185 MemRd:0
1186 Mem2Reg:0
1187 jump:1
1188 branch:0
1189 branch_ne:0
1190 PCsrc0
1191 lui:0
1192 Decode stage completed
1193
1194 Entering Execute stage
1195 ALU_ctrl lines: 0 0 0 0
1196 Jump instruction executed
1197 Execute stage completed
1198
1199 Entering Memory access stage
1200 Mem2Reg=0
1201 Value from ALU is passed to write port of register
    file
1202 Memory access stage completed
1203
1204 Entering writeback stage
1205 Writeback stage completed
1206
1207
1208
1209 CLOCK CYCLE= 25
1210
1211 Entering fetch stage:
1212 Instruction fetched =
    00000010010100000000100000101010
1213 PC updated to
1214 PC = 000000000100000000000000100000
1215 Fetch stage completed
1216
```

```
1217 Entering Decode stage
1218 Opcode=000000
1219 Instruction is decoded as R format
1220 RS=10010
1221 RT=10000
1222 RD=00001
1223 Function field=101010
1224 Shift amount=00000
1225
1226 Setting all control Signals
1227 Alusrc:0
1228 Zero_flag:0
1229 MemWr:0
1230 MemRd:0
1231 Mem2Reg:0
1232 jump:0
1233 branch:0
1234 branch_ne:0
1235 PCsrc0
1236 lui:0
1237 Decode stage completed
1238
1239 Entering Execute stage
1240 ALU_ctrl lines: 0 1 1 1
1241 ALU operands:
1242 Operand1=5
1243 Operand2=0
1244 ALU SLT operation is performed
1245 Execute stage completed
1246
1247 Entering Memory access stage
1248 Mem2Reg=0
1249 Value from ALU is passed to write port of register
    file
1250 Memory access stage completed
1251
1252 Entering writeback stage
1253 RegWr=1
1254 Register file is being written back
1255 Writing back to the register number:1
1256 Value written back to register= 0
```

```
1257 Writeback stage completed
1258
1259
1260
1261 CLOCK CYCLE= 26
1262
1263 Entering fetch stage:
1264 Instruction fetched =
    0001010000100000000000000000000010101
1265 PC updated to
1266 PC = 00000000010000000000000000000000100100
1267 Fetch stage completed
1268
1269 Entering Decode stage
1270 Opcode=000101
1271 Instruction is decoded as BNE
1272 RS=00001
1273 RT=00000
1274 Immediate value=21
1275
1276 Setting all control Signals
1277 Alusrc:0
1278 Zero_flag:0
1279 MemWr:0
1280 MemRd:0
1281 Mem2Reg:0
1282 jump:0
1283 branch:0
1284 branch_ne:1
1285 PCsrc0
1286 lui:0
1287 Decode stage completed
1288
1289 Entering Execute stage
1290 ALU_ctrl lines: 0 1 1 0
1291 ALU operands:
1292 Operand1=0
1293 Operand2=0
1294 ALU SUBTRACT operation is performed
1295 Execute stage completed
1296
```

```
1297 Entering Memory access stage
1298 Mem2Reg=0
1299 Value from ALU is passed to write port of register
    file
1300 Memory access stage completed
1301
1302 Entering writeback stage
1303 Writeback stage completed
1304
1305
1306
1307 CLOCK CYCLE= 27
1308
1309 Entering fetch stage:
1310 Instruction fetched =
    0000000000100000100000010000000
1311 PC updated to
1312 PC = 00000000100000000000000101000
1313 Fetch stage completed
1314
1315 Entering Decode stage
1316 Opcode=000000
1317 Instruction is decoded as R format
1318 RS=00000
1319 RT=10000
1320 RD=01000
1321 Function field=000000
1322 Shift amount=00010
1323
1324 Setting all control Signals
1325 Alusrc:0
1326 Zero_flag:0
1327 MemWr:0
1328 MemRd:0
1329 Mem2Reg:0
1330 jump:0
1331 branch:0
1332 branch_ne:0
1333 PCsrc0
1334 lui:0
1335 Decode stage completed
```

```
1336
1337 Entering Execute stage
1338 ALU_ctrl lines: 0 1 0 0
1339 ALU operands:
1340 Operand1=0
1341 Operand2=2
1342 ALU SLL operation is performed
1343 Execute stage completed
1344
1345 Entering Memory access stage
1346 Mem2Reg=0
1347 Value from ALU is passed to write port of register
    file
1348 Memory access stage completed
1349
1350 Entering writeback stage
1351 RegWr=1
1352 Register file is being written back
1353 Writing back to the register number:8
1354 Value written back to register= 0
1355 Writeback stage completed
1356
1357
1358
1359 CLOCK CYCLE= 28
1360
1361 Entering fetch stage:
1362 Instruction fetched =
    0000000000100100100100010000000
1363 PC updated to
1364 PC = 000000001000000000000000101100
1365 Fetch stage completed
1366
1367 Entering Decode stage
1368 Opcode=000000
1369 Instruction is decoded as R format
1370 RS=00000
1371 RT=10010
1372 RD=01001
1373 Function field=000000
1374 Shift amount=00010
```

```
1375
1376 Setting all control Signals
1377 Alusrc:0
1378 Zero_flag:0
1379 MemWr:0
1380 MemRd:0
1381 Mem2Reg:0
1382 jump:0
1383 branch:0
1384 branch_ne:0
1385 PCsrc0
1386 lui:0
1387 Decode stage completed
1388
1389 Entering Execute stage
1390 ALU_ctrl lines: 0 1 0 0
1391 ALU operands:
1392 Operand1=5
1393 Operand2=2
1394 ALU SLL operation is performed
1395 Execute stage completed
1396
1397 Entering Memory access stage
1398 Mem2Reg=0
1399 Value from ALU is passed to write port of register
    file
1400 Memory access stage completed
1401
1402 Entering writeback stage
1403 RegWr=1
1404 Register file is being written back
1405 Writing back to the register number:9
1406 Value written back to register= 20
1407 Writeback stage completed
1408
1409
1410
1411 CLOCK CYCLE= 29
1412
1413 Entering fetch stage:
1414 Instruction fetched =
```

```
1414 00111100000000010001000000000001  
1415 PC updated to  
1416 PC = 000000001000000000000000110000  
1417 Fetch stage completed  
1418  
1419 Entering Decode stage  
1420 Opcode=001111  
1421 Instruction is decoded as lui  
1422 RS=00000  
1423 RT=00001  
1424 Immediate value=4097  
1425  
1426 Setting all control Signals  
1427 Alusrc:1  
1428 Zero_flag:0  
1429 MemWr:0  
1430 MemRd:0  
1431 Mem2Reg:0  
1432 jump:0  
1433 branch:0  
1434 branch_ne:0  
1435 PCsrc0  
1436 lui:1  
1437 Decode stage completed  
1438  
1439 Entering Execute stage  
1440 ALU_ctrl lines: 0 0 0 0  
1441 LUI instruction executed  
1442 Execute stage completed  
1443  
1444 Entering Memory access stage  
1445 Mem2Reg=0  
1446 Value from ALU is passed to write port of register  
file  
1447 Memory access stage completed  
1448  
1449 Entering writeback stage  
1450 RegWr=1  
1451 Register file is being written back  
1452 Writing back to register number :1  
1453 Value written back to register= 268500992
```

```
1454 Writeback stage completed
1455
1456
1457
1458 CLOCK CYCLE= 30
1459
1460 Entering fetch stage:
1461 Instruction fetched =
    0000000001010000000100000100001
1462 PC updated to
1463 PC = 000000000100000000000000110100
1464 Fetch stage completed
1465
1466 Entering Decode stage
1467 Opcode=00000
1468 Instruction is decoded as R format
1469 RS=00001
1470 RT=01000
1471 RD=00001
1472 Function field=100001
1473 Shift amount=00000
1474
1475 Setting all control Signals
1476 Alusrc:0
1477 Zero_flag:0
1478 MemWr:0
1479 MemRd:0
1480 Mem2Reg:0
1481 jump:0
1482 branch:0
1483 branch_ne:0
1484 PCsrc0
1485 lui:0
1486 Decode stage completed
1487
1488 Entering Execute stage
1489 ALU_ctrl lines: 0 0 1 0
1490 ALU operands:
1491 Operand1=268500992
1492 Operand2=0
1493 ALU ADD operation is performed
```

```
1494 Execute stage completed
1495
1496 Entering Memory access stage
1497 Mem2Reg=0
1498 Value from ALU is passed to write port of register
    file
1499 Memory access stage completed
1500
1501 Entering writeback stage
1502 RegWr=1
1503 Register file is being written back
1504 Writing back to the register number:1
1505 Value written back to register= 268500992
1506 Writeback stage completed
1507
1508
1509
1510 CLOCK CYCLE= 31
1511
1512 Entering fetch stage:
1513 Instruction fetched =
    100011000010100000000000000000100
1514 PC updated to
1515 PC = 000000001000000000000000111000
1516 Fetch stage completed
1517
1518 Entering Decode stage
1519 Opcode=100011
1520 Instruction is decoded as LW
1521 RS=00001
1522 RT=01000
1523 Immediate value=4
1524
1525 Setting all control Signals
1526 Alusrc:1
1527 Zero_flag:0
1528 MemWr:0
1529 MemRd:1
1530 Mem2Reg:1
1531 jump:0
1532 branch:0
```

```
1533 branch_ne:0
1534 PCsrc0
1535 lui:0
1536 Decode stage completed
1537
1538 Entering Execute stage
1539 ALU_ctrl lines: 0 0 1 0
1540 Sign extended value:
    000000000000000000000000000000100
1541 ALU operands:
1542 Operand1=268500992
1543 Operand2=4
1544 ALU ADD operation is performed
1545 Execute stage completed
1546
1547 Entering Memory access stage
1548 MemRd=1
1549 Data Memory is being Read
1550 Value read from the memory=1
1551 Mem2Reg=1
1552 Value from Memory is passed to write port of
    register file
1553 Memory access stage completed
1554
1555 Entering writeback stage
1556 RegWr=1
1557 Register file is being written back
1558 Writing back to register number :8
1559 Value written back to register= 1
1560 Writeback stage completed
1561
1562
1563
1564 CLOCK CYCLE= 32
1565
1566 Entering fetch stage:
1567 Instruction fetched =
    0011110000000010001000000000001
1568 PC updated to
1569 PC = 0000000010000000000000111100
1570 Fetch stage completed
```

```
1571
1572 Entering Decode stage
1573 Opcode=001111
1574 Instruction is decoded as lui
1575 RS=00000
1576 RT=00001
1577 Immediate value=4097
1578
1579 Setting all control Signals
1580 Alusrc:1
1581 Zero_flag:0
1582 MemWr:0
1583 MemRd:0
1584 Mem2Reg:0
1585 jump:0
1586 branch:0
1587 branch_ne:0
1588 PCsrc0
1589 lui:1
1590 Decode stage completed
1591
1592 Entering Execute stage
1593 ALU_ctrl lines: 0 0 0 0
1594 LUI instruction executed
1595 Execute stage completed
1596
1597 Entering Memory access stage
1598 Mem2Reg=0
1599 Value from ALU is passed to write port of register
    file
1600 Memory access stage completed
1601
1602 Entering writeback stage
1603 RegWr=1
1604 Register file is being written back
1605 Writing back to register number :1
1606 Value written back to register= 268500992
1607 Writeback stage completed
1608
1609
1610
```

```
1611 CLOCK CYCLE= 33
1612
1613 Entering fetch stage:
1614 Instruction fetched =
    00000000001010010000100000100001
1615 PC updated to
1616 PC = 00000000100000000000001000000
1617 Fetch stage completed
1618
1619 Entering Decode stage
1620 Opcode=000000
1621 Instruction is decoded as R format
1622 RS=00001
1623 RT=01001
1624 RD=00001
1625 Function field=100001
1626 Shift amount=00000
1627
1628 Setting all control Signals
1629 Alusrc:0
1630 Zero_flag:0
1631 MemWr:0
1632 MemRd:0
1633 Mem2Reg:0
1634 jump:0
1635 branch:0
1636 branch_ne:0
1637 PCsrc0
1638 lui:0
1639 Decode stage completed
1640
1641 Entering Execute stage
1642 ALU_ctrl lines: 0 0 1 0
1643 ALU operands:
1644 Operand1=268500992
1645 Operand2=20
1646 ALU ADD operation is performed
1647 Execute stage completed
1648
1649 Entering Memory access stage
1650 Mem2Reg=0
```

```
1651 Value from ALU is passed to write port of register
      file
1652 Memory access stage completed
1653
1654 Entering writeback stage
1655 RegWr=1
1656 Register file is being written back
1657 Writing back to the register number:1
1658 Value written back to register= 268501012
1659 Writeback stage completed
1660
1661
1662
1663 CLOCK CYCLE= 34
1664
1665 Entering fetch stage:
1666 Instruction fetched =
      100011000010100100000000000000100
1667 PC updated to
1668 PC = 000000000100000000000000001000100
1669 Fetch stage completed
1670
1671 Entering Decode stage
1672 Opcode=100011
1673 Instruction is decoded as LW
1674 RS=00001
1675 RT=01001
1676 Immediate value=4
1677
1678 Setting all control Signals
1679 Alusrc:1
1680 Zero_flag:0
1681 MemWr:0
1682 MemRd:1
1683 Mem2Reg:1
1684 jump:0
1685 branch:0
1686 branch_ne:0
1687 PCsrc0
1688 lui:0
1689 Decode stage completed
```

```
1690
1691 Entering Execute stage
1692 ALU_ctrl lines: 0 0 1 0
1693 Sign extended value:
    00000000000000000000000000000000100
1694 ALU operands:
1695 Operand1=268501012
1696 Operand2=4
1697 ALU ADD operation is performed
1698 Execute stage completed
1699
1700 Entering Memory access stage
1701 MemRd=1
1702 Data Memory is being Read
1703 Value read from the memory=18
1704 Mem2Reg=1
1705 Value from Memory is passed to write port of
    register file
1706 Memory access stage completed
1707
1708 Entering writeback stage
1709 RegWr=1
1710 Register file is being written back
1711 Writing back to register number :9
1712 Value written back to register= 18
1713 Writeback stage completed
1714
1715
1716
1717 CLOCK CYCLE= 35
1718
1719 Entering fetch stage:
1720 Instruction fetched =
    00000001000010010101000000100000
1721 PC updated to
1722 PC = 0000000001000000000000001001000
1723 Fetch stage completed
1724
1725 Entering Decode stage
1726 Opcode=000000
1727 Instruction is decoded as R format
```

```
1728 RS=01000
1729 RT=01001
1730 RD=01010
1731 Function field=100000
1732 Shift amount=00000
1733
1734 Setting all control Signals
1735 Alusrc:0
1736 Zero_flag:0
1737 MemWr:0
1738 MemRd:0
1739 Mem2Reg:0
1740 jump:0
1741 branch:0
1742 branch_ne:0
1743 PCsrc0
1744 lui:0
1745 Decode stage completed
1746
1747 Entering Execute stage
1748 ALU_ctrl lines: 0 0 1 0
1749 ALU operands:
1750 Operand1=1
1751 Operand2=18
1752 ALU ADD operation is performed
1753 Execute stage completed
1754
1755 Entering Memory access stage
1756 Mem2Reg=0
1757 Value from ALU is passed to write port of register file
1758 Memory access stage completed
1759
1760 Entering writeback stage
1761 RegWr=1
1762 Register file is being written back
1763 Writing back to the register number:10
1764 Value written back to register= 19
1765 Writeback stage completed
1766
1767
```

```
1768
1769 CLOCK CYCLE= 36
1770
1771 Entering fetch stage:
1772 Instruction fetched =
    00010101010100110000000000000100
1773 PC updated to
1774 PC = 00000000100000000000001001100
1775 Fetch stage completed
1776
1777 Entering Decode stage
1778 Opcode=000101
1779 Instruction is decoded as BNE
1780 RS=01010
1781 RT=10011
1782 Immediate value=4
1783
1784 Setting all control Signals
1785 Alusrc:0
1786 Zero_flag:0
1787 MemWr:0
1788 MemRd:0
1789 Mem2Reg:0
1790 jump:0
1791 branch:0
1792 branch_ne:1
1793 PCsrc0
1794 lui:0
1795 Decode stage completed
1796
1797 Entering Execute stage
1798 ALU_ctrl lines: 0 1 1 0
1799 ALU operands:
1800 Operand1=19
1801 Operand2=18
1802 ALU SUBTRACT operation is performed
1803 Execute stage completed
1804
1805 Entering Memory access stage
1806 Mem2Reg=0
1807 Value from ALU is passed to write port of register
```

```
1807 file
1808 Memory access stage completed
1809
1810 Entering writeback stage
1811 Writeback stage completed
1812
1813
1814
1815 CLOCK CYCLE= 37
1816
1817 Entering fetch stage:
1818 Instruction fetched =
    00000010011010100000100000101010
1819 PC updated to
1820 PC = 000000000100000000000000000000001100000
1821 Fetch stage completed
1822
1823 Entering Decode stage
1824 Opcode=000000
1825 Instruction is decoded as R format
1826 RS=10011
1827 RT=01010
1828 RD=00001
1829 Function field=101010
1830 Shift amount=00000
1831
1832 Setting all control Signals
1833 Alusrc:0
1834 Zero_flag:0
1835 MemWr:0
1836 MemRd:0
1837 Mem2Reg:0
1838 jump:0
1839 branch:0
1840 branch_ne:0
1841 PCsrc0
1842 lui:0
1843 Decode stage completed
1844
1845 Entering Execute stage
1846 ALU_ctrl lines: 0 1 1 1
```

```
1847 ALU operands:  
1848 Operand1=18  
1849 Operand2=19  
1850 ALU SLT operation is performed  
1851 Execute stage completed  
1852  
1853 Entering Memory access stage  
1854 Mem2Reg=0  
1855 Value from ALU is passed to write port of register  
    file  
1856 Memory access stage completed  
1857  
1858 Entering writeback stage  
1859 RegWr=1  
1860 Register file is being written back  
1861 Writing back to the register number:1  
1862 Value written back to register= 1  
1863 Writeback stage completed  
1864  
1865  
1866  
1867 CLOCK CYCLE= 38  
1868  
1869 Entering fetch stage:  
1870 Instruction fetched =  
    00010100001000000000000000000010  
1871 PC updated to  
1872 PC = 0000000010000000000000001100100  
1873 Fetch stage completed  
1874  
1875 Entering Decode stage  
1876 Opcode=000101  
1877 Instruction is decoded as BNE  
1878 RS=00001  
1879 RT=00000  
1880 Immediate value=2  
1881  
1882 Setting all control Signals  
1883 Alusrc:0  
1884 Zero_flag:0  
1885 MemWr:0
```

```
1886 MemRd:0
1887 Mem2Reg:0
1888 jump:0
1889 branch:0
1890 branch_ne:1
1891 PCsrc0
1892 lui:0
1893 Decode stage completed
1894
1895 Entering Execute stage
1896 ALU_ctrl lines: 0 1 1 0
1897 ALU operands:
1898 Operand1=1
1899 Operand2=0
1900 ALU SUBTRACT operation is performed
1901 Execute stage completed
1902
1903 Entering Memory access stage
1904 Mem2Reg=0
1905 Value from ALU is passed to write port of register
file
1906 Memory access stage completed
1907
1908 Entering writeback stage
1909 Writeback stage completed
1910
1911
1912
1913 CLOCK CYCLE= 39
1914
1915 Entering fetch stage:
1916 Instruction fetched =
    00100000000000100000000000000001
1917 PC updated to
1918 PC = 00000000100000000000001110000
1919 Fetch stage completed
1920
1921 Entering Decode stage
1922 Opcode=001000
1923 Instruction is decoded as add type instruction(addi
or addiu)
```

```
1924 RS=00000
1925 RT=00001
1926 Immediate value=1
1927
1928 Setting all control Signals
1929 Alusrc:1
1930 Zero_flag:0
1931 MemWr:0
1932 MemRd:0
1933 Mem2Reg:0
1934 jump:0
1935 branch:0
1936 branch_ne:0
1937 PCsrc0
1938 lui:0
1939 Decode stage completed
1940
1941 Entering Execute stage
1942 ALU_ctrl lines: 0 0 1 0
1943 Sign extended value:
    00000000000000000000000000000001
1944 ALU operands:
1945 Operand1=0
1946 Operand2=1
1947 ALU ADD operation is performed
1948 Execute stage completed
1949
1950 Entering Memory access stage
1951 Mem2Reg=0
1952 Value from ALU is passed to write port of register
    file
1953 Memory access stage completed
1954
1955 Entering writeback stage
1956 RegWr=1
1957 Register file is being written back
1958 Writing back to register number :1
1959 Value written back to register= 1
1960 Writeback stage completed
1961
1962
```

```
1963
1964 CLOCK CYCLE= 40
1965
1966 Entering fetch stage:
1967 Instruction fetched =
    00000010010000011001000000100010
1968 PC updated to
1969 PC = 000000000100000000000001110100
1970 Fetch stage completed
1971
1972 Entering Decode stage
1973 Opcode=000000
1974 Instruction is decoded as R format
1975 RS=10010
1976 RT=00001
1977 RD=10010
1978 Function field=100010
1979 Shift amount=00000
1980
1981 Setting all control Signals
1982 Alusrc:0
1983 Zero_flag:0
1984 MemWr:0
1985 MemRd:0
1986 Mem2Reg:0
1987 jump:0
1988 branch:0
1989 branch_ne:0
1990 PCsrc0
1991 lui:0
1992 Decode stage completed
1993
1994 Entering Execute stage
1995 ALU_ctrl lines: 0 1 1 0
1996 ALU operands:
1997 Operand1=5
1998 Operand2=1
1999 ALU SUBTRACT operation is performed
2000 Execute stage completed
2001
2002 Entering Memory access stage
```

```
2003 Mem2Reg=0
2004 Value from ALU is passed to write port of register
    file
2005 Memory access stage completed
2006
2007 Entering writeback stage
2008 RegWr=1
2009 Register file is being written back
2010 Writing back to the register number:18
2011 Value written back to register= 4
2012 Writeback stage completed
2013
2014
2015
2016 CLOCK CYCLE= 41
2017
2018 Entering fetch stage:
2019 Instruction fetched =
    00001000000100000000000000000000111
2020 PC updated to
2021 PC = 000000000100000000000000000000001111000
2022 Fetch stage completed
2023
2024 Entering Decode stage
2025 Opcode=000010
2026 Instruction is decoded as jump
2027 Jump target address=4194332
2028
2029 Setting all control Signals
2030 Alusrc:0
2031 Zero_flag:0
2032 MemWr:0
2033 MemRd:0
2034 Mem2Reg:0
2035 jump:1
2036 branch:0
2037 branch_ne:0
2038 PCsrc0
2039 lui:0
2040 Decode stage completed
2041
```

```
2042 Entering Execute stage
2043 ALU_ctrl lines: 0 0 0 0
2044 Jump instruction executed
2045 Execute stage completed
2046
2047 Entering Memory access stage
2048 Mem2Reg=0
2049 Value from ALU is passed to write port of register
    file
2050 Memory access stage completed
2051
2052 Entering writeback stage
2053 Writeback stage completed
2054
2055
2056
2057 CLOCK CYCLE= 42
2058
2059 Entering fetch stage:
2060 Instruction fetched =
    0000001001010000000100000101010
2061 PC updated to
2062 PC = 000000001000000000000000100000
2063 Fetch stage completed
2064
2065 Entering Decode stage
2066 Opcode=00000
2067 Instruction is decoded as R format
2068 RS=10010
2069 RT=10000
2070 RD=00001
2071 Function field=101010
2072 Shift amount=00000
2073
2074 Setting all control Signals
2075 Alusrc:0
2076 Zero_flag:0
2077 MemWr:0
2078 MemRd:0
2079 Mem2Reg:0
2080 jump:0
```

```
2081 branch:0
2082 branch_ne:0
2083 PCsrc0
2084 lui:0
2085 Decode stage completed
2086
2087 Entering Execute stage
2088 ALU_ctrl lines: 0 1 1 1
2089 ALU operands:
2090 Operand1=4
2091 Operand2=0
2092 ALU SLT operation is performed
2093 Execute stage completed
2094
2095 Entering Memory access stage
2096 Mem2Reg=0
2097 Value from ALU is passed to write port of register
    file
2098 Memory access stage completed
2099
2100 Entering writeback stage
2101 RegWr=1
2102 Register file is being written back
2103 Writing back to the register number:1
2104 Value written back to register= 0
2105 Writeback stage completed
2106
2107
2108
2109 CLOCK CYCLE= 43
2110
2111 Entering fetch stage:
2112 Instruction fetched =
    000101000010000000000000000010101
2113 PC updated to
2114 PC = 000000001000000000000000100100
2115 Fetch stage completed
2116
2117 Entering Decode stage
2118 Opcode=000101
2119 Instruction is decoded as BNE
```

```
2120 RS=00001
2121 RT=00000
2122 Immediate value=21
2123
2124 Setting all control Signals
2125 Alusrc:0
2126 Zero_flag:0
2127 MemWr:0
2128 MemRd:0
2129 Mem2Reg:0
2130 jump:0
2131 branch:0
2132 branch_ne:1
2133 PCsrc0
2134 lui:0
2135 Decode stage completed
2136
2137 Entering Execute stage
2138 ALU_ctrl lines: 0 1 1 0
2139 ALU operands:
2140 Operand1=0
2141 Operand2=0
2142 ALU SUBTRACT operation is performed
2143 Execute stage completed
2144
2145 Entering Memory access stage
2146 Mem2Reg=0
2147 Value from ALU is passed to write port of register
    file
2148 Memory access stage completed
2149
2150 Entering writeback stage
2151 Writeback stage completed
2152
2153
2154
2155 CLOCK CYCLE= 44
2156
2157 Entering fetch stage:
2158 Instruction fetched =
    0000000000100000100000010000000
```

```
2159 PC updated to
2160 PC = 00000000010000000000000000101000
2161 Fetch stage completed
2162
2163 Entering Decode stage
2164 Opcode=000000
2165 Instruction is decoded as R format
2166 RS=00000
2167 RT=10000
2168 RD=01000
2169 Function field=000000
2170 Shift amount=00010
2171
2172 Setting all control Signals
2173 Alusrc:0
2174 Zero_flag:0
2175 MemWr:0
2176 MemRd:0
2177 Mem2Reg:0
2178 jump:0
2179 branch:0
2180 branch_ne:0
2181 PCsrc0
2182 lui:0
2183 Decode stage completed
2184
2185 Entering Execute stage
2186 ALU_ctrl lines: 0 1 0 0
2187 ALU operands:
2188 Operand1=0
2189 Operand2=2
2190 ALU SLL operation is performed
2191 Execute stage completed
2192
2193 Entering Memory access stage
2194 Mem2Reg=0
2195 Value from ALU is passed to write port of register
    file
2196 Memory access stage completed
2197
2198 Entering writeback stage
```

```
2199 RegWr=1
2200 Register file is being written back
2201 Writing back to the register number:8
2202 Value written back to register= 0
2203 Writeback stage completed
2204
2205
2206
2207 CLOCK CYCLE= 45
2208
2209 Entering fetch stage:
2210 Instruction fetched =
    0000000000100100100100010000000
2211 PC updated to
2212 PC = 0000000001000000000000000101100
2213 Fetch stage completed
2214
2215 Entering Decode stage
2216 Opcode=000000
2217 Instruction is decoded as R format
2218 RS=00000
2219 RT=10010
2220 RD=01001
2221 Function field=000000
2222 Shift amount=00010
2223
2224 Setting all control Signals
2225 Alusrc:0
2226 Zero_flag:0
2227 MemWr:0
2228 MemRd:0
2229 Mem2Reg:0
2230 jump:0
2231 branch:0
2232 branch_ne:0
2233 PCsrc0
2234 lui:0
2235 Decode stage completed
2236
2237 Entering Execute stage
2238 ALU_ctrl lines: 0 1 0 0
```

```
2239 ALU operands:  
2240 Operand1=4  
2241 Operand2=2  
2242 ALU SLL operation is performed  
2243 Execute stage completed  
2244  
2245 Entering Memory access stage  
2246 Mem2Reg=0  
2247 Value from ALU is passed to write port of register  
    file  
2248 Memory access stage completed  
2249  
2250 Entering writeback stage  
2251 RegWr=1  
2252 Register file is being written back  
2253 Writing back to the register number:9  
2254 Value written back to register= 16  
2255 Writeback stage completed  
2256  
2257  
2258  
2259 CLOCK CYCLE= 46  
2260  
2261 Entering fetch stage:  
2262 Instruction fetched =  
    00111100000000010001000000000001  
2263 PC updated to  
2264 PC = 00000000100000000000000110000  
2265 Fetch stage completed  
2266  
2267 Entering Decode stage  
2268 Opcode=001111  
2269 Instruction is decoded as lui  
2270 RS=00000  
2271 RT=00001  
2272 Immediate value=4097  
2273  
2274 Setting all control Signals  
2275 Alusrc:1  
2276 Zero_flag:0  
2277 MemWr:0
```

```
2278 MemRd:0
2279 Mem2Reg:0
2280 jump:0
2281 branch:0
2282 branch_ne:0
2283 PCsrc0
2284 lui:1
2285 Decode stage completed
2286
2287 Entering Execute stage
2288 ALU_ctrl lines: 0 0 0 0
2289 LUI instruction executed
2290 Execute stage completed
2291
2292 Entering Memory access stage
2293 Mem2Reg=0
2294 Value from ALU is passed to write port of register
    file
2295 Memory access stage completed
2296
2297 Entering writeback stage
2298 RegWr=1
2299 Register file is being written back
2300 Writing back to register number :1
2301 Value written back to register= 268500992
2302 Writeback stage completed
2303
2304
2305
2306 CLOCK CYCLE= 47
2307
2308 Entering fetch stage:
2309 Instruction fetched =
    0000000001010000000100000100001
2310 PC updated to
2311 PC = 000000000100000000000000110100
2312 Fetch stage completed
2313
2314 Entering Decode stage
2315 Opcode=000000
2316 Instruction is decoded as R format
```

```
2317 RS=00001
2318 RT=01000
2319 RD=00001
2320 Function field=100001
2321 Shift amount=00000
2322
2323 Setting all control Signals
2324 Alusrc:0
2325 Zero_flag:0
2326 MemWr:0
2327 MemRd:0
2328 Mem2Reg:0
2329 jump:0
2330 branch:0
2331 branch_ne:0
2332 PCsrc0
2333 lui:0
2334 Decode stage completed
2335
2336 Entering Execute stage
2337 ALU_ctrl lines: 0 0 1 0
2338 ALU operands:
2339 Operand1=268500992
2340 Operand2=0
2341 ALU ADD operation is performed
2342 Execute stage completed
2343
2344 Entering Memory access stage
2345 Mem2Reg=0
2346 Value from ALU is passed to write port of register file
2347 Memory access stage completed
2348
2349 Entering writeback stage
2350 RegWr=1
2351 Register file is being written back
2352 Writing back to the register number:1
2353 Value written back to register= 268500992
2354 Writeback stage completed
2355
2356
```

```
2357
2358 CLOCK CYCLE= 48
2359
2360 Entering fetch stage:
2361 Instruction fetched =
    10001100001010000000000000000000100
2362 PC updated to
2363 PC = 000000001000000000000000111000
2364 Fetch stage completed
2365
2366 Entering Decode stage
2367 Opcode=100011
2368 Instruction is decoded as LW
2369 RS=00001
2370 RT=01000
2371 Immediate value=4
2372
2373 Setting all control Signals
2374 Alusrc:1
2375 Zero_flag:0
2376 MemWr:0
2377 MemRd:1
2378 Mem2Reg:1
2379 jump:0
2380 branch:0
2381 branch_ne:0
2382 PCsrc0
2383 lui:0
2384 Decode stage completed
2385
2386 Entering Execute stage
2387 ALU_ctrl lines: 0 0 1 0
2388 Sign extended value:
    00000000000000000000000000000000100
2389 ALU operands:
2390 Operand1=268500992
2391 Operand2=4
2392 ALU ADD operation is performed
2393 Execute stage completed
2394
2395 Entering Memory access stage
```

```
2396 MemRd=1
2397 Data Memory is being Read
2398 Value read from the memory=1
2399 Mem2Reg=1
2400 Value from Memory is passed to write port of
    register file
2401 Memory access stage completed
2402
2403 Entering writeback stage
2404 RegWr=1
2405 Register file is being written back
2406 Writing back to register number :8
2407 Value written back to register= 1
2408 Writeback stage completed
2409
2410
2411
2412 CLOCK CYCLE= 49
2413
2414 Entering fetch stage:
2415 Instruction fetched =
    00111100000000010001000000000001
2416 PC updated to
2417 PC = 00000000100000000000000111100
2418 Fetch stage completed
2419
2420 Entering Decode stage
2421 Opcode=001111
2422 Instruction is decoded as lui
2423 RS=00000
2424 RT=00001
2425 Immediate value=4097
2426
2427 Setting all control Signals
2428 Alusrc:1
2429 Zero_flag:0
2430 MemWr:0
2431 MemRd:0
2432 Mem2Reg:0
2433 jump:0
2434 branch:0
```

```
2435 branch_ne:0
2436 PCsrc0
2437 lui:1
2438 Decode stage completed
2439
2440 Entering Execute stage
2441 ALU_ctrl lines: 0 0 0 0
2442 LUI instruction executed
2443 Execute stage completed
2444
2445 Entering Memory access stage
2446 Mem2Reg=0
2447 Value from ALU is passed to write port of register
    file
2448 Memory access stage completed
2449
2450 Entering writeback stage
2451 RegWr=1
2452 Register file is being written back
2453 Writing back to register number :1
2454 Value written back to register= 268500992
2455 Writeback stage completed
2456
2457
2458
2459 CLOCK CYCLE= 50
2460
2461 Entering fetch stage:
2462 Instruction fetched =
    0000000001010010000100000100001
2463 PC updated to
2464 PC = 0000000001000000000000001000000
2465 Fetch stage completed
2466
2467 Entering Decode stage
2468 Opcode=000000
2469 Instruction is decoded as R format
2470 RS=00001
2471 RT=01001
2472 RD=00001
2473 Function field=100001
```

```
2474 Shift amount=00000
2475
2476 Setting all control Signals
2477 Alusrc:0
2478 Zero_flag:0
2479 MemWr:0
2480 MemRd:0
2481 Mem2Reg:0
2482 jump:0
2483 branch:0
2484 branch_ne:0
2485 PCsrc0
2486 lui:0
2487 Decode stage completed
2488
2489 Entering Execute stage
2490 ALU_ctrl lines: 0 0 1 0
2491 ALU operands:
2492 Operand1=268500992
2493 Operand2=16
2494 ALU ADD operation is performed
2495 Execute stage completed
2496
2497 Entering Memory access stage
2498 Mem2Reg=0
2499 Value from ALU is passed to write port of register
      file
2500 Memory access stage completed
2501
2502 Entering writeback stage
2503 RegWr=1
2504 Register file is being written back
2505 Writing back to the register number:1
2506 Value written back to register= 268501008
2507 Writeback stage completed
2508
2509
2510
2511 CLOCK CYCLE= 51
2512
2513 Entering fetch stage:
```

```
2514 Instruction fetched =
    100011000010100100000000000000100
2515 PC updated to
2516 PC = 0000000010000000000000001000100
2517 Fetch stage completed
2518
2519 Entering Decode stage
2520 Opcode=100011
2521 Instruction is decoded as LW
2522 RS=00001
2523 RT=01001
2524 Immediate value=4
2525
2526 Setting all control Signals
2527 Alusrc:1
2528 Zero_flag:0
2529 MemWr:0
2530 MemRd:1
2531 Mem2Reg:1
2532 jump:0
2533 branch:0
2534 branch_ne:0
2535 PCsrc0
2536 lui:0
2537 Decode stage completed
2538
2539 Entering Execute stage
2540 ALU_ctrl lines: 0 0 1 0
2541 Sign extended value:
    000000000000000000000000000000100
2542 ALU operands:
2543 Operand1=268501008
2544 Operand2=4
2545 ALU ADD operation is performed
2546 Execute stage completed
2547
2548 Entering Memory access stage
2549 MemRd=1
2550 Data Memory is being Read
2551 Value read from the memory=13
2552 Mem2Reg=1
```

```
2553 Value from Memory is passed to write port of
register file
2554 Memory access stage completed
2555
2556 Entering writeback stage
2557 RegWr=1
2558 Register file is being written back
2559 Writing back to register number :9
2560 Value written back to register= 13
2561 Writeback stage completed
2562
2563
2564
2565 CLOCK CYCLE= 52
2566
2567 Entering fetch stage:
2568 Instruction fetched =
    00000001000010010101000000100000
2569 PC updated to
2570 PC = 0000000001000000000000001001000
2571 Fetch stage completed
2572
2573 Entering Decode stage
2574 Opcode=000000
2575 Instruction is decoded as R format
2576 RS=01000
2577 RT=01001
2578 RD=01010
2579 Function field=100000
2580 Shift amount=00000
2581
2582 Setting all control Signals
2583 Alusrc:0
2584 Zero_flag:0
2585 MemWr:0
2586 MemRd:0
2587 Mem2Reg:0
2588 jump:0
2589 branch:0
2590 branch_ne:0
2591 PCsrc0
```

```
2592 lui:0
2593 Decode stage completed
2594
2595 Entering Execute stage
2596 ALU_ctrl lines: 0 0 1 0
2597 ALU operands:
2598 Operand1=1
2599 Operand2=13
2600 ALU ADD operation is performed
2601 Execute stage completed
2602
2603 Entering Memory access stage
2604 Mem2Reg=0
2605 Value from ALU is passed to write port of register
    file
2606 Memory access stage completed
2607
2608 Entering writeback stage
2609 RegWr=1
2610 Register file is being written back
2611 Writing back to the register number:10
2612 Value written back to register= 14
2613 Writeback stage completed
2614
2615
2616
2617 CLOCK CYCLE= 53
2618
2619 Entering fetch stage:
2620 Instruction fetched =
    0001010101001100000000000000100
2621 PC updated to
2622 PC = 00000000100000000000001001100
2623 Fetch stage completed
2624
2625 Entering Decode stage
2626 Opcode=000101
2627 Instruction is decoded as BNE
2628 RS=01010
2629 RT=10011
2630 Immediate value=4
```

```
2631
2632 Setting all control Signals
2633 Alusrc:0
2634 Zero_flag:0
2635 MemWr:0
2636 MemRd:0
2637 Mem2Reg:0
2638 jump:0
2639 branch:0
2640 branch_ne:1
2641 PCsrc0
2642 lui:0
2643 Decode stage completed
2644
2645 Entering Execute stage
2646 ALU_ctrl lines: 0 1 1 0
2647 ALU operands:
2648 Operand1=14
2649 Operand2=18
2650 ALU SUBTRACT operation is performed
2651 Execute stage completed
2652
2653 Entering Memory access stage
2654 Mem2Reg=0
2655 Value from ALU is passed to write port of register
file
2656 Memory access stage completed
2657
2658 Entering writeback stage
2659 Writeback stage completed
2660
2661
2662
2663 CLOCK CYCLE= 54
2664
2665 Entering fetch stage:
2666 Instruction fetched =
00000010011010100000100000101010
2667 PC updated to
2668 PC = 0000000010000000000001100000
2669 Fetch stage completed
```

```
2670
2671 Entering Decode stage
2672 Opcode=000000
2673 Instruction is decoded as R format
2674 RS=10011
2675 RT=01010
2676 RD=00001
2677 Function field=101010
2678 Shift amount=00000
2679
2680 Setting all control Signals
2681 Alusrc:0
2682 Zero_flag:0
2683 MemWr:0
2684 MemRd:0
2685 Mem2Reg:0
2686 jump:0
2687 branch:0
2688 branch_ne:0
2689 PCsrc0
2690 lui:0
2691 Decode stage completed
2692
2693 Entering Execute stage
2694 ALU_ctrl lines: 0 1 1 1
2695 ALU operands:
2696 Operand1=18
2697 Operand2=14
2698 ALU SLT operation is performed
2699 Execute stage completed
2700
2701 Entering Memory access stage
2702 Mem2Reg=0
2703 Value from ALU is passed to write port of register
    file
2704 Memory access stage completed
2705
2706 Entering writeback stage
2707 RegWr=1
2708 Register file is being written back
2709 Writing back to the register number:1
```

```
2710 Value written back to register= 0
2711 Writeback stage completed
2712
2713
2714
2715 CLOCK CYCLE= 55
2716
2717 Entering fetch stage:
2718 Instruction fetched =
    00010100001000000000000000000010
2719 PC updated to
2720 PC = 000000001000000000000001100100
2721 Fetch stage completed
2722
2723 Entering Decode stage
2724 Opcode=000101
2725 Instruction is decoded as BNE
2726 RS=00001
2727 RT=00000
2728 Immediate value=2
2729
2730 Setting all control Signals
2731 Alusrc:0
2732 Zero_flag:0
2733 MemWr:0
2734 MemRd:0
2735 Mem2Reg:0
2736 jump:0
2737 branch:0
2738 branch_ne:1
2739 PCsrc0
2740 lui:0
2741 Decode stage completed
2742
2743 Entering Execute stage
2744 ALU_ctrl lines: 0 1 1 0
2745 ALU operands:
2746 Operand1=0
2747 Operand2=0
2748 ALU SUBTRACT operation is performed
2749 Execute stage completed
```

```
2750
2751 Entering Memory access stage
2752 Mem2Reg=0
2753 Value from ALU is passed to write port of register
    file
2754 Memory access stage completed
2755
2756 Entering writeback stage
2757 Writeback stage completed
2758
2759
2760
2761 CLOCK CYCLE= 56
2762
2763 Entering fetch stage:
2764 Instruction fetched =
    00100010000100000000000000000001
2765 PC updated to
2766 PC = 00000000100000000000001101000
2767 Fetch stage completed
2768
2769 Entering Decode stage
2770 Opcode=001000
2771 Instruction is decoded as add type instruction(addi
    or addiu)
2772 RS=10000
2773 RT=10000
2774 Immediate value=1
2775
2776 Setting all control Signals
2777 Alusrc:1
2778 Zero_flag:0
2779 MemWr:0
2780 MemRd:0
2781 Mem2Reg:0
2782 jump:0
2783 branch:0
2784 branch_ne:0
2785 PCsrc0
2786 lui:0
2787 Decode stage completed
```

```
2788
2789 Entering Execute stage
2790 ALU_ctrl lines: 0 0 1 0
2791 Sign extended value:
    00000000000000000000000000000001
2792 ALU operands:
2793 Operand1=0
2794 Operand2=1
2795 ALU ADD operation is performed
2796 Execute stage completed
2797
2798 Entering Memory access stage
2799 Mem2Reg=0
2800 Value from ALU is passed to write port of register
    file
2801 Memory access stage completed
2802
2803 Entering writeback stage
2804 RegWr=1
2805 Register file is being written back
2806 Writing back to register number :16
2807 Value written back to register= 1
2808 Writeback stage completed
2809
2810
2811
2812 CLOCK CYCLE= 57
2813
2814 Entering fetch stage:
2815 Instruction fetched =
    000010000001000000000000000000111
2816 PC updated to
2817 PC = 0000000001000000000000001101100
2818 Fetch stage completed
2819
2820 Entering Decode stage
2821 Opcode=000010
2822 Instruction is decoded as jump
2823 Jump target address=4194332
2824
2825 Setting all control Signals
```

```
2826 Alusrc:0
2827 Zero_flag:0
2828 MemWr:0
2829 MemRd:0
2830 Mem2Reg:0
2831 jump:1
2832 branch:0
2833 branch_ne:0
2834 PCsrc0
2835 lui:0
2836 Decode stage completed
2837
2838 Entering Execute stage
2839 ALU_ctrl lines: 0 0 0 0
2840 Jump instruction executed
2841 Execute stage completed
2842
2843 Entering Memory access stage
2844 Mem2Reg=0
2845 Value from ALU is passed to write port of register
file
2846 Memory access stage completed
2847
2848 Entering writeback stage
2849 Writeback stage completed
2850
2851
2852
2853 CLOCK CYCLE= 58
2854
2855 Entering fetch stage:
2856 Instruction fetched =
    00000010010100000000100000101010
2857 PC updated to
2858 PC = 000000000100000000000000100000
2859 Fetch stage completed
2860
2861 Entering Decode stage
2862 Opcode=000000
2863 Instruction is decoded as R format
2864 RS=10010
```

```
2865 RT=10000
2866 RD=00001
2867 Function field=101010
2868 Shift amount=00000
2869
2870 Setting all control Signals
2871 Alusrc:0
2872 Zero_flag:0
2873 MemWr:0
2874 MemRd:0
2875 Mem2Reg:0
2876 jump:0
2877 branch:0
2878 branch_ne:0
2879 PCsrc0
2880 lui:0
2881 Decode stage completed
2882
2883 Entering Execute stage
2884 ALU_ctrl lines: 0 1 1 1
2885 ALU operands:
2886 Operand1=4
2887 Operand2=1
2888 ALU SLT operation is performed
2889 Execute stage completed
2890
2891 Entering Memory access stage
2892 Mem2Reg=0
2893 Value from ALU is passed to write port of register
    file
2894 Memory access stage completed
2895
2896 Entering writeback stage
2897 RegWr=1
2898 Register file is being written back
2899 Writing back to the register number:1
2900 Value written back to register= 0
2901 Writeback stage completed
2902
2903
2904
```

```
2905 CLOCK CYCLE= 59
2906
2907 Entering fetch stage:
2908 Instruction fetched =
    000101000010000000000000000010101
2909 PC updated to
2910 PC = 000000001000000000000000100100
2911 Fetch stage completed
2912
2913 Entering Decode stage
2914 Opcode=000101
2915 Instruction is decoded as BNE
2916 RS=00001
2917 RT=00000
2918 Immediate value=21
2919
2920 Setting all control Signals
2921 Alusrc:0
2922 Zero_flag:0
2923 MemWr:0
2924 MemRd:0
2925 Mem2Reg:0
2926 jump:0
2927 branch:0
2928 branch_ne:1
2929 PCsrc0
2930 lui:0
2931 Decode stage completed
2932
2933 Entering Execute stage
2934 ALU_ctrl lines: 0 1 1 0
2935 ALU operands:
2936 Operand1=0
2937 Operand2=0
2938 ALU SUBTRACT operation is performed
2939 Execute stage completed
2940
2941 Entering Memory access stage
2942 Mem2Reg=0
2943 Value from ALU is passed to write port of register
    file
```

```
2944 Memory access stage completed
2945
2946 Entering writeback stage
2947 Writeback stage completed
2948
2949
2950
2951 CLOCK CYCLE= 60
2952
2953 Entering fetch stage:
2954 Instruction fetched =
    00000000000100000100000010000000
2955 PC updated to
2956 PC = 000000000100000000000000101000
2957 Fetch stage completed
2958
2959 Entering Decode stage
2960 Opcode=000000
2961 Instruction is decoded as R format
2962 RS=00000
2963 RT=10000
2964 RD=01000
2965 Function field=000000
2966 Shift amount=00010
2967
2968 Setting all control Signals
2969 Alusrc:0
2970 Zero_flag:0
2971 MemWr:0
2972 MemRd:0
2973 Mem2Reg:0
2974 jump:0
2975 branch:0
2976 branch_ne:0
2977 PCsrc0
2978 lui:0
2979 Decode stage completed
2980
2981 Entering Execute stage
2982 ALU_ctrl lines: 0 1 0 0
2983 ALU operands:
```

```
2984 Operand1=1
2985 Operand2=2
2986 ALU SLL operation is performed
2987 Execute stage completed
2988
2989 Entering Memory access stage
2990 Mem2Reg=0
2991 Value from ALU is passed to write port of register
  file
2992 Memory access stage completed
2993
2994 Entering writeback stage
2995 RegWr=1
2996 Register file is being written back
2997 Writing back to the register number:8
2998 Value written back to register= 4
2999 Writeback stage completed
3000
3001
3002
3003 CLOCK CYCLE= 61
3004
3005 Entering fetch stage:
3006 Instruction fetched =
  0000000000100100100100010000000
3007 PC updated to
3008 PC = 0000000001000000000000000101100
3009 Fetch stage completed
3010
3011 Entering Decode stage
3012 Opcode=000000
3013 Instruction is decoded as R format
3014 RS=00000
3015 RT=10010
3016 RD=01001
3017 Function field=000000
3018 Shift amount=00010
3019
3020 Setting all control Signals
3021 Alusrc:0
3022 Zero_flag:0
```

```
3023 MemWr:0
3024 MemRd:0
3025 Mem2Reg:0
3026 jump:0
3027 branch:0
3028 branch_ne:0
3029 PCsrc0
3030 lui:0
3031 Decode stage completed
3032
3033 Entering Execute stage
3034 ALU_ctrl lines: 0 1 0 0
3035 ALU operands:
3036 Operand1=4
3037 Operand2=2
3038 ALU SLL operation is performed
3039 Execute stage completed
3040
3041 Entering Memory access stage
3042 Mem2Reg=0
3043 Value from ALU is passed to write port of register
    file
3044 Memory access stage completed
3045
3046 Entering writeback stage
3047 RegWr=1
3048 Register file is being written back
3049 Writing back to the register number:9
3050 Value written back to register= 16
3051 Writeback stage completed
3052
3053
3054
3055 CLOCK CYCLE= 62
3056
3057 Entering fetch stage:
3058 Instruction fetched =
    0011110000000010001000000000001
3059 PC updated to
3060 PC = 0000000010000000000000110000
3061 Fetch stage completed
```

```
3062
3063 Entering Decode stage
3064 Opcode=001111
3065 Instruction is decoded as lui
3066 RS=00000
3067 RT=00001
3068 Immediate value=4097
3069
3070 Setting all control Signals
3071 Alusrc:1
3072 Zero_flag:0
3073 MemWr:0
3074 MemRd:0
3075 Mem2Reg:0
3076 jump:0
3077 branch:0
3078 branch_ne:0
3079 PCsrc0
3080 lui:1
3081 Decode stage completed
3082
3083 Entering Execute stage
3084 ALU_ctrl lines: 0 0 0 0
3085 LUI instruction executed
3086 Execute stage completed
3087
3088 Entering Memory access stage
3089 Mem2Reg=0
3090 Value from ALU is passed to write port of register
      file
3091 Memory access stage completed
3092
3093 Entering writeback stage
3094 RegWr=1
3095 Register file is being written back
3096 Writing back to register number :1
3097 Value written back to register= 268500992
3098 Writeback stage completed
3099
3100
3101
```

```
3102 CLOCK CYCLE= 63
3103
3104 Entering fetch stage:
3105 Instruction fetched =
    0000000001010000000100000100001
3106 PC updated to
3107 PC = 00000000100000000000000110100
3108 Fetch stage completed
3109
3110 Entering Decode stage
3111 Opcode=000000
3112 Instruction is decoded as R format
3113 RS=00001
3114 RT=01000
3115 RD=00001
3116 Function field=100001
3117 Shift amount=00000
3118
3119 Setting all control Signals
3120 Alusrc:0
3121 Zero_flag:0
3122 MemWr:0
3123 MemRd:0
3124 Mem2Reg:0
3125 jump:0
3126 branch:0
3127 branch_ne:0
3128 PCsrc0
3129 lui:0
3130 Decode stage completed
3131
3132 Entering Execute stage
3133 ALU_ctrl lines: 0 0 1 0
3134 ALU operands:
3135 Operand1=268500992
3136 Operand2=4
3137 ALU ADD operation is performed
3138 Execute stage completed
3139
3140 Entering Memory access stage
3141 Mem2Reg=0
```

```
3142 Value from ALU is passed to write port of register
      file
3143 Memory access stage completed
3144
3145 Entering writeback stage
3146 RegWr=1
3147 Register file is being written back
3148 Writing back to the register number:1
3149 Value written back to register= 268500996
3150 Writeback stage completed
3151
3152
3153
3154 CLOCK CYCLE= 64
3155
3156 Entering fetch stage:
3157 Instruction fetched =
      10001100001010000000000000000000100
3158 PC updated to
3159 PC = 00000000010000000000000000000000111000
3160 Fetch stage completed
3161
3162 Entering Decode stage
3163 Opcode=100011
3164 Instruction is decoded as LW
3165 RS=00001
3166 RT=01000
3167 Immediate value=4
3168
3169 Setting all control Signals
3170 Alusrc:1
3171 Zero_flag:0
3172 MemWr:0
3173 MemRd:1
3174 Mem2Reg:1
3175 jump:0
3176 branch:0
3177 branch_ne:0
3178 PCsrc0
3179 lui:0
3180 Decode stage completed
```

```
3181
3182 Entering Execute stage
3183 ALU_ctrl lines: 0 0 1 0
3184 Sign extended value:
    00000000000000000000000000000000100
3185 ALU operands:
3186 Operand1=268500996
3187 Operand2=4
3188 ALU ADD operation is performed
3189 Execute stage completed
3190
3191 Entering Memory access stage
3192 MemRd=1
3193 Data Memory is being Read
3194 Value read from the memory=5
3195 Mem2Reg=1
3196 Value from Memory is passed to write port of
    register file
3197 Memory access stage completed
3198
3199 Entering writeback stage
3200 RegWr=1
3201 Register file is being written back
3202 Writing back to register number :8
3203 Value written back to register= 5
3204 Writeback stage completed
3205
3206
3207
3208 CLOCK CYCLE= 65
3209
3210 Entering fetch stage:
3211 Instruction fetched =
    00111100000000010001000000000001
3212 PC updated to
3213 PC = 000000001000000000000000111100
3214 Fetch stage completed
3215
3216 Entering Decode stage
3217 Opcode=001111
3218 Instruction is decoded as lui
```

```
3219 RS=00000
3220 RT=00001
3221 Immediate value=4097
3222
3223 Setting all control Signals
3224 Alusrc:1
3225 Zero_flag:0
3226 MemWr:0
3227 MemRd:0
3228 Mem2Reg:0
3229 jump:0
3230 branch:0
3231 branch_ne:0
3232 PCsrc0
3233 lui:1
3234 Decode stage completed
3235
3236 Entering Execute stage
3237 ALU_ctrl lines: 0 0 0 0
3238 LUI instruction executed
3239 Execute stage completed
3240
3241 Entering Memory access stage
3242 Mem2Reg=0
3243 Value from ALU is passed to write port of register
    file
3244 Memory access stage completed
3245
3246 Entering writeback stage
3247 RegWr=1
3248 Register file is being written back
3249 Writing back to register number :1
3250 Value written back to register= 268500992
3251 Writeback stage completed
3252
3253
3254
3255 CLOCK CYCLE= 66
3256
3257 Entering fetch stage:
3258 Instruction fetched =
```

```
3258 0000000001010010000100000100001
3259 PC updated to
3260 PC = 0000000001000000000000001000000
3261 Fetch stage completed
3262
3263 Entering Decode stage
3264 Opcode=00000
3265 Instruction is decoded as R format
3266 RS=00001
3267 RT=01001
3268 RD=00001
3269 Function field=100001
3270 Shift amount=00000
3271
3272 Setting all control Signals
3273 Alusrc:0
3274 Zero_flag:0
3275 MemWr:0
3276 MemRd:0
3277 Mem2Reg:0
3278 jump:0
3279 branch:0
3280 branch_ne:0
3281 PCsrc0
3282 lui:0
3283 Decode stage completed
3284
3285 Entering Execute stage
3286 ALU_ctrl lines: 0 0 1 0
3287 ALU operands:
3288 Operand1=268500992
3289 Operand2=16
3290 ALU ADD operation is performed
3291 Execute stage completed
3292
3293 Entering Memory access stage
3294 Mem2Reg=0
3295 Value from ALU is passed to write port of register
      file
3296 Memory access stage completed
3297
```

```
3298 Entering writeback stage
3299 RegWr=1
3300 Register file is being written back
3301 Writing back to the register number:1
3302 Value written back to register= 268501008
3303 Writeback stage completed
3304
3305
3306
3307 CLOCK CYCLE= 67
3308
3309 Entering fetch stage:
3310 Instruction fetched =
    100011000010100100000000000000100
3311 PC updated to
3312 PC = 0000000010000000000000001000100
3313 Fetch stage completed
3314
3315 Entering Decode stage
3316 Opcode=100011
3317 Instruction is decoded as LW
3318 RS=00001
3319 RT=01001
3320 Immediate value=4
3321
3322 Setting all control Signals
3323 Alusrc:1
3324 Zero_flag:0
3325 MemWr:0
3326 MemRd:1
3327 Mem2Reg:1
3328 jump:0
3329 branch:0
3330 branch_ne:0
3331 PCsrc0
3332 lui:0
3333 Decode stage completed
3334
3335 Entering Execute stage
3336 ALU_ctrl lines: 0 0 1 0
3337 Sign extended value:
```



```
3376 Shift amount=00000
3377
3378 Setting all control Signals
3379 Alusrc:0
3380 Zero_flag:0
3381 MemWr:0
3382 MemRd:0
3383 Mem2Reg:0
3384 jump:0
3385 branch:0
3386 branch_ne:0
3387 PCsrc0
3388 lui:0
3389 Decode stage completed
3390
3391 Entering Execute stage
3392 ALU_ctrl lines: 0 0 1 0
3393 ALU operands:
3394 Operand1=5
3395 Operand2=13
3396 ALU ADD operation is performed
3397 Execute stage completed
3398
3399 Entering Memory access stage
3400 Mem2Reg=0
3401 Value from ALU is passed to write port of register
    file
3402 Memory access stage completed
3403
3404 Entering writeback stage
3405 RegWr=1
3406 Register file is being written back
3407 Writing back to the register number:10
3408 Value written back to register= 18
3409 Writeback stage completed
3410
3411
3412
3413 CLOCK CYCLE= 69
3414
3415 Entering fetch stage:
```

```
3416 Instruction fetched =
    000101010101001100000000000000100
3417 PC updated to
3418 PC = 0000000010000000000000001001100
3419 Fetch stage completed
3420
3421 Entering Decode stage
3422 Opcode=000101
3423 Instruction is decoded as BNE
3424 RS=01010
3425 RT=10011
3426 Immediate value=4
3427
3428 Setting all control Signals
3429 Alusrc:0
3430 Zero_flag:0
3431 MemWr:0
3432 MemRd:0
3433 Mem2Reg:0
3434 jump:0
3435 branch:0
3436 branch_ne:1
3437 PCsrc0
3438 lui:0
3439 Decode stage completed
3440
3441 Entering Execute stage
3442 ALU_ctrl lines: 0 1 1 0
3443 ALU operands:
3444 Operand1=18
3445 Operand2=18
3446 ALU SUBTRACT operation is performed
3447 Execute stage completed
3448
3449 Entering Memory access stage
3450 Mem2Reg=0
3451 Value from ALU is passed to write port of register
    file
3452 Memory access stage completed
3453
3454 Entering writeback stage
```

```
3455 Writeback stage completed
3456
3457
3458
3459 CLOCK CYCLE= 70
3460
3461 Entering fetch stage:
3462 Instruction fetched =
    00100100000010110000000000000001
3463 PC updated to
3464 PC = 000000001000000000000001010000
3465 Fetch stage completed
3466
3467 Entering Decode stage
3468 Opcode=001001
3469 Instruction is decoded as add type instruction(addi
    or addiu)
3470 RS=00000
3471 RT=01011
3472 Immediate value=1
3473
3474 Setting all control Signals
3475 Alusrc:1
3476 Zero_flag:0
3477 MemWr:0
3478 MemRd:0
3479 Mem2Reg:0
3480 jump:0
3481 branch:0
3482 branch_ne:0
3483 PCsrc0
3484 lui:0
3485 Decode stage completed
3486
3487 Entering Execute stage
3488 ALU_ctrl lines: 0 0 1 0
3489 Sign extended value:
    00000000000000000000000000000001
3490 ALU operands:
3491 Operand1=0
3492 Operand2=1
```

```
3493 ALU ADD operation is performed
3494 Execute stage completed
3495
3496 Entering Memory access stage
3497 Mem2Reg=0
3498 Value from ALU is passed to write port of register
    file
3499 Memory access stage completed
3500
3501 Entering writeback stage
3502 RegWr=1
3503 Register file is being written back
3504 Writing back to register number :11
3505 Value written back to register= 1
3506 Writeback stage completed
3507
3508
3509
3510 CLOCK CYCLE= 71
3511
3512 Entering fetch stage:
3513 Instruction fetched =
    00111100000000010001000000000001
3514 PC updated to
3515 PC = 000000001000000000000001010100
3516 Fetch stage completed
3517
3518 Entering Decode stage
3519 Opcode=001111
3520 Instruction is decoded as lui
3521 RS=00000
3522 RT=00001
3523 Immediate value=4097
3524
3525 Setting all control Signals
3526 Alusrc:1
3527 Zero_flag:0
3528 MemWr:0
3529 MemRd:0
3530 Mem2Reg:0
3531 jump:0
```

```
3532 branch:0
3533 branch_ne:0
3534 PCsrc0
3535 lui:1
3536 Decode stage completed
3537
3538 Entering Execute stage
3539 ALU_ctrl lines: 0 0 0 0
3540 LUI instruction executed
3541 Execute stage completed
3542
3543 Entering Memory access stage
3544 Mem2Reg=0
3545 Value from ALU is passed to write port of register
    file
3546 Memory access stage completed
3547
3548 Entering writeback stage
3549 RegWr=1
3550 Register file is being written back
3551 Writing back to register number :1
3552 Value written back to register= 268500992
3553 Writeback stage completed
3554
3555
3556
3557 CLOCK CYCLE= 72
3558
3559 Entering fetch stage:
3560 Instruction fetched =
    101011000010101100000000000100100
3561 PC updated to
3562 PC = 000000001000000000000001011000
3563 Fetch stage completed
3564
3565 Entering Decode stage
3566 Opcode=101011
3567 Instruction is decoded as sw
3568 RS=00001
3569 RT=01011
3570 Immediate value=36
```

```
3571
3572 Setting all control Signals
3573 Alusrc:1
3574 Zero_flag:0
3575 MemWr:1
3576 MemRd:0
3577 Mem2Reg:0
3578 jump:0
3579 branch:0
3580 branch_ne:0
3581 PCsrc0
3582 lui:0
3583 Decode stage completed
3584
3585 Entering Execute stage
3586 ALU_ctrl lines: 0 0 1 0
3587 Sign extended value:
    0000000000000000000000000000100100
3588 ALU operands:
3589 Operand1=268500992
3590 Operand2=36
3591 ALU ADD operation is performed
3592 Execute stage completed
3593
3594 Entering Memory access stage
3595 MemWr=1
3596 Data Memory is being Written
3597 Memory access stage completed
3598
3599 Entering writeback stage
3600 Writeback stage completed
3601
3602
3603
3604 CLOCK CYCLE= 73
3605
3606 Entering fetch stage:
3607 Instruction fetched =
    000010000001000000000000000011110
3608 PC updated to
3609 PC = 00000000100000000000001011100
```

```
3610 Fetch stage completed
3611
3612 Entering Decode stage
3613 Opcode=000010
3614 Instruction is decoded as jump
3615 Jump target address=4194424
3616
3617 Setting all control Signals
3618 Alusrc:0
3619 Zero_flag:0
3620 MemWr:0
3621 MemRd:0
3622 Mem2Reg:0
3623 jump:1
3624 branch:0
3625 branch_ne:0
3626 PCsrc0
3627 lui:0
3628 Decode stage completed
3629
3630 Entering Execute stage
3631 ALU_ctrl lines: 0 0 0 0
3632 Jump instruction executed
3633 Execute stage completed
3634
3635 Entering Memory access stage
3636 Mem2Reg=0
3637 Value from ALU is passed to write port of register
      file
3638 Memory access stage completed
3639
3640 Entering writeback stage
3641 Writeback stage completed
3642
3643
3644 Total clock cycles= 74
3645
3646 RESULT is
3647 Found 1
3648
3649 Process finished with exit code 0
```