Bangladesh University of Engineering and Technology
CSE 209
Computer Architecture Sessional

Assignment-1
4-bit ALU Design

Section A1
Group 01

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1 Introduction

An arithmetic logic unit (ALU) is a multi-operation, combinational-logic digital function. It can perform a set of basic arithmetic operations and a set of logic operations. The ALU has a number of selection lines to select a particular operation in the unit. The selection lines are decoded within the ALU so that k selection variables can specify up to 2^k distinct operations.

Figure 1 shows the block diagram of a 4-bit ALU. The four data inputs from A are combined with the four inputs from B to generate an operation at the F outputs. The mode-select input s_2 distinguishes between arithmetic and logic operations. The two function-select inputs s_1 and s_0 specify the particular arithmetic or logic operation to be generated. With three selection variables, it is possible to specify four arithmetic operations (with s_2 in one state) and four logic operations (with s_2 in the other state). The input and output carries have meaning only during an arithmetic operation. The input carry in the least significant position of an ALU is quite often used as a fourth selection variable that can double the number of arithmetic operations. In this way, it is possible to generate four more operations, for a total of eight arithmetic operations.

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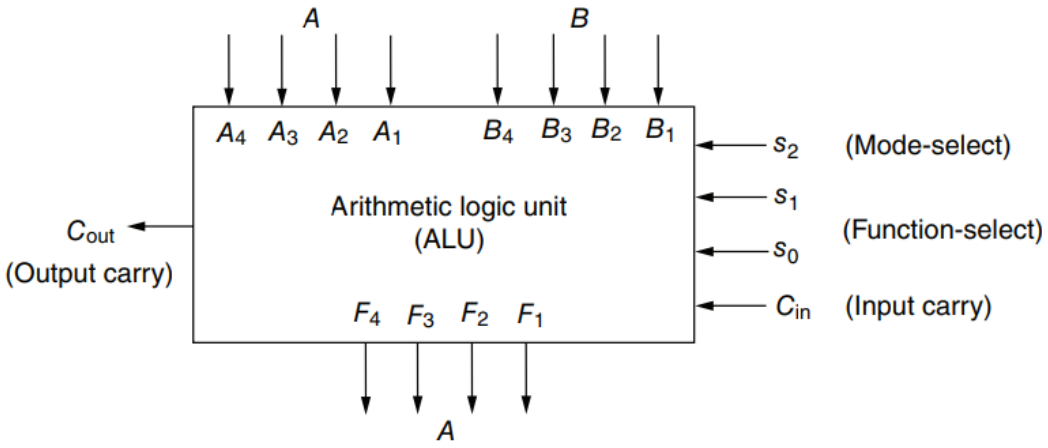

Figure 1: Block Diagram of a 4-bit ALU

The design of a typical ALU will be carried out in three stages. First, the design of the arithmetic section will be undertaken. Second, the design of the logic section will be considered. Finally, the arithmetic section will be modified so that it can perform both arithmetic and logic operations.

There are also 4 status outputs (flags) in ALU. They are denoted by C(Carry Flag), Z(Zero Flag), V(Overflow Flag), S(Sign Flag). Their representations carry out the following meanings:

- C(Carry Flag): This flag is set when there is a carry out of the most significant bit of the result.
- Z(Zero Flag): This flag is set when the result of the operation is zero.
- V(Overflow Flag): This flag is set when the result of the operation is too large to be represented in the given number of bits.
- S(Sign Flag): This flag is set when the result of the operation is negative.

2 Problem Specification with assigned instructions

Design a 4-bit ALU with three selection bits CS2, CS1, CS0 that can perform the following operations:

CS2	**CS1**	**CS0**	**Functions**
0	0	0	Add
0	0	1	AND
0	1	X	Sub with borrow
1	0	0	Complement A
1	0	1	OR
1	1	X	NEG A

Table 1: Control Signals and Functions of the 4-bit ALU

Here, CS2, CS1, and CS0 are the control signals. X means that the value of the signal is not important. The ALU should have 4 status outputs (flags) C, Z, V, S.

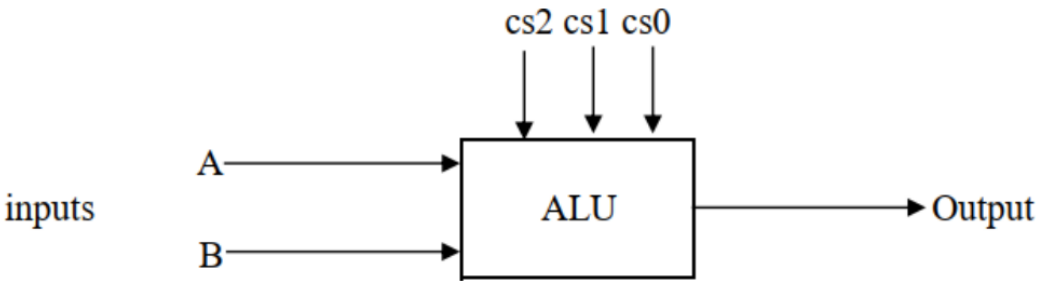

Figure 2: Block Diagram of a 4-bit ALU

3 Detailed design steps with k-maps (if applicable)

4 Truth Table

CS2	CS1	CS0	Functions	X_i	Y_i	Z_i	Cin
0	0	0	Add	A_i	B_i	C_i	0
0	0	1	AND	A_iB_i	0	C_i	0
0	1	X	Sub with borrow	A_i	$\bar{B}_i$	C_i	0
1	0	0	Complement A_i	$\bar{A}_i$	0	C_i	0
1	0	1	OR	A_i+B_i	0	C_i	0
1	1	X	NEG A	$\bar{A}_i$	0	C_i	1

Table 2: Truth Table of X_i, Y_i, Z_i, Cin

CS2	CS1	CS0	Functions	X_i	S11	S10
0	0	0	Add	A_i	0	0
0	0	1	AND	A_iB_i	0	1
0	1	X	Sub with borrow	A_i	0	0
1	0	0	Complement A_i	$\bar{A}_i$	1	0
1	0	1	OR	A_i+B_i	1	1
1	1	X	NEG A	$\bar{A}_i$	1	0

Table 3: Truth Table of MUX input for X_i

CS2	CS1	CS0	Functions	Y_i	S2
0	0	0	Add	B_i	0
0	0	1	AND	0	X
0	1	X	Sub with borrow	$\bar{B}_i$	1
1	0	0	Complement 0	0	X
1	0	1	OR	0	X
1	1	X	NEG A	0	X

Table 4: Truth Table of MUX input for Y_i

5 Block Diagram

6 Complete Circuit Diagram

7 ICs used with count as a chart

IC	Count
74153	2
74157	1
7408	2
7432	2
7404	2
7486	1
7483	2
Total	12

Table 5: ICs used with count

8 The simulator used along with the version number

Logisim - 2.7.1

9 Discussions

10 Contribution of Each Member