ECE 585- FALL 2022

FINAL PROJECT

SIMULATION OF LLC

Portland State UNIVERSITY

GROUP 13

MOUNICA CHAGANTI (mounica@pdx.edu)

ROHITH REDDY MALLEPALLI (rm34@pdx.edu)

GOUTHAM KUMAR REDDY PALEM (goutham2@pdx.edu)

HEMA NAYAKA (hema2@pdx.edu)

FINAL REPORT

Objective:

Simulation of the last level cache (LLC) for a new processor that can be used with up to three other processors in a shared memory configuration.

Design Choices:

Used System Verilog for simulation

Specifications:

Cache total capacity : 16MB
Each line size : 64-byte
Associativity : 8-way
Cache writes hit policy: write back Cache
writes miss policy : write allocate
Replacement policy : Pseudo – LRU
Cache Coherence : MESI Protocol
System maintains inclusivity

Format of trace file contents:

n address
Where n is
0 read request from L1 data cache
1 write request from L1 data cache
2 read request from L1 instruction cache
3 snooped invalidate command
4 snooped read request
5 snooped write request
6 snooped read with intent to modify request
8 clear the cache and reset all state
9 print contents and state of each valid cache line (doesn't end simulation!)

Assumptions

Assume CPU address is 32-bit
Processor's next higher-level cache uses 64-byte lines and is 4 way set associative
For snoop result, assume LSB 2 bits of Byte select to be
00 HIT
01 HITM
10 NO HIT
11 NO HIT

SOURCE CODE:

Cache Package: my_pkg.sv

All the parameterizable variables are defined in this package and can be used anywhere in the project functions.

LLC Cache module: LLC_13

Reads addresses from trace file, performs address Partition to determine Tag, index and Byte Select. Determines hit or miss, while parallelly considering snoop results and performs snoop operations.

TEST PLAN:

1. Simple Hit, Miss Tests

a. Read an address from a trace file; it will be a first compulsory miss.
b. Now, give the same address again to check if it is a hit.
c. Write an address to a cache line, miss!
d. Write again to the same address, now hit.
e. Now change the byte offset of the hit addresses, it will be hit again, since 64 bytes are loaded into cache line.

2.Testing L1 Data cache and Instruction Requests and state change.

a. Read an address from trace file with command 0 or command 2 with LSB bits as 00
b. Give the same address again; it will be hit now. State is shared.
c. Now give another address with LSB bits of byte select 11.
d. Read the same address again, it will be a hit now, the state is Exclusive.
e. Read the above address again, with different byte select, states are not changed. Remains in same state.

3. Testing L1 Cache Write Request:

a. Give a write Request, first miss, State is in Modified.
b. Write to the same address again; the state is still in modified.
c. Read the address again, hit and is in modified state.

4. Testing Snooped Invalidate Command:

a. Give a read command address, it's a miss, so moves to shared or Exclusive depending on byte select LSB bits.
b. Give the same address again, with command 0 or 2, it will be hit.
c. Give the above address, but now with command 4, it will be invalidated.
d. Give the above address, now it will be a miss.
e. Give the write command address, it will be a miss
f. To test if it in modified state, give the read command to the same address.
g. Now give the invalidate command to the same address.
h. Read the address again, it's a miss now.

5. Testing Snoop Results:

a. Give a read command with LSB byte select bits as 11, so moves to exclusive.
b. Now give command 6 to the same address.
c. Read the address, again it will be in invalidated state, it's a miss.
d. Give a write command to a address, it will be in modified state.
e. When snooped a Bus Read request, it will move to shared state, releasing Flush Data to DRAM Bus Operation.
f. Give the Read command with LSB 2 bits as 00, so it will be in shared state.
g. Give Bus Read Command to the same address, it will still be in shared state.
h. Give the bus Read with Intend to Modify to the same address.
i. Read the address, will be a miss, since invalidated above.
j. Again give a write command to a new address will be miss, state is modified.
k. This time snoops a Bus Read with Intend to modify, so moves to invalidate state, while releasing Bus signal "Flush Data to DRAM".
l. Read the above address again, will be a miss since invalidated.
m. Read the same address, changes to shared or Exclusive depending on LSB 2 bits.

6.Testing Working of PLRU:

a. Give 8 address such that they will be filled into a set. (Same index and different tag)
b. Now give another address with same index.
c. way 0 will be evicted.
d. Now read the way 2 address.
e. Give a new address with same index but different tag.
f. way 4 will be evicted.
g. Read way 1 address.
h. Again give a new address with same index and different tag. Way 6 will be evicted.

7. Testing mode 8 and mode 9:

a. Give a set of addresses with different commands
b. Give any address with command 9, see if the contents of caches along with valid states is printed except(invalid)
c. To clear the cache, give command 8.
d. To see if they are cleared, give command 9 again, nothing should be displayed now.