Sai Govardhan

As a B.Tech ECE senior at PESU, I have proven experience in ASIC Design and FPGA Prototyping, backed by my multiple internships and projects. With Teaching Assistant roles for three core subjects, eight Cadence Badges, and a VLSI Specialization, I have a robust foundation in this domain.
I am passionate about building efficient Hardware Accelerators and RISC-V Processor Architectures.

CONTACT INFORMATION

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EDUCATION

Bachelor of Technology in Electronics and Communication Engineering, 2019 – 2023
PES University, RR Campus, Bangalore
VLSI Specialisation (NiCE Domain) | Current CGPA: 7.59 up to VII semester

EXPERIENCE

VLSI Design Intern, Jan 2023 – present
International Institute of Information Technology, Bangalore
Working on the digital design and theoretical modelling of the Ganaka Architecture under the supervision of Dr. G N Srinivasa Prasanna.

Hardware Accelerator Research Intern, Jan 2023 – present
Centre for Innovation and Entrepreneurship, PES University
Researched and implemented architectures for Hardware Acceleration on the Intel Cyclone DE10 FPGA board under the guidance of Prof. Sathya Prasad.
Currently preparing a workshop for the summer. [GitHub: **DE10_FPGA**]

Electronics Research Intern, Sept 2022 – Dec 2022
OrbitAID Aerospace, Indian Institute of Science, Bangalore
(Work bound by Non-Disclosure Agreement)

Project Intern - FarmBot, June 2021 – Oct 2021
Center for Internet of Things, PES University
Was the ECE domain in-charge of the farming automation bot which used CNC principles for watering and detecting plants. [GitHub: **farmbot-pesu**]

PROJECTS

Fault Tolerant RISC-V Processor Design 2023 - present
Leading a Fault Tolerant RISC-V Processor team designing novel fault correction techniques using approximate computing and submodule level hardware redundancy.
Advisor: Dr. Rashmi Seethur

Low Power Hardware Accelerator for Multidimensional Data Sorting 2022 - 2023
Designed novel multi-dimensional hardware sorting architectures to provide efficient sorting of data, and analysed them with their low power variants using index sorting and clock gating (Total of 14 implementations at 50MHz). Verification done using SystemVerilog Layered Testbench with 100 iterations for each implementation.
[GitHub: **Low_Power_Multidimensional_Sorters**] | Advisor: Dr. Sudeendra Kumar K

Other Projects on GitHub:
[RISC_V_Single_Cycle_Processor] [RISC_V_Assembly_Programs] [SPEC_CPU_2017]

PUBLICATIONS

Low Power Multidimensional Sorters using Clock Gating and Index Sorting
Samahith S A, **Sai Govardhan,** Manogna R, Hitesh D, Dr. Sudeendra Kumar K
(Accepted by IEEE CONECCT 2023)

TEACHING EXPERIENCE

Student Teaching Assistant,
PES University

- **Embedded Firmware Development with UEFI** 2023
  Demonstrated the UEFI shell basics on QEMU using TianoCore's EDKII platform.
  [GitHub: **UEFI_AHP**] | Advisor: Dr. Sudeendra Kumar K

- **Synthesis, Physical Design and Timing Analysis of Digital Circuits** 2023
  Implemented HDL to Floorplan demos on the Mentor Oasys tool, and guided analysis on physical design characteristics and timing analysis.
  [Manual: **bit.ly/mentorlabpesu**] | Advisor: Dr. Sudeendra Kumar K

- **Digital System Design** 2022
  Was responsible for implementing Advanced Digital Design concepts on the Cadence Tools from RTL to GDSII, with hands-on projects for 190+ students.
  [GitHub: **DSD_AHP**] [Manual: **bit.ly/cadencelabpesu**] |Advisor: Dr. Rashmi Seethur

SKILLS

Digital Design (ASIC Design and FPGA Prototyping), Static Timing Analysis, Synthesis, Equivalence Checking
Verification: Functional and Formal Verification (Assertions), Coverage
Computer Architecture (RISC-V)
Programming Languages: Verilog, SystemVerilog, C Programming, Python
Tools: Cadence (NCSim, Genus, Tempus, Incisive Metrics Center, Conformal LEC), Mentor (Oasys, QuestaSim), Xilinx Vivado, Intel Quartus Prime
Benchmarking: SPEC CPU 2017

CERTIFICATIONS

NPTEL Online Certification

- Advanced Computer Architecture (**Link to Certificate**)

Cadence Digital Badge Programme
(Link to all badges: **http://www.credly.com/users/sai-govardhan/badges**)

- Genus Synthesis Solution with Stylus Common UI v21.1
- Low-Power Synthesis Flow with Genus Stylus Common UI v21.1
- Conformal Equivalence Checking v22.1
- Basic Static Timing Analysis v2.0
- Tempus Signoff Timing Analysis and Closure v21.1
- Fundamentals of IEEE 1801 Low-Power Specification Format v8.0
- Cadence RTL-to-GDSII Flow v4.0
- Joules Power Calculator v21.1

AWARDS

Won 2nd place at the Hackezee Hackathon, 2021
For the project- Gesture Controlled Rescue Vehicle in the electronics hackathon organized by the ECE Department PESU.

Won 3rd place at the Gutsy Entrepreneur 2.0 Contest, 2020
For the EmoBuild (Emotional Intelligence – Build Platform) business idea and prototype app design at the flagship hackathon organized by CIE PESU.

Won 2nd place at Pioneer, 2020
The Business Modelling Contest, by presenting creative strategies for existing businesses navigating the pandemic, in an event organized by CIE PESU.

Distinction Awards for the I, II, V, VI and VII semesters at PESU 2019 – 2023

Won the Most Disciplined Outgoing Student award, 2017
At Presidency School, Nandini Layout.