

Sai Govardhan



I'm a B.Tech ECE senior at PES University, Bangalore, with a VLSI specialization and a passion for Digital Design, Verification and Computer Architecture.

CONTACT INFORMATION	saigov14@gmail.com saigovardhanmc@pesu.pes.edu +91 6360222109	github.com/govardhnn linkedin.com/in/saigovardhan govardhnn.github.io
EDUCATION	B.Tech in Electronics and Communication Engineering, <i>PES University, RR Campus, Bangalore</i> VLSI Specialisation (NiCE Domain) 7.59 CGPA upto VII SEM	2019 – 2023
EXPERIENCE	VLSI Design Intern, <i>International Institute of Information Technology, Bangalore</i> Working under Dr. G N Srinivasa Prasanna on the Ganaka Architecture and I'm part of the Neuromorphic Computing research group.	Jan 2023 – present
	Research Intern (Hardware Acceleration), <i>Centre for Innovation and Entrepreneurship, PES University</i> Implemented Architectures for Hardware Acceleration on the Intel Cyclone DE10 FPGA board under the guidance of Prof. Sathya Prasad. [GitHub: DE10 FPGA]	Jan 2023 – present
	Electronics Intern, <i>OrbitAID Aerospace, Indian Institute of Science, Bangalore</i> (Work bound by Non-Disclosure Agreement)	Sept 2022 – Dec 2022
	Project Intern - FarmBot, <i>Center for Internet of Things, PES University</i> Was the ECE domain in-charge of the farming automation bot which used CNC principles for watering and detecting plants. [GitHub: farmbot-pesu]	June 2021 – Oct 2021
PROJECTS	Fault Tolerant RISC-V Processor Design Guiding a Fault Tolerant RISC-V Processor team designing novel fault correction techniques using approximate computing and submodule level hardware redundancy. Advisor: Dr. Rashmi Seethur	2023 - present
	Low Power Hardware Accelerator for Multidimensional Data Sorting Designed novel multi-dimensional hardware sorting architectures to provide efficient sorting of data, and analysed them with their low power variants using index sorting and clock gating (Total of 14 implementations at 50MHz). Verification done using SystemVerilog Layered Testbench with 98% coverage. [GitHub: Low Power Multidimensional Sorters] Advisor: Dr. Sudeendra Kumar K	2022 - 2023
	Other Projects on GitHub: [RISC V Single Cycle Processor] [RISC V Assembly Programs] [SPEC CPU 2017]	
PUBLICATIONS	Low Power Multidimensional Sorters using Clock Gating and Index Sorting Samahith S A, Sai Govardhan, Manogna R, Hitesh D, Dr. Sudeendra Kumar K (Accepted by IEEE CONECCT)	
TEACHING EXPERIENCE	Student Teaching Assistant, <i>PES University</i> <ul style="list-style-type: none">Embedded Firmware Development with UEFI Used TianoCore's EDKII platform to demonstrate the UEFI shell basics on QEMU. [GitHub: UEFI AHP] Advisor: Dr. Sudeendra Kumar K	2023

- Synthesis, Physical Design and Timing Analysis of Digital Circuits** 2023
 Implemented HDL to Floorplan demos on the Mentor Oasys tool, and guided analysis on physical design characteristics and timing analysis.
 [Manual: bit.ly/mentorlabpesu] | Advisor: Dr. Sudeendra Kumar K
- Digital System Design** 2022
 Was responsible for implementing Advanced Digital Design concepts on the Cadence Tools from RTL to GDSII, with hands-on projects for 190+ students.
 [GitHub: [DSD_AHP](https://github.com/DSD-AHP)] [Manual: bit.ly/cadencelabpesu] | Advisor: Dr. Rashmi Seethur

SKILLS

Digital Design (ASIC Design and FPGA Prototyping), Static Timing Analysis, Synthesis, Equivalence Checking,
Verification: Functional and Formal Verification (Assertions), Coverage
Computer Architecture (RISC-V)
Programming Languages: Verilog, SystemVerilog, C Programming, Python.
Tools: Cadence (NCSim, Genus, Tempus, Incisive Metrics Center, Conformal LEC), Mentor (Oasys, QuestaSim), Xilinx Vivado, Intel Quartus Prime.
Benchmarking: SPEC CPU 2017

CERTIFICATIONS

NPTEL Online Certification

- Advanced Computer Architecture ([Link to Certificate](#))

Cadence Digital Badge Programme
 (Link to all badges: <http://www.credly.com/users/sai-govardhan/badges>)

- Genus Synthesis Solution with Stylus Common UI v21.1
- Low-Power Synthesis Flow with Genus Stylus Common UI v21.1
- Conformal Equivalence Checking v22.1
- Basic Static Timing Analysis v2.0
- Tempus Signoff Timing Analysis and Closure v21.1
- Fundamentals of IEEE 1801 Low-Power Specification Format v8.0
- Cadence RTL-to-GDSII Flow v4.0
- Joules Power Calculator v21.1

AWARDS

Won 2nd place at the Hackezee Hackathon, 2021
 For the project- Gesture Controlled Rescue Vehicle in the electronics hackathon organized by the ECE Department PESU.

Won 3rd place at the Gutsy Entrepreneur 2.0 Contest, 2020
 For the EmoBuild (Emotional Intelligence – Build Platform) business idea, in the hackathon organized by CIE PESU.

Won 2nd place at Pioneer, 2020
 The Business Modelling Contest organized by CIE PESU

Distinction Awards for the I, II, V, VI and VII semesters 2019 – 2023

Won the Most Disciplined Outgoing Student award, 2017
Presidency School, Nandini Layout.