Sai Govardhan

Research Interests	Digital Design (ASIC Design and FPGA Prototyping) Computer Architecture (RISC-V)	
Contact Information	saigov14@gmail.com govardhnn.github.io	linkedin.com/in/saigovardhan github.com/govardhnn

Education

B.Tech in Electronics and Communication Engineering 2019 - 2023
PES University, Bangalore
- VLSI Specialization
- CGPA: 7.71/10, Capstone: 10/10

Experience

CPU Design and Verification Intern July 2023 - Present
InCore Semiconductors, Chennai

VLSI Design Intern
International Institute of Information Technology, Bangalore Jan 2023 – June 2023

Hardware Accelerator Research Intern
Centre for Innovation and Entrepreneurship, PES University Jan 2023 – June 2023

Electronics Research Intern
OrbitAID Aerospace, Indian Institute of Science, Bangalore Sept 2022 – Dec 2022

Project Intern - FarmBot
Center for Internet of Things, PES University June 2021 – Oct 2021

Teaching

Embedded Firmware Development with UEFI
Student Teaching Assistant, PES University

Synthesis, Physical Design and Timing Analysis of Digital Circuits
Student Teaching Assistant, PES University

Digital System Design
Student Teaching Assistant, PES University

Publications

Low Power Multidimensional Sorters using Clock Gating and Index Sorting
Samahith S A, **Sai Govardhan**, *Manogna R, Hitesh D, Dr. Sudeendra Kumar K*
In the IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), July 2023
[Paper Link]

Skills

Projects

Certifications

Advanced Computer Architecture
NPTEL Online Certification

Genus Synthesis Solution with Stylus Common UI v21.1
Cadence Digital Badge Programme **[Credly Link]**

Low-Power Synthesis Flow with Genus Stylus Common UI v21.1 date
Cadence Digital Badge Programme [**Credly Link**]

Conformal Equivalence Checking v22.1 date
Cadence Digital Badge Programme [**Credly Link**]

Basic Static Timing Analysis v2.0 date
Cadence Digital Badge Programme [**Credly Link**]

Tempus Signoff Timing Analysis and Closure v21.1 date
Cadence Digital Badge Programme [**Credly Link**]

Fundamentals of IEEE 1801 Low-Power Specification Format v8.0 date
Cadence Digital Badge Programme [**Credly Link**]

Cadence RTL-to-GDSII Flow v4.0 date
Cadence Digital Badge Programme [**Credly Link**]

Joules Power Calculator v21.1 date
Cadence Digital Badge Programme

Awards

award date
by

award date
by