Sai Govardhan

Research Interests	Digital Design (ASIC Design and FPGA Prototyping) Computer Architecture (RISC-V)	
Contact Information	saigov14@gmail.com govardhnn.github.io	linkedin.com/in/saigovardhan github.com/govardhnn

Education

B.Tech in Electronics and Communication Engineering 2019 - 2023
PES University, Bangalore

- VLSI Specialization
- CGPA: 7.71/10, Capstone: 10/10

Experience

CPU Design and Verification Intern July 2023 - Present
InCore Semiconductors, Chennai

VLSI Design Intern Jan 2023 – June 2023
International Institute of Information Technology, Bangalore

Hardware Accelerator Research Intern Jan 2023 – June 2023
Centre for Innovation and Entrepreneurship, PES University

Electronics Research Intern Sept 2022 – Dec 2022
OrbitAID Aerospace, Indian Institute of Science, Bangalore

Project Intern - FarmBot June 2021 – Sept 2021
Center for Internet of Things, PES University

Teaching

Embedded Firmware Development with UEFI
Student Teaching Assistant, PES University

Synthesis, Physical Design and Timing Analysis of Digital Circuits
Student Teaching Assistant, PES University

Digital System Design
Student Teaching Assistant, PES University

Publications

Low Power Multidimensional Sorters using Clock Gating and Index Sorting
Samahith S A, **Sai Govardhan***, Manogna R, Hitesh D, Dr. Sudeendra Kumar K*
In the IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), July 2023 [**Paper Link**]

Certifications

Advanced Computer Architecture
NPTEL Online Certification

Genus Synthesis Solution with Stylus Common UI v21.1
Cadence Digital Badge Programme [**Credly Link**]

Low-Power Synthesis Flow with Genus Stylus Common UI v21.1
Cadence Digital Badge Programme [**Credly Link**]

Conformal Equivalence Checking v22.1
Cadence Digital Badge Programme [**Credly Link**]

Basic Static Timing Analysis v2.0
Cadence Digital Badge Programme [**Credly Link**]

Tempus Signoff Timing Analysis and Closure v21.1
Cadence Digital Badge Programme [**Credly Link**]

Fundamentals of IEEE 1801 Low-Power Specification Format v8.0
Cadence Digital Badge Programme [**Credly Link**]

Cadence RTL-to-GDSII Flow v4.0
Cadence Digital Badge Programme [**Credly Link**]

Joules Power Calculator v21.1
Cadence Digital Badge Programme [**Credly Link**]

Awards

Won the Certificate of Appreciation
Was one of the six recipients of the appreciation award for the graduating batch of BTech ECE at PES University, for my contributions to the VLSI Domain

Won 2nd place at the Hackezee Hackathon
For the IoT and sensors project- 'Gesture Controlled Rescue Vehicle' in the flagship hackathon organized by the ECE Department PESU

Won 3rd place at the Gutsy Entrepreneur 2.0 Contest
For the EmoBuild (Emotional Intelligence - Build Platform) business idea and prototype app design at the 14-day hackathon organized by CIE PESU

Won 2nd place at Pioneer
The Business Modelling Contest, by presenting creative strategies for existing businesses navigating the pandemic, in an event organized by CIE PESU

Distinction Awards for the I, II, V and VI semesters
by the ECE Department, PES University

Won the Most Disciplined Outgoing Student award
at Presidency School, Nandini Layout