

# Sai Govardhan

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## CONTACT INFORMATION

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## EDUCATION

**B.Tech in Electronics and Communication Engineering** 2019 - 2023  
*PES University, Bangalore*

- VLSI Specialization
- Thesis: Low Power Multidimensional Hardware Sorting Accelerator  
Advisor: Dr. Sudeendra Kumar K.

## EXPERIENCE

**CPU Design Engineer - II** April 2025 – Present  
**CPU Design Engineer - I** Nov 2023 – March 2025  
*InCore Semiconductors, Bangalore*

- MultiCore Cache Subsystem Design (Sept 2024 - Present)
  - Mid Level and Last Level Cache microarch specification and BSV Design
  - Tilelink to AXI4 Bridge Design
  - Unit Level Bluecheck verification setupAdvisors: Niraj Sharma and Gautam Doshi
- Tapeout contribution to In-Tst-1/In-SoC-2 on TSMC 40LP (Jan - Aug 2024)
  - RTL Linting and CDC, ASIC Synthesis, Logical Equivalence Checking,
  - SRAM and ROM Generation and Integration.Advisor: Arjun Menon
- PinMux Design for InCore SoCs (Nov - Dec 2024)  
Advisor: Niraj Sharma

**RTL Design Intern** July 2023 – Oct 2023  
*InCore Semiconductors, Chennai*

- RISC-V CPU Extension Retiming - Azurite  
Advisors: Babu P.S. and Neel Gala

**VLSI Design Intern** Jan 2023 – June 2023  
*International Institute of Information Technology, Bangalore*

- Ganaka Computer Architecture Performance Modelling  
Dr. G. N. Srinivasa Prasanna

**Hardware Accelerator Research Intern** Jan 2023 – June 2023  
*Centre for Innovation and Entrepreneurship, PES University*

- Implementation of Architectures for Hardware Acceleration on the Intel Cyclone DE10 FPGA
- FPGA Track Lead for the CIE Summer Workshop  
Prof. Sathya Prasad

**Electronics Research Intern** Sept 2022 – Dec 2022  
*OrbitAID Aerospace, Indian Institute of Science, Bangalore*

- Research topic: On Orbit Servicing of Space System Architectures  
Advisor: Sakthikumar R.

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|              | <b>Project Intern</b> <span style="float: right;">June 2021 – Sept 2021</span><br><i>Center for Internet of Things, PES University</i> <ul style="list-style-type: none"> <li>Farmbot</li> </ul> <p style="text-align: center;">ECE domain in-charge of the farming automation IOT project</p>  |
| TEACHING     | <b>Embedded Firmware Development with UEFI [GitHub Link]</b><br><i>Student Teaching Assistant, PES University</i> <ul style="list-style-type: none"> <li>Demonstration of the UEFI shell basics on QEMU using TianoCore's EDKII platform.</li> </ul> <p style="text-align: center;">Advisor: Dr. Sudeendra Kumar K.</p><br><b>Synthesis, Physical Design and Timing Analysis of Digital Circuits [Manual]</b><br><i>Student Teaching Assistant, PES University</i> <ul style="list-style-type: none"> <li>Implementation of RTL to Floorplan demos on the Mentor Oasys tool, and analysis of physical design characteristics and timing analysis.</li> </ul> <p style="text-align: center;">Advisor: Dr. Sudeendra Kumar K.</p><br><b>Digital System Design [GitHub Link] [Manual]</b><br><i>Student Teaching Assistant, PES University</i> <ul style="list-style-type: none"> <li>Hands-on Advanced Digital Design Projects on Cadence Tools from RTL to GDSII, for 190+ students.</li> </ul> <p style="text-align: center;">Advisor: Dr. Rashmi Seethur</p> |
| PUBLICATIONS | <b>Low Power Multidimensional Sorters using Clock Gating and Index Sorting</b><br><i>Samahith S A, Sai Govardhan, Manogna R, Hitesh D, Dr. Sudeendra Kumar K</i><br><b>Nominated for the best paper award</b> in the <i>IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), July 2023.</i><br><b>[Paper Link]</b>   |
| SKILLS       | <b>Digital Design:</b> RTL Linting and CDC, Synthesis, Static Timing Analysis, Logical Equivalence Checking, Gate Level Simulation, SRAM and ROM generation<br><b>Computer Architecture:</b> RISC-V ISA implementation, Cache Coherence<br><b>CPU Benchmarking:</b> Coremarks, Dhrystone, Whetstone, SPEC CPU 2017<br><b>Verification:</b> Functional and Formal Verification (Assertions)<br><b>Hardware Description Languages:</b> Bluespec SystemVerilog, Verilog<br><b>Imperative Programming Languages:</b> C, C++<br><b>Scripting Languages:</b> Python, TCL and Bash<br><b>EDA Tools:</b> Cadence (Xcelium, Genus, Conformal LEC, Tempus, Incisive Metrics Center),<br>Synopsys(Spyglass), Mentor(QuartaSim, Oasys), Xilinx(Vivado), Intel(Quartus Prime), TSMC(Memory Compilers), Verilator   |
| WORKSHOPS    | <b>CIE Summer Workshop</b> <span style="float: right;">March 2023 - June 2023</span><br><i>PES University, RR Campus, Bangalore</i><br>Was the FPGA Track lead of the CIE Summer workshop, which involved guiding four teams for four weeks on the fundamentals of mapping and implementing algorithms to hardware architectures on the Intel DE-10 FPGA Board. <b>[GitHub Link]</b><br><br><b>CIOT Workshop</b> <span style="float: right;">October 2021</span><br><i>PES University, RR Campus, Bangalore</i><br>Presented the Farmbot project in which I was the electronics lead, and trained students with IOT fundamentals using dev-kits for two days. <b>[GitHub Link]</b>  |

## CERTIFICATIONS

### **Advanced Computer Architecture**

*NPTEL Online Certification* [[Certificate Link](#)]

### **Genus Synthesis Solution with Stylus Common UI v21.1**

*Cadence Digital Badge Programme* [[Credly Link](#)]

### **Low-Power Synthesis Flow with Genus Stylus Common UI v21.1**

*Cadence Digital Badge Programme* [[Credly Link](#)]

### **Conformal Equivalence Checking v22.1**

*Cadence Digital Badge Programme* [[Credly Link](#)]

### **Basic Static Timing Analysis v2.0**

*Cadence Digital Badge Programme* [[Credly Link](#)]

### **Tempus Signoff Timing Analysis and Closure v21.1**

*Cadence Digital Badge Programme* [[Credly Link](#)]

### **Fundamentals of IEEE 1801 Low-Power Specification Format v8.0**

*Cadence Digital Badge Programme* [[Credly Link](#)]

### **Cadence RTL-to-GDSII Flow v4.0**

*Cadence Digital Badge Programme* [[Credly Link](#)]

### **Joules Power Calculator v21.1**

*Cadence Digital Badge Programme* [[Credly Link](#)]

## AWARDS

### **Won the Certificate of Appreciation**

*Was one of the six recipients of the appreciation award for the graduating batch of BTech ECE at PES University, for my contributions to the VLSI Domain*

### **Won 2nd place at the Hackezee Hackathon**

*For the IoT and sensors project- ‘Gesture Controlled Rescue Vehicle’ in the flagship hackathon organized by the ECE Department PESU*

### **Won 3rd place at the Gutsy Entrepreneur 2.0 Contest**

*For the EmoBuild (Emotional Intelligence - Build Platform) business idea and prototype app design at the 14-day hackathon organized by CIE PESU*

### **Won 2nd place at Pioneer**

*The Business Modelling Contest, by presenting creative strategies for existing businesses navigating the pandemic, in an event organized by CIE PESU*

### **Distinction Awards for the I, II, V and VI semesters**

*by the ECE Department, PES University*

### **Won the Most Disciplined Outgoing Student award**

*at Presidency School, Nandini Layout*