Sai Govardhan

As a B.Tech ECE graduate from PES University, I have proven expertise in ASIC Design and FPGA Prototyping, backed by my coursework, internships (at IIITB, CIE-PESU, OrbitAID-IISC), and projects. With Teaching Assistant experience for three core subjects, eight Cadence Digital Badges for the 'Digital Design and Signoff' track, and a VLSI Specialization, I have a robust foundation in this domain. I am passionate about building efficient Hardware Accelerators and Processor µArchitectures.

CONTACT INFORMATION

saigov14@gmail.com
saigovardhanmc@pesu.pes.edu
+91 6360222109
github.com/govardhnn
linkedin.com/in/saigovardhan
govardhnn.github.io

EDUCATION

Bachelor of Technology in Electronics and Communication Engineering, 2019 – 2023
PES University, RR Campus, Bangalore
VLSI Specialisation (NiCE Domain) | CGPA: 7.71 | Capstone: 10

EXPERIENCE

VLSI Design Intern, Jan 2023 – June 2023
International Institute of Information Technology (CSL Lab - Gyanalakshmi), Bangalore
Worked on modelling the Novel Ganaka Architecture using Valgrind on the SPEC CPU 2017 benchmarks, under the guidance of Dr. G N Srinivasa Prasanna.

Hardware Accelerator Research Intern, Jan 2023 – June 2023
Centre for Innovation and Entrepreneurship, PES University
Researched and implemented Hardware Accelerators on the Intel Cyclone DE10 FPGA board under the supervision of Prof. Sathya Prasad.
Currently mentoring the FPGA track of the summer workshop. [GitHub: DE10_FPGA]

Electronics Research Intern, Sept 2022 – Dec 2022
OrbitAID Aerospace, Indian Institute of Science, Bangalore
(Work bound by Non-Disclosure Agreement)

Project Intern - FarmBot, June 2021 – Oct 2021
Center for Internet of Things, PES University
Was the ECE domain in-charge of the farming automation bot which used CNC principles for watering and detecting plants. [GitHub: farmbot-pesu]

PROJECTS

Fault Tolerant RISC-V Processor Design 2023 - present
Leading a Fault Tolerant RISC-V Processor team designing fault detection and correction techniques using submodule level hardware redundancy.
Advisor: Dr. Rashmi Seethur

Low Power Hardware Accelerator for Multidimensional Data Sorting 2022 - 2023
Designed novel multi-dimensional hardware sorting architectures to provide efficient sorting of data, and analysed them with their low power variants using index sorting and clock gating (Total 12 implementations at 50MHz, upto 68.56% power reduction). Functional Verification done using a SystemVerilog Layered Testbench.
Advisor: Dr. Sudeendra Kumar K

Other Projects on GitHub:
[RISC_V_Single_Cycle_Processor][RISC_V_Assembly_Programs][SPEC_CPU_2017]

PUBLICATIONS

Low Power Multidimensional Sorters using Clock Gating and Index Sorting
Samahith S A, **Sai Govardhan,** Manogna R, Hitesh D, Dr. Sudeendra Kumar K
(Accepted by IEEE CONECCT 2023)

TEACHING EXPERIENCE

Student Teaching Assistant,
PES University

- **Embedded Firmware Development with UEFI** 2023
  Demonstrated the UEFI shell commands by emulating TianoCore's EDKII on QEMU.
  [GitHub: **UEFI_AHP**] | Advisor: Dr. Sudeendra Kumar K

- **Synthesis, Physical Design and Timing Analysis of Digital Circuits** 2023
  Implemented HDL to Floorplan demos on the Mentor Oasys tool.
  [Manual: **bit.ly/mentorlabpesu**] | Advisor: Dr. Sudeendra Kumar K

- **Digital System Design** 2022
  Was responsible for implementing ASIC Design concepts from the course onto the Cadence Tools. Provided and evaluated hands-on projects for 190+ students.
  [GitHub: **DSD_AHP**] [Manual: **bit.ly/cadencelabpesu**] |Advisor: Dr. Rashmi Seethur

SKILLS

Digital Design (ASIC Design and FPGA Prototyping), Static Timing Analysis, Synthesis, Equivalence Checking
Verification: Functional and Formal Verification (Assertions), Coverage
Computer Architecture (RISC-V)
Programming Languages: Verilog, SystemVerilog, C Programming, Python
Tools: Cadence (NCSim, Genus, Tempus, Incisive Metrics Center, Conformal LEC), Mentor (Oasys, QuestaSim), Xilinx Vivado, Intel Quartus Prime
Benchmarking: SPEC CPU 2017

CERTIFICATIONS

NPTEL Online Certification

- Advanced Computer Architecture (**Link to Certificate**)

Cadence Digital Badge Programme
(Link to all badges: **http://www.credly.com/users/sai-govardhan/badges**)

- Genus Synthesis Solution with Stylus Common UI v21.1
- Low-Power Synthesis Flow with Genus Stylus Common UI v21.1
- Conformal Equivalence Checking v22.1
- Basic Static Timing Analysis v2.0
- Tempus Signoff Timing Analysis and Closure v21.1
- Fundamentals of IEEE 1801 Low-Power Specification Format v8.0
- Cadence RTL-to-GDSII Flow v4.0
- Joules Power Calculator v21.1

AWARDS

Won the Certificate of Appreciation – ECE Department, PESU 2023
Was one of the six recipients of the appreciation award for the graduating batch of B.Tech ECE at PES University, for my contributions to the VLSI Domain.

Won 2nd place at the Hackezee Hackathon, 2021
For the project- Gesture Controlled Rescue Vehicle in the electronics hackathon organized by the ECE Department PESU.

Won 3rd place at the Gutsy Entrepreneur 2.0 Contest, 2020
For the EmoBuild (Emotional Intelligence – Build Platform) business idea and prototype app design at the flagship hackathon organized by CIE PESU.

Won 2nd place at Pioneer, 2020
The Business Modelling Contest, by presenting creative strategies for existing businesses navigating the pandemic, in an event organized by CIE PESU.

Distinction Awards for the I, II, V, VI, VII and VIII semesters at PESU 2019 – 2023

Won the Most Disciplined Outgoing Student award, 2017
At Presidency School, Nandini Layout.

Last updated: 18th June, 2023