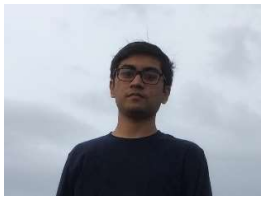
Sai Govardhan



I'm a B.Tech ECE senior at PES University, Bangalore, with a VLSI specialization and a passion for Digital Design and Computer Architecture.

CONTACT INFORMATION

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EDUCATION

B.Tech in Electronics and Communication Engineering, 2019 – 2023
PES University, RR Campus, Bangalore
VLSI Specialisation (NiCE Domain)

EXPERIENCE

VLSI Design Intern, Jan 2023 – present
International Institute of Information Technology, Bangalore
Working under Dr. G N Srinivasa Prasanna on VLSI Design, Benchmarking, Neuromorphic Computing, at the Computational Sciences Labs (Ganaka), IIITB.
[GitHub: Neuromorphic_designs, SPEC_CPU_2017, MLPerf]

AI Hardware Research Intern, Jan 2023 – April 2023
Centre for Innovation and Entrepreneurship, PES University
Implemented Architectures for Hardware Acceleration on the Intel Cyclone DE10 board's FPGA and SOC under the guidance of Prof. Sathya Prasad.
[GitHub: DE10_FPGA]

Hardware Intern, Sept 2022 – Dec 2022
OrbitAID Aerospace, Indian Institute of Science, Bangalore
(Work bound by Non-Disclosure Agreement)

Project Intern - FarmBot, June 2021 – Oct 2021
Center for Internet of Things, PES University
Was the Electronics domain in-charge of the farming automation bot which used CNC principles for watering and detecting plants and weed.
[GitHub: farmbot-pesu]
Conducted an IoT Workshop and guided the next batch of interns.

PROJECTS

Fault Tolerant RISC-V Processor Design (ongoing) 2023
Guiding a Fault Tolerant RISC-V Processor team designing novel fault correction techniques using hardware redundancy in various submodules.
Advisor: Dr. Rashmi Seethur

Low Power Hardware Accelerator for Data Sorting 2022
Designed novel multi-dimensional hardware sorting architectures to provide efficient sorting of data, and analysed them with their low power variants using index sorting and clock gating (Total of 14 implementations at 50MHz).
Advisor: Dr. Sudeendra Kumar K

Other Projects (on GitHub)
[RISC_V_Single_Cycle_Processor][RISC_V_Assembly_Programs]
[VeriRiscCPU][Verification]

PUBLICATIONS

Low Power Multidimensional Sorters using Clock Gating and Index Sorting
(Submitted to IEEE CONECCT)

TEACHING EXPERIENCE

Student Teaching Assistant,
PES University

- **Embedded Firmware Development with UEFI** 2023
  Used TianoCore's EDKII platform to demonstrate the UEFI shell basics on QEMU.
  [GitHub: **UEFI_AHP**]
  Advisor: Dr. Sudeendra Kumar K

- **Synthesis, Physical Design and Timing Analysis of Digital Circuits** 2023
  Implemented HDL to Floorplan demos on the Mentor Oasys tool, and guided analysis on physical design characteristics and timing analysis.
  [Manual: **bit.ly/mentorlabpesu**]
  Advisor: Dr. Sudeendra Kumar K

- **Digital System Design** 2022
  Was responsible for implementing Advanced Digital Design concepts on the Cadence Tools from RTL to GDSII, with hands-on projects for 190+ students.
  [GitHub: **DSD_AHP**] [Manual: **bit.ly/cadencelabpesu**]
  Advisor: Dr. Rashmi Seethur

SKILLS

Digital Design (ASIC Design and FPGA Prototyping), Static Timing Analysis, Synthesis, Equivalence Checking, Functional and Formal Verification (Assertions), Coverage
Computer Architecture (RISC-V), Hardware Security, IoT.
Programming Languages: Verilog, System Verilog, RISC-V Assembly, C Programming, Python.
Tools: Cadence (NCSim, Genus, Tempus, Incisive Metrics Center, Conformal LEC, IFV), Mentor (Oasys, QuestaSim), Xilinx Vivado, Intel Quartus Prime.
Benchmarking: SPEC CPU 2017, MLPerf.

CERTIFICATIONS

Cadence Digital Badge Programme
(Credly Link: **http://www.credly.com/users/sai-govardhan/badges**)

- Genus Synthesis Solution with Stylus Common UI v21.1
- Low-Power Synthesis Flow with Genus Stylus Common UI v21.1
- Conformal Equivalence Checking v22.1
- Basic Static Timing Analysis v2.0
- Tempus Signoff Timing Analysis and Closure v21.1
- Fundamentals of IEEE 1801 Low-Power Specification Format v8.0
- Cadence RTL-to-GDSII Flow v4.0
- Joules Power Calculator v21.1

AWARDS

Won 2nd place at the Hackezee Hackathon, 2021
For the project- Gesture Controlled Rescue Vehicle in the electronics hackathon organized by the ECE Department PESU.

Won 3rd place at the Gutsy Entrepreneur 2.0 Contest, 2020
For the EmoBuild business idea, in the hackathon organized by CIE PESU.

Won 2nd place at Pioneer, 2020
The Business Modelling Contest organized by CIE PESU

Distinction Awards for the I, II, V, VII and VII semesters 2019 – 2023

Won the Most Disciplined Outgoing Student award, 2017
Presidency School, Nandini Layout.

LANGUAGES

English, Kannada, Telugu, and Hindi.