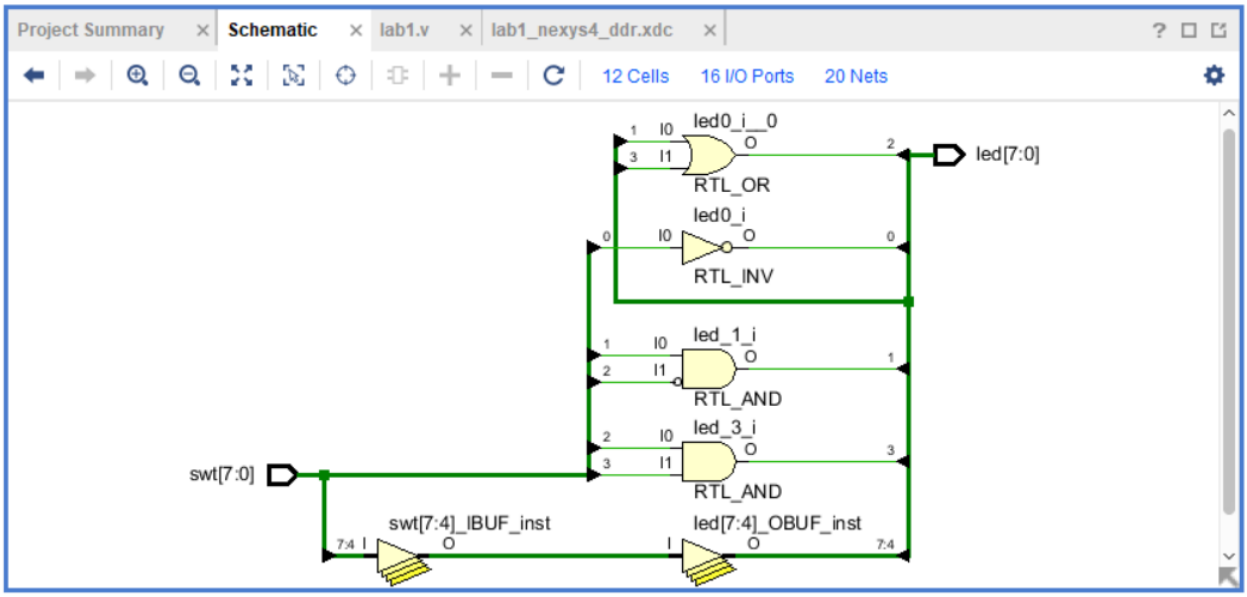
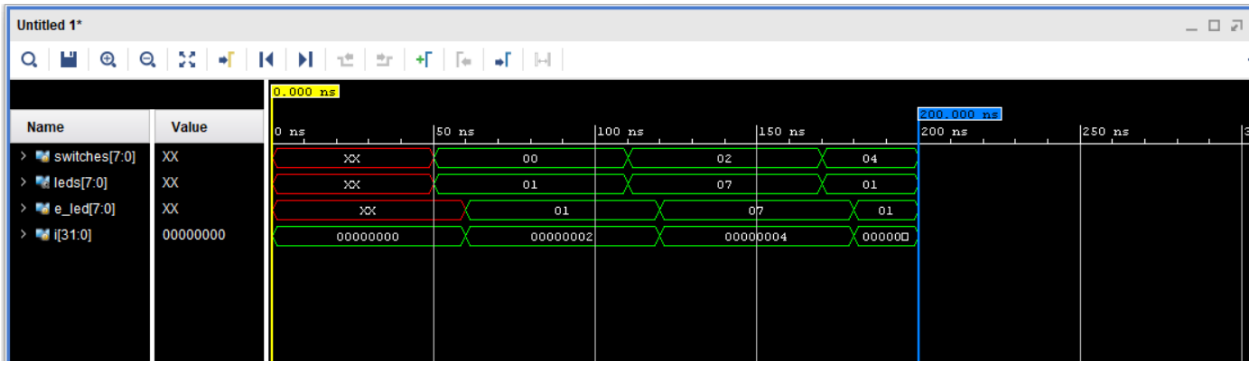
Lab 1 output simulations:

RTL



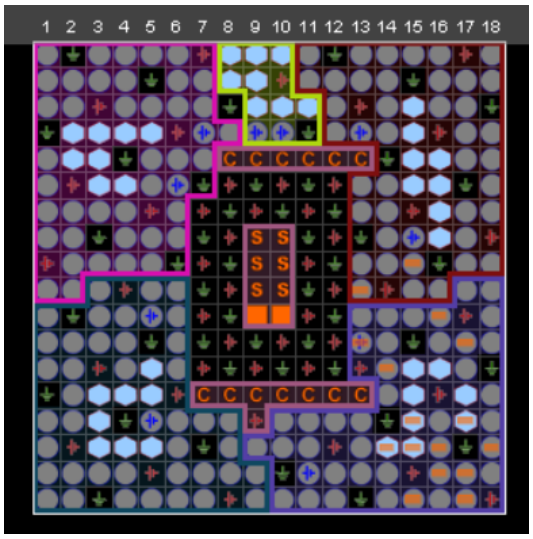
Simulation- behavioural simulation

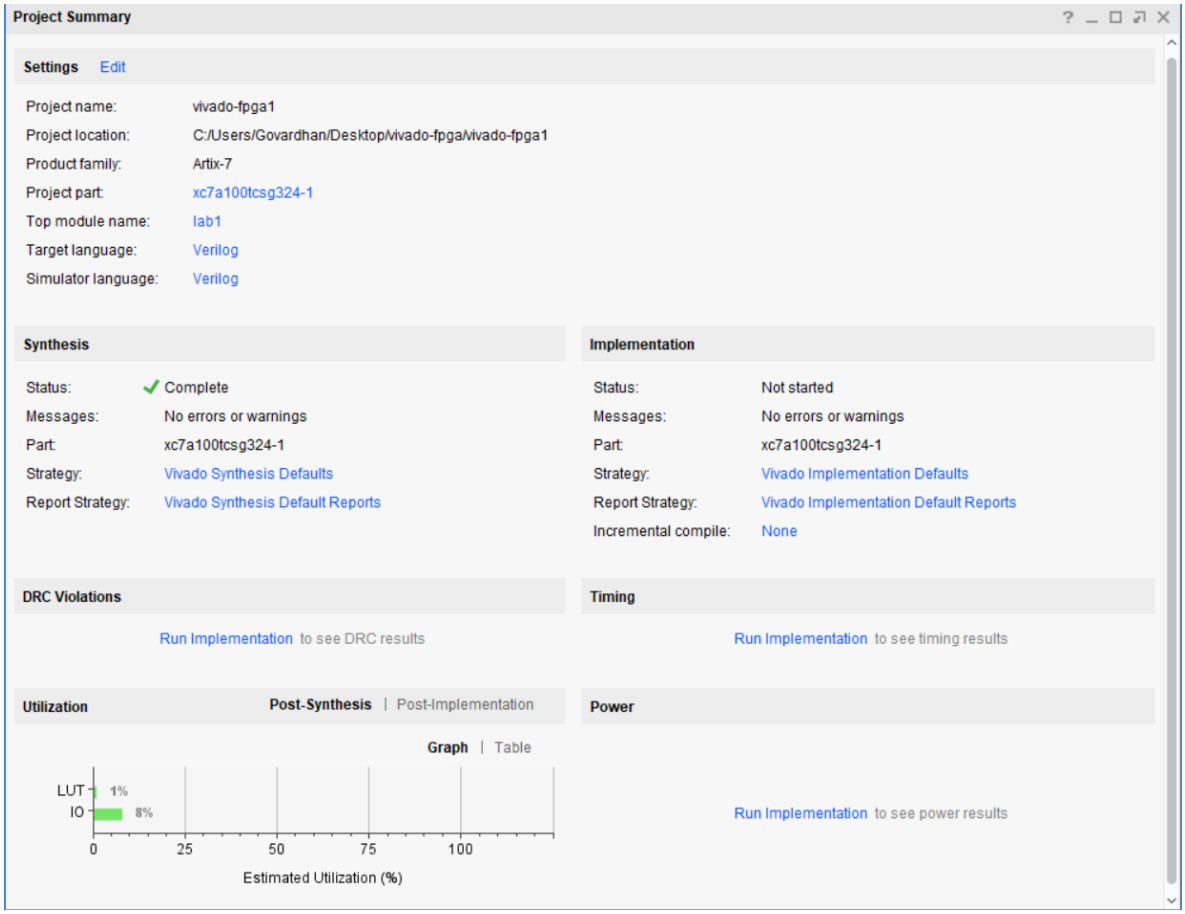


Output Matched Message!

```
#    }
# }
# run 200ns
LED output matched at                 60
LED output matched at                120
LED output matched at                180
INFO: [USF-XSim-96] XSim completed. Design snapshot 'lab1_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 200ns
launch_simulation: Time (s): cpu = 00:00:06 ; elapsed = 00:00:14 . Memory (MB): peak = 1371.840 ; gain = 11.258
save_wave_config {C:/Users/Govardhan/Desktop/vivado-fpga/vivado-fpga1/lab1_tb_behav.wcfg}
```

Synthesised Design





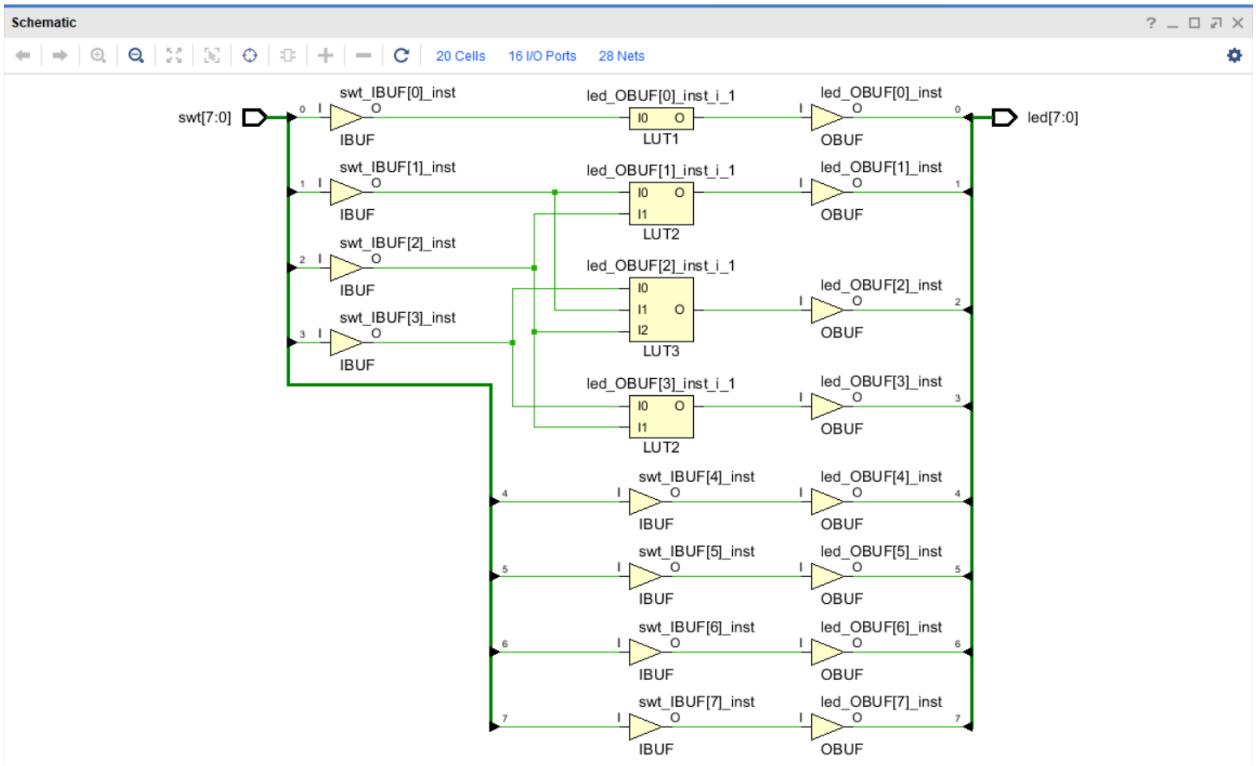
Utilisation table for Basys 3 Board

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

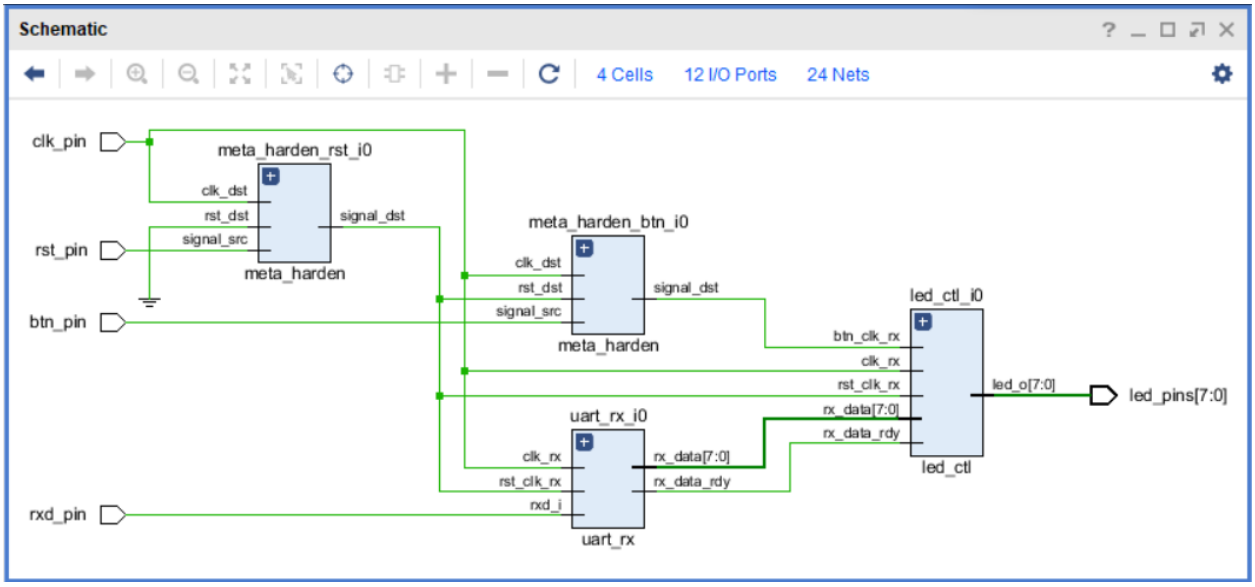
Resource	Estimation	Available	Utilization %
LUT	3	63400	0.01
IO	16	210	7.62

Schematic

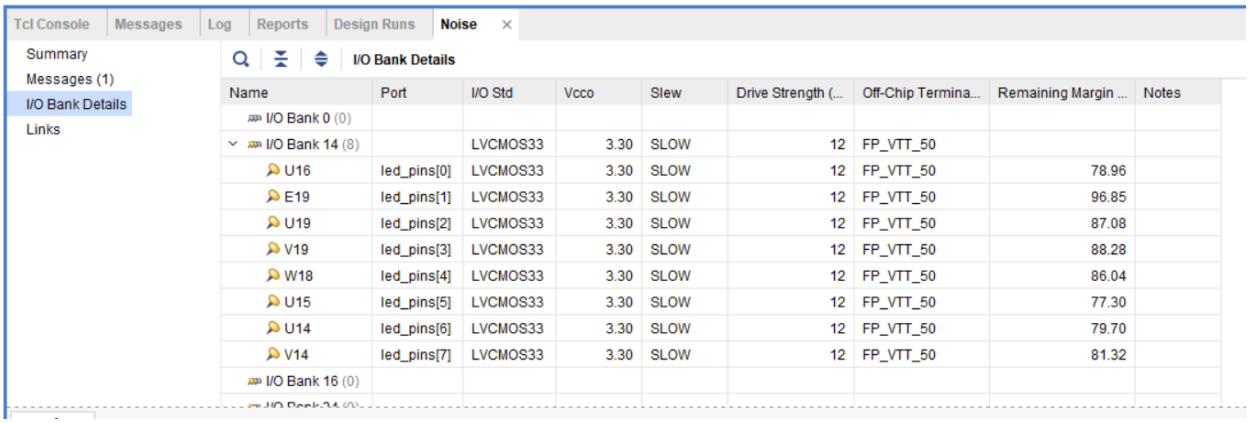


Lab 2 Outputs

RTL Design

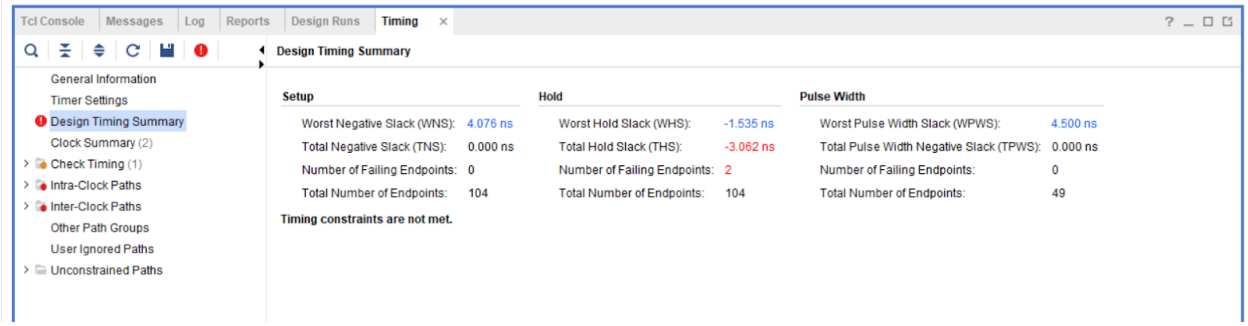


Noise Report



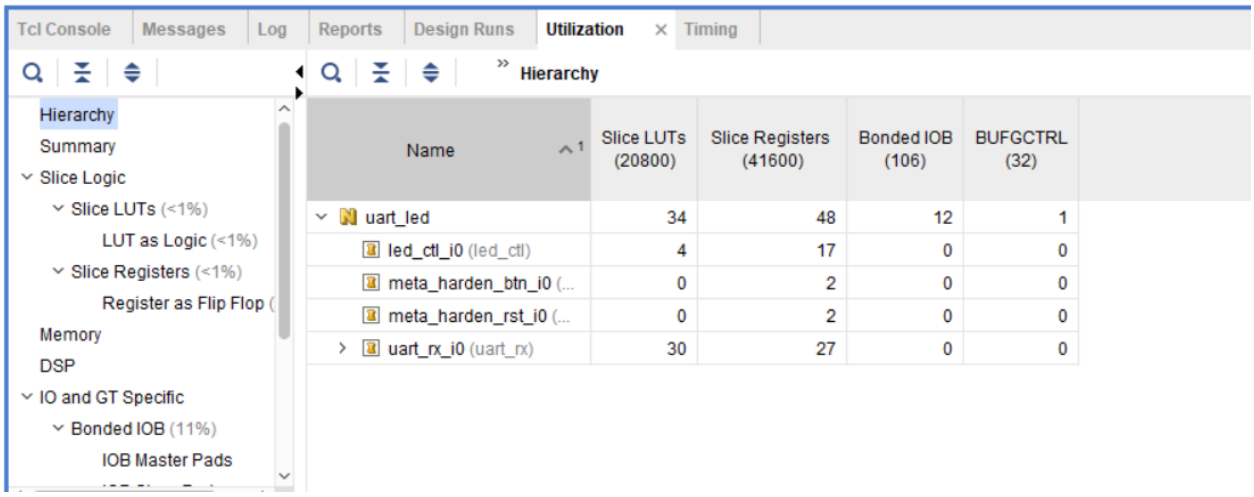
Name	Port	I/O Std	Vcco	Slew	Drive Strength (...	Off-Chip Termina...	Remaining Margin ...	Notes
I/O Bank 0 (0)								
I/O Bank 14 (8)		LVCMOS33	3.30	SLOW	12	FP_VTT_50		
U16	led_pins[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	78.96	
E19	led_pins[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	96.85	
U19	led_pins[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	87.08	
V19	led_pins[3]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	88.28	
W18	led_pins[4]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	86.04	
U15	led_pins[5]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	77.30	
U14	led_pins[6]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	79.70	
V14	led_pins[7]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	81.32	
I/O Bank 16 (0)								

Timing Report

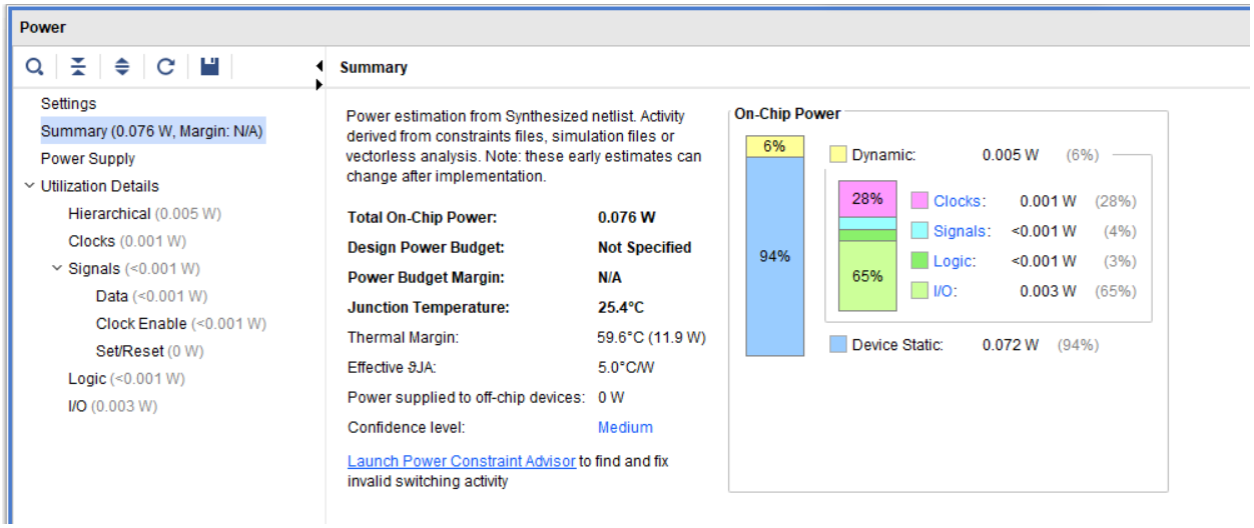


>>TIMING CONSTRAINTS NOT MET

Utilization

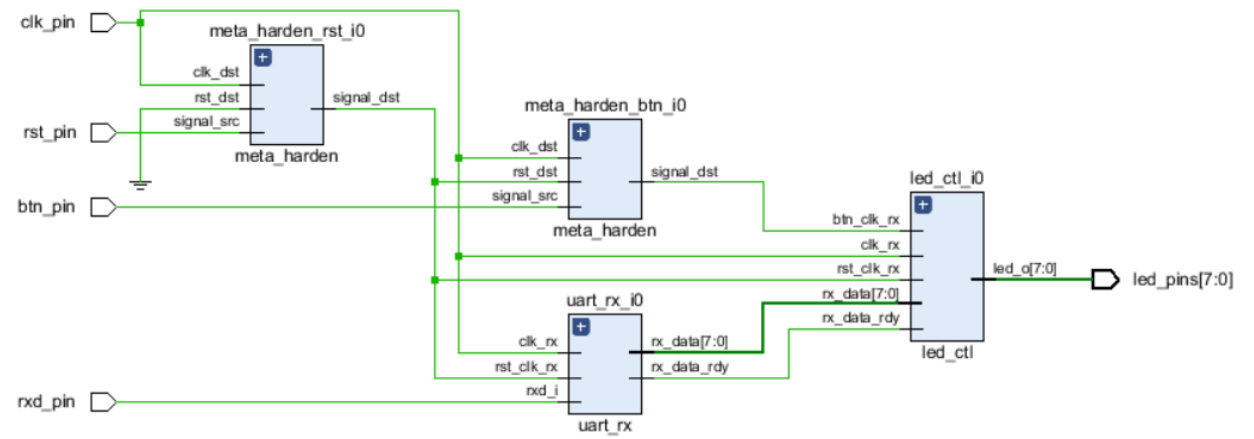


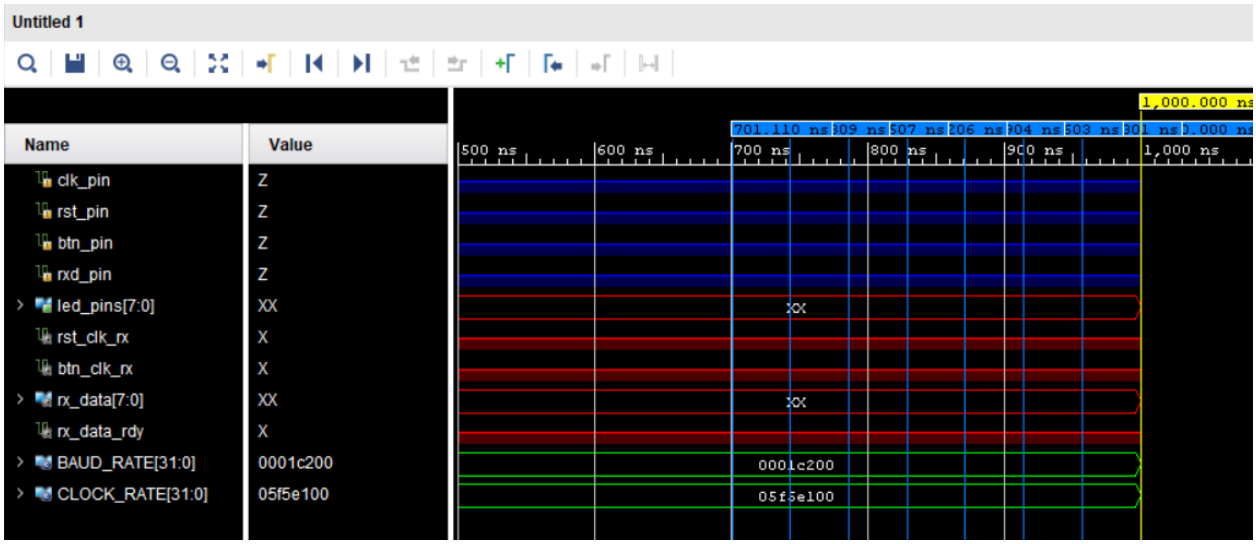
Power Report

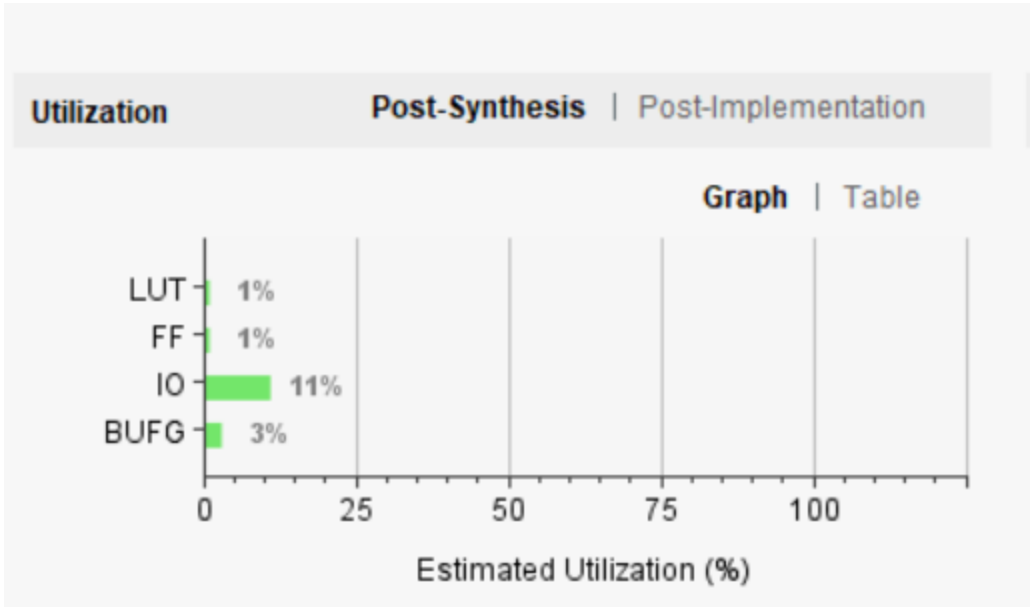


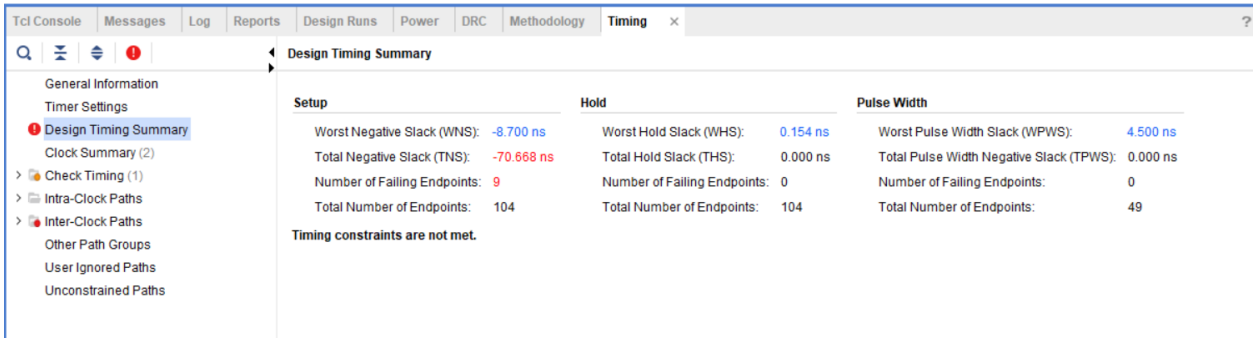
Lab 3

RTL output




Untitled 1
Name
Value
clk_pin
Z
rst_pin
Z
btn_pin
Z
rxd_pin
Z
led_pins[7:0]
XX
rst_clk_rx
X
btn_clk_rx
X
rx_data[7:0]
XX
rx_data_rdy
X
BAUD_RATE[31:0]
0001c200
CLOCK_RATE[31:0]
05f5e100
500 ns
600 ns
700 ns
800 ns
900 ns
1,000 ns
1,000.000 ns
0001c200
05f5e100


Utilization
Post-Synthesis | Post-Implementation
Graph | Table
LUT
1%
FF
1%
IO
11%
BUFG
3%
0
25
50
75
100
Estimated Utilization (%)


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (2)
Check Timing (1)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
Setup
Worst Negative Slack (WNS): -8.700 ns
Total Negative Slack (TNS): -70.668 ns
Number of Failing Endpoints: 9
Total Number of Endpoints: 104
Hold
Worst Hold Slack (WHS): 0.154 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 104
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 49
Timing constraints are not met.