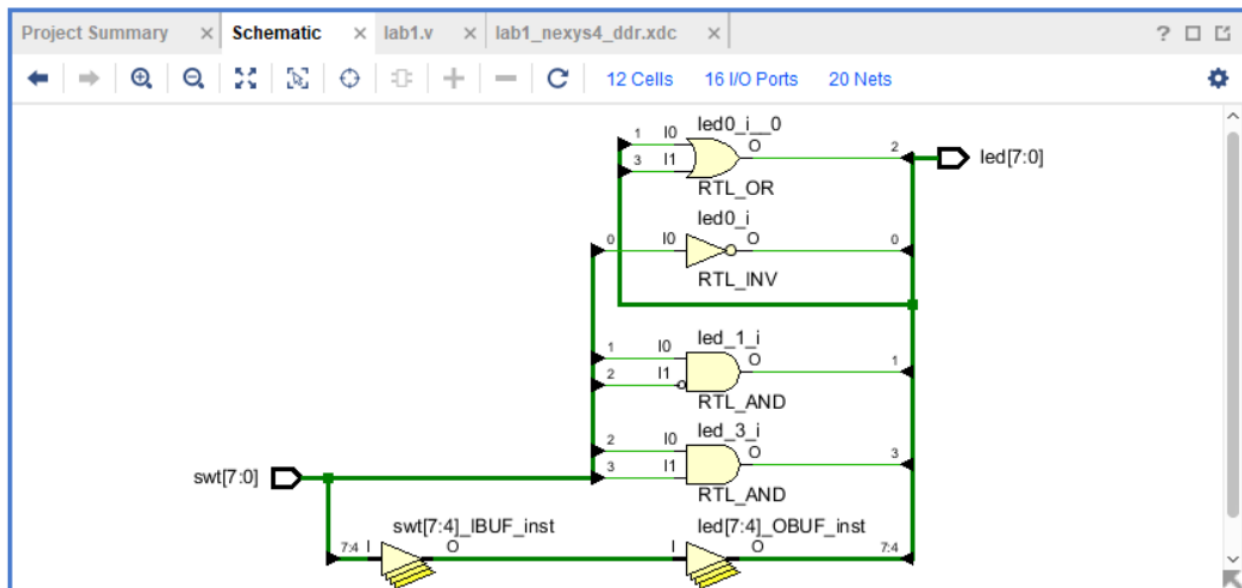
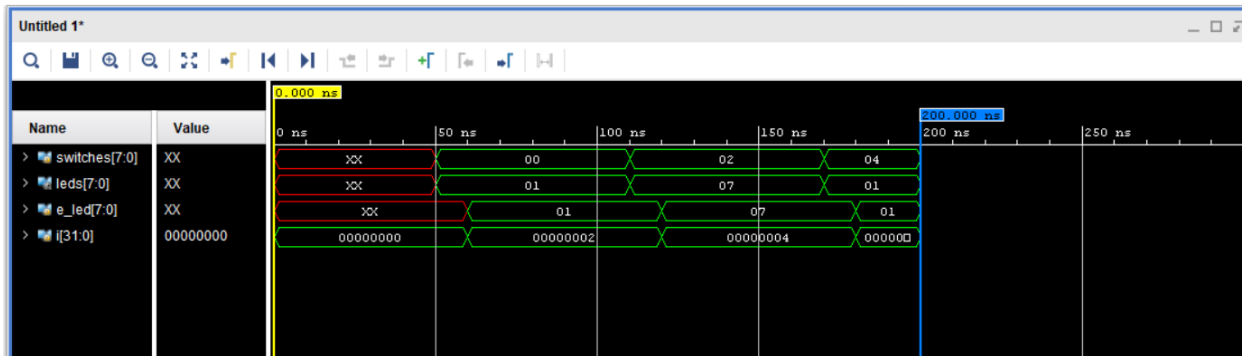


Lab 1 output simulations:  
RTL



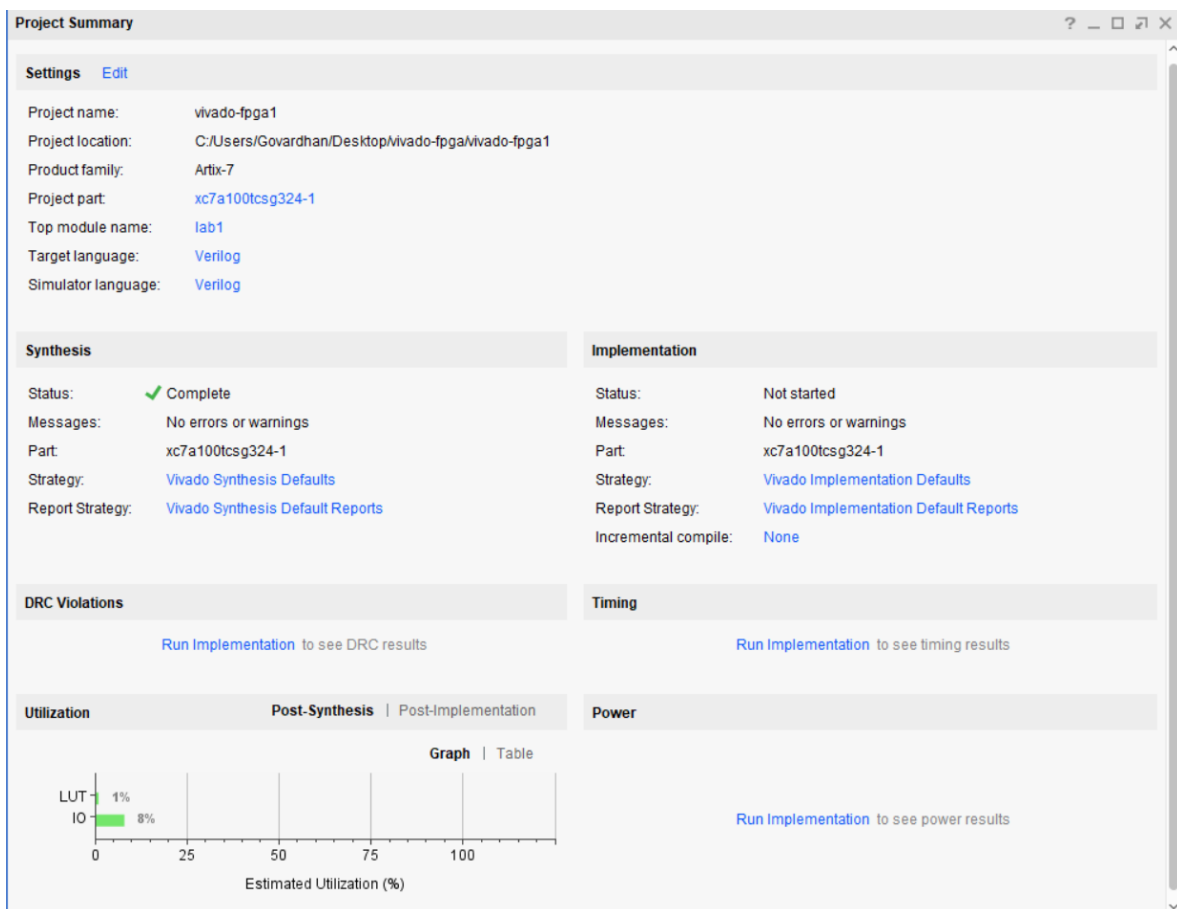
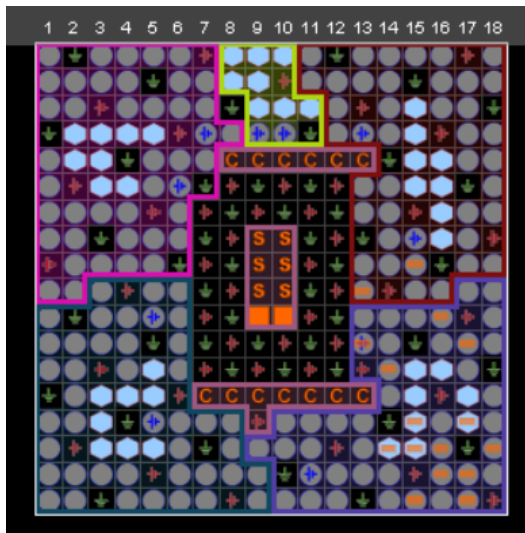
Simulation- behavioural simulation



Output Matched Message!

```
# }
# }
# run 200ns
LED output matched at          60
LED output matched at          120
LED output matched at          180
INFO: [USF-XSim-96] XSim completed. Design snapshot 'lab1_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 200ns
launch_simulation: Time (s): cpu = 00:00:06 ; elapsed = 00:00:14 . Memory (MB): peak = 1371.840 ; gain = 11.258
save_wave_config {C:/Users/Govardhan/Desktop/vivado-fpga/vivado-fpgal/lab1_tb_behav.wcfg}
```

## Synthesised Design



Utilisation table for Basys 3 Board

## Utilization

Post-Synthesis | Post-Implementation

Graph | Table

Resource	Estimation	Available	Utilization %
LUT	3	63400	0.01
IO	16	210	7.62

## Schematic

