8-bit enhanced USB microcontroller CH552, CH551

manual

version 1

Http://wch.c n

1 Overview

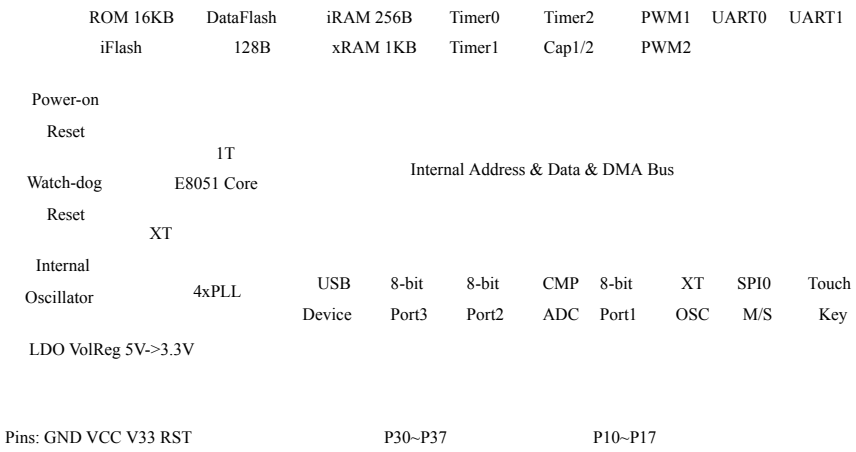
The CH552 chip is an enhanced E8051 core microcontroller compatible with the MCS51 instruction set. 79% of the instructions are single-byte single-cycle. The command, the average command speed is 8 to 15 times faster than the standard MCS51.

CH552 supports up to 32MHz system frequency, built-in 16K program memory ROM and 256 bytes internal iRAM and 1K bytes On-chip xRAM, xRAM supports DMA direct memory access.

CH552 has built-in ADC analog-to-digital conversion, touch button capacitance detection, 3 groups of timers and signal capture and PWM, dual asynchronous serial port, Functional modules such as SPI, USB device controller and full-speed transceiver.

CH551 is a simplified version of CH552, program memory ROM is only 10K, on-chip xRAM is only 512 bytes, asynchronous serial port only mentions For UART0, the package format is only SOP16, and the ADC analog-to-digital conversion module and USB type-C module are removed, except for the above differences. As with the CH552, refer directly to the CH552 manual and documentation.

The following is an internal block diagram of the CH552 for reference only.



2, characteristics

- Core: Enhanced E8051 core, compatible with the MCS51 instruction set, 79% of its instructions are single-byte single-cycle instructions, average instructions The speed is 8 to 15 times faster than the standard MCS51, featuring XRAM data fast copy instructions and dual DPTR pointers.
- ROM: 16KB capacity multi-programmable non-volatile memory ROM, can be used for program storage space; or can be divided It is a 14KB program memory area and a 2KB boot code BootLoader/ISP program area.
- DataFlash: 128-byte non-volatile data memory that can be erased multiple times, and supports data rewriting in bytes.
- RAM: 256 bytes internal iRAM, can be used for fast data temporary storage and stack; 1KB on-chip xRAM, can be used for a large number of According to the temporary storage and DMA direct memory access.
- USB: embedded USB controller and USB transceiver, support USB-Device device mode, support USB type-C master-slave detection, Support USB 2.0 full speed 12Mbps or low speed 1.5Mbps. Supports up to 64 bytes of data packets, built-in FIFO, and DMA support.
- Timer: 3 groups of timers, T0/T1/T2 are standard MCS51 timers.

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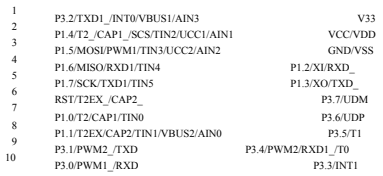
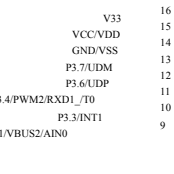
- Capture: Timer T2 is extended to support 2 signal captures.
- PWM: 2 sets of PWM outputs, PWM1/PWM2 are 2 8-bit PWM outputs.
- UART: 2 sets of asynchronous serial ports, all support higher communication baud rate, UART0 is standard MCS51 serial port.
- SPI: SPI controller built-in FIFO, clock frequency up to half of the system frequency Fsys, support serial data input and output Simplex multiplexing, supporting Master/Slave master-slave mode.
- ADC: 4-channel 8-bit A/D analog-to-digital converter that supports voltage comparison.
- Touch-Key: 6-channel capacitance detection, supports up to 15 touch buttons, and supports independent timer interrupt.
- GPIO: Supports up to 17 GPIO pins (including XI/XO and RST and USB signal pins).
- Interrupt: Support 14 groups of interrupt sources, including 6 groups of interrupts compatible with standard MCS51 (INT0, T0, INT1, T1) UART0, T2), and extended 8 groups of interrupts (SPI0, TKEY, USB, ADC, UART1, PWMX, GPIO, WDOG), The middle GPIO interrupt can be selected from 7 pins.
- Watch-Dog: 8-bit preset watchdog timer WDOG, which supports timed interrupt.
- Reset: Supports 4 kinds of reset signal sources, built-in power-on reset, support software reset and watchdog overflow reset, optional pin The input is reset.
- Clock: Built-in 24MHz clock source, external crystal can be supported by multiplexing GPIO pins.
- Power: Built-in 5V to 3.3V low dropout voltage regulator, supporting 5V or 3.3V or even 2.8V supply voltage. Support low work Sleep-free, support USB, UART0, UART1, SPI0 and some GPIO external wake-up.
- The chip has a unique ID number built in.

3, the package

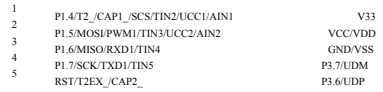
CH552T



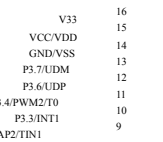
CH552G



CH552E



CH551G



Package form	Plastic body width		Pin spacing		Package description	Order model
TSSOP-20	4.40mm	173mil	0.65mm	25mil	Thin and small 20-foot patch	CH552T
SOP-16	3.9mm	150mil	1.27mm	50mil	Standard 16-foot patch	CH552G
MSOP-10	3.0mm	118mil	0.50mm	19.7mil micro-small 10-foot patch		CH552E
SOP-16	3.9mm	150mil	1.27mm	50mil	Standard 16-foot patch	CH551G

4, the pin

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Pin number			Pin	Other function name	Other function description
TSSOP20	SOP16	MSOP10	name	(Left function is preferred)	
19	15	9	VCC	VDD	For the power input, an external 0.1uF power supply decoupling capacitor is required.
20	16	10	V33		Internal USB power regulator output and internal USB power input, Connect VCC to the external power supply when the power supply voltage is less than 3.6V.

18	14	8	GND VSS	External 0.1uF power supply decoupling capacitor when the power supply voltage is greater than 3.6V Common ground terminal.
6	6	5	The RST RST/T2EX_/CAP2_	suffix underlined pin is a mapping of un-underlined pins of the same name.
7	-	-	P1.0 T2/CAP1/TIN0	The RST pin has a built-in pull-down resistor; other GPIOs have pull-up resistors by default.
8	9	-	P1.1 T2EX/CAP2/TIN1 /VBUS2/AIN0	RST: External reset input. T2: External count input/clock output of timer/counter 2.
17	-	-	P1.2 XI/RXD_	T2EX: Timer/Counter 2 Reload/Capture Input.
16	-	-	P1.3 XO/TXD_	CAP1, CAP2: Capture input 1 and 2 of timer/counter 2.
2	2	1	P1.4 T2_/CAP1_/SCS /TIN2/UCC1/AIN1	TIN0～TIN5: 0#～5# channel touch button capacitance detection input. AIN0 to AIN3: 0# to 3# channel ADC analog signal input.
3	3	2	P1.5 MOSI/PWM1/TIN3 /UCC2/AIN2	UCC1, UCC2: USB type-C bidirectional configuration channel. VBUS1, VBUS2: USB type-C bus voltage detection input.
4	4	3	P1.6 MISO/RXD1/TIN4	XI, XO: external crystal oscillator input, inverting output.
5	5	4	P1.7 SCK/TXD1/TIN5	RXD, TXD: UART0 serial data input, serial data output.
10	8	-	P3.0 PWM1_/RXD	SCS, MOSI, MISO, SCK: SPI0 interface, SCS is chip select input
9	7	-	P3.1 PWM2_/TXD	In, MOSI is the master output/slave input, MISO is the master input
1	1	-	P3.2 TXD1_/INT0 /VBUS1/AIN3	/ Slave output, SCK is the serial clock. PWM1, PWM2: PWM1 output, PWM2 output. RXD1, TXD1: UART1 serial data input, serial data output.
11	10	-	P3.3 INT1	INT0, INT1: External interrupt 0, external interrupt 1 input.
12	11	-	P3.4 PWM2/RXD1_/T0	T0, T1: Timer 0, Timer 1 external input.
13	-	-	P3.5 T1	UDM, UDP: D-, D+ signal terminals of USB devices.
14	12	6	P3.6 UDP	Note: P3.6 and P3.7 use V33 internally as I/O power supply.
15	13	7	P3.7 UDM	With its input and output high level can only reach V33 voltage, does not support 5V

5, special function register SFR

The following abbreviations may be used in describing the registers in this manual:

abbreviation	description
RO	Indicates access type: read only
WO	Indicates the access type: write only, the value read is invalid
RW	Indicates access type: readable and writable
H	Express hexadecimal number with its end
B	End with a binary number

5.1 SFR Introduction and Address Distribution

The CH552 uses the Special Function Register SFR to control, manage, and set the operating mode.

The SFR occupies the 80h-FFh address range of the internal data storage space and can only be accessed by direct address mode instructions. Among them Registers with addresses x0h or x8h are bit-addressable, which avoids modifying the value of other bits when accessing a specific bit;
Registers with other addresses that are not multiples of 8 can only be accessed in bytes.

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Some SFRs can only write data in safe mode, but are read-only in non-secure mode, for example: GLOBAL_CFG, CLOCK_CFG, WAKE_CTRL.

Some SFRs have one or more aliases, for example: SPI0_CK_SE/SPI0_S_PRE.

The partial address corresponds to a plurality of independent SFRs, for example: SAFE_MOD/CHIP_ID, ROM_CTRL/ROM_STATUS.

The CH552 contains registers for the 8051 standard SFR, with additional device control registers added. The specific SFR is shown in the table below.

Table 5.1 Special Function Register Table

SFR	0,8	1,9	2, A	3, B	4, C	5, D	6, E	7, F
0xF8	SPI0_STAT	SPI0_DATA	SPI0_CTRL	SPI0_CK_SE SPI0_S_PRE	SPI0_SETUP		RESET_KEEP	WDOG_COUNT
0xF0	B							
0xE8	IE_EX	IP_EX	UEP4_1_MOD	UEP2_3_MOD	UEP0_DMA_L	UEP0_DMA_H	UEP1_DMA_L	UEP1_DMA_H
0xE0	ACC	USB_INT_EN	USB_CTRL	USB_DEV_AD	UEP2_DMA_L	UEP2_DMA_H	UEP3_DMA_L	UEP3_DMA_H
0xD8	USB_INT_FG	USB_INT_ST	USB_MIS_ST	USB_RX_LEN	UEP0_CTRL	UEP0_T_LEN	UEP4_CTRL	UEP4_T_LEN
0xD0	PSW	UDEV_CTRL	UEP1_CTRL	UEP1_T_LEN	UEP2_CTRL	UEP2_T_LEN	UEP3_CTRL	UEP3_T_LEN

0xC8	T2CON	T2MOD	RCAP2L	RCAP2L	TL2	TH2	T2CAP1L	T2CAP1H
0xC0	SCON1	SBUF1	SBAUD1	TKEY_CTRL	TKEY_DATL	TKEY_DATH	PIN_FUNC	GPIO_IE
0xB8	IP	CLOCK_CFG						
0xB0	P3	GLOBAL_CFG						
0xA8	IE	WAKE_CTRL						
0xA0	P2	SAFE_MOD CHIP_ID	XBUS_AUX					
0x98	SCON	SBUF	ADC_CFG	PWM_DATA2	PWM_DATA1	PWM_CTRL	PWM_CK_SE	ADC_DATA
0x90	P1	USB_C_CTRL	P1_MOD_OC	P1_DIR_PU			P3_MOD_OC	P3_DIR_PU
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_L	ROM_DATA_H
0x80	ADC_CTRL	SP	DPL	DPH	ROM_ADDR_L	ROM_ADDR_H	ROM_CTRL ROM_STATUS	PCON

Remarks: (1), red text means can be addressed by bit; (2), the following is the corresponding description of the color box

Register address

SPI0 related register

ADC related register

Touch-Key related register

USB related register

Timer/Counter 2 Related Register

Port setting related register

PWM1 and PWM2 related registers

UART1 related register

Flash-ROM related register

5.2 SFR classification and reset values

Table 5.2 SFR Description and Reset Values

Functional classification	name	address	description	Reset value
System settings	B	F0h	B register	0000 0000b
Related register	ACC	E0h	accumulator	0000 0000b

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	PSW	D0h	program status register	0000 0000b
	GLOBAL_CFG	B1h	Global configuration register (CH552 bootloader status)	1010 0000b
			Global Configuration Register (CH552 Application Status)	1000 0000b
			Global configuration register (in CH551 bootloader state)	1110 0000b
			Global configuration register (in CH551 application state)	1100 0000b
	CHIP_ID	A1h	CH552 chip ID identification code (read only)	0101 0010b
			CH551 chip ID identification code (read only)	0101 0001b
	SAFE_MOD	A1h	safe mode control register (write only)	0000 0000b
	DPH	83h	data address pointer is 8 bits high	0000 0000b
	DPL	82h	data address pointer lower 8 bits	0000 0000b
	DPTR	82h	DPL and DPH form a 16-bit SFR	0000h
	SP	81h	stack pointer	0000 0111b
	WDOG_COUNT	FFh	watchdog count register	0000 0000b
Clock, sleep	RESET_KEEP	FEh	reset holding register (in power-on reset state)	0000 0000b
And power control	CLOCK_CFG	B9h	system clock configuration register	1000 0011b
Related register	WAKE_CTRL	A9h	Sleep Wake Control Register	0000 0000b
	PCON	87h	power control register (in power-on reset state)	0001 0000b
	IP_EX	E9h	extended interrupt priority control register	0000 0000b
	IE_EX	E8h	extended interrupt enable register	0000 0000b
Interrupt control	GPIO_IE	C7h	GPIO Interrupt Enable Register	0000 0000b
Related register	IP	B8h	Interrupt Priority Control Register	0000 0000b
	IE	A8h	interrupt enable register	0000 0000b

	ROM_DATA_H	8Fh flash-ROM data register high byte	Xxxx xxxxb
	ROM_DATA_L	8Eh flash-ROM data register low byte	Xxxx xxxxb
	ROM_DATA	8Eh ROM_DATA_L and ROM_DATA_H form a 16-bit SFR	Xxxxh
Flash-ROM	ROM_STATUS	86h flash-ROM status register (read only)	0000 0000b
Related register	ROM_CTRL	86h flash-ROM control register (write only)	0000 0000b
	ROM_ADDR_H	85h flash-ROM address register high byte	Xxxx xxxxb
	ROM_ADDR_L	84h flash-ROM address register low byte	Xxxx xxxxb
	ROM_ADDR	84h ROM_ADDR_L and ROM_ADDR_H form a 16-bit SFR	Xxxxh
	PIN_FUNC	C6h pin function selection register	1000 0000b
	XBUS_AUX	A2h external bus auxiliary setting register	0000 0000b
	P3_DIR_PU	97h P3 Port Direction Control and Pull-Up Enable Register	1111 1111b
Port setting	P3_MOD_OC	96h P3 port output mode register	1111 1111b
Related register	P1_DIR_PU	93h P1 Port Direction Control and Pull-Up Enable Register	1111 1111b
	P1_MOD_OC	92h P1 port output mode register	1111 1111b
	P3	B0h P3 port input and output registers	1111 1111b
	P2	A0h P2 port output register	1111 1111b
	P1	90h P1 port input and output registers	1111 1111b
Timer/counter	TH1	8Dh Timer1 count high byte	Xxxx xxxxb
0 and 1	TH0	8Ch Timer0 count high byte	Xxxx xxxxb
Related register	TL1	8Bh Timer1 count low byte	Xxxx xxxxb
	TL0	8Ah Timer0 count low byte	Xxxx xxxxb

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	TMOD	89h Timer0/1 mode register	0000 0000b
	TCON	88h Timer0/1 Control Register	0000 0000b
UART0	SBUF	99h UART0 Data Register	Xxxx xxxxb
Related register	SCON	98h UART0 Control Register	0000 0000b
	T2CAP1H	CFh Timer2 capture 1 data high byte (read only)	Xxxx xxxxb
	T2CAP1L	CEh Timer2 capture 1 data low byte (read only)	Xxxx xxxxb
	T2CAP1	CEh T2CAP1L and T2CAP1H form a 16-bit SFR	Xxxxh
	TH2	CDh Timer2 counter high byte	0000 0000b
	TL2	CCh Timer2 counter low byte	0000 0000b
Timer/counter	T2COUNT	CCh TL2 and TH2 form a 16-bit SFR	0000h
2 related registers	RCAP2H	CBh count reload/capture 2 data register high byte	0000 0000b
	RCAP2L	CAh Count Reload/Capture 2 Data Register Low Byte	0000 0000b
	RCAP2	CAh RCAP2L and RCAP2H form a 16-bit SFR	0000h
	T2MOD	C9h Timer2 mode register	0000 0000b
	T2CON	C8h Timer2 Control Register	0000 0000b
	PWM_CK_SE	9Eh PWM Clock Divider Setting Register	0000 0000b
PWM1 and PWM2	PWM_CTRL	9Dh PWM Control Register	0000 0010b
Related register	PWM_DATA1	9Ch PWM1 Data Register	Xxxx xxxxb
	PWM_DATA2	9Bh PWM2 Data Register	Xxxx xxxxb
	SPI0_SETUP	FCh SPI0 setup register	0000 0000b
	SPI0_S_PRE	FBh SPI0 Slave Mode Preset Data Register	0010 0000b
SPI0	SPI0_CK_SE	FBh SPI0 clock divider setting register	0010 0000b
Related register	SPI0_CTRL	FAh SPI0 Control Register	0000 0010b
	SPI0_DATA	F9h SPI0 Data Transceiver Register	Xxxx xxxxb
	SPI0_STAT	F8h SPI0 Status Register	0000 1000b
	SBAUD1	C2h UART1 Baud Rate Setting Register	Xxxx xxxxb
UART1	SBUF1	C1h UART1 Data Register	Xxxx xxxxb
Related register	SCON1	C0h UART1 Control Register	0100 0000b
	ADC_DATA	9Fh ADC Data Register	Xxxx xxxxb
ADC	ADC_CFG	9Ah ADC Configuration Register	0000 0000b
Related register	ADC_CTRL	80h ADC Control Register	X000 0000b

Touch-Key Related register	TKEY_DATH	C5h Touch-Key data high byte (read only)	0000 0000b
	TKEY_DATL	C4h Touch-Key data low byte (read only)	Xxxx xxxxb
	TKEY_DAT	C4h TKEY_DATL and TKEY_DATH form a 16-bit SFR	00xxh
	TKEY_CTRL	C3h Touch-Key Control Register	X000 0000b
USB Related register	UEP1_DMA_H	EFh Endpoint 1 Buffer Start Address High Byte	0000 00xxb
	UEP1_DMA_L	EEh Endpoint 1 Buffer Start Address Low Byte	Xxxx xxxxb
	UEP1_DMA	EEh UEP1_DMA_L and UEP1_DMA_H form a 16-bit SFR	0xxxh
	UEP0_DMA_H	EDh endpoint 0 and 4 buffer start address high byte	0000 00xxb
	UEP0_DMA_L	ECh endpoint 0 and 4 buffer start address low byte	Xxxx xxxxb
	UEP0_DMA	ECh UEP0_DMA_L and UEP0_DMA_H form a 16-bit SFR	0xxxh
	UEP2_3_MOD	EBh Endpoint 2, 3 Mode Control Register	0000 0000b
	UEP4_1_MOD	EAh Endpoint 1, 4 Mode Control Register	0000 0000b

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UEP3_DMA_H	E7h Endpoint 3 Buffer Start Address High Byte	0000 00xxb
UEP3_DMA_L	E6h Endpoint 3 Buffer Start Address Low Byte	Xxxx xxxxb
UEP3_DMA	E6h UEP3_DMA_L and UEP3_DMA_H form a 16-bit SFR	0xxxh
UEP2_DMA_H	E5h Endpoint 2 Buffer Start Address High Byte	0000 00xxb
UEP2_DMA_L	E4h Endpoint 2 Buffer Start Address Low Byte	Xxxx xxxxb
UEP2_DMA	E4h UEP2_DMA_L and UEP2_DMA_H form a 16-bit SFR	0xxxh
USB_DEV_AD	E3h USB Device Address Register	0000 0000b
USB_CTRL	E2h USB Control Register	0000 0110b
USB_INT_EN	E1h USB Interrupt Enable Register	0000 0000b
UEP4_T_LEN	DFh Endpoint 4 Transmit Length Register	0xxx xxxxb
UEP4_CTRL	DEh Endpoint 4 Control Register	0000 0000b
UEP0_T_LEN	DDh Endpoint 0 Transmit Length Register	0xxx xxxxb
UEP0_CTRL	DCh Endpoint 0 Control Register	0000 0000b
USB_RX_LEN	DBh USB Receive Length Register (Read Only)	0xxx xxxxb
USB_MIS_ST	DAh USB Miscellaneous Status Register (Read Only)	Xx10 1000b
USB_INT_ST	D9h USB Interrupt Status Register (Read Only)	00xx xxxxb
USB_INT_FG	D8h USB Interrupt Flag Register	0010 0000b
UEP3_T_LEN	D7h Endpoint 3 Transmit Length Register	0xxx xxxxb
UEP3_CTRL	D6h Endpoint 3 Control Register	0000 0000b
UEP2_T_LEN	D5h Endpoint 2 Transmit Length Register	0000 0000b
UEP2_CTRL	D4h Endpoint 2 Control Register	0000 0000b
UEP1_T_LEN	D3h Endpoint 1 Transmit Length Register	0xxx xxxxb
UEP1_CTRL	D2h Endpoint 1 Control Register	0000 0000b
UDEV_CTRL	D1h USB device port control register	10xx 0000b
USB_C_CTRL	91h USB type-C configuration channel control register	0000 0000b

5.3 General 8051 Register

Table 5.3.1 General 8051 Register List

name	address	description	Reset value
B	F0h B register		00h
A, ACC	E0h accumulator		00h
PSW	D0h program status register		00h
GLOBAL_CFG	B1h	Global configuration register (CH552 bootloader status)	A0h
		Global Configuration Register (CH552 Application Status)	80h
		Global configuration register (in CH551 bootloader state)	E0h
		Global configuration register (in CH551 application state)	C0h
CHIP_ID	A1h	CH552 chip ID identification code (read only)	52h
		CH551 chip ID identification code (read only)	51h
SAFE_MOD	A1h safe mode control register (write only)		00h

PCON	87h power control register (in power-on reset state)	10h
DPH	83h data address pointer is 8 bits high	00h
DPL	82h data address pointer lower 8 bits	00h
DPTR	82h DPL and DPH form a 16-bit SFR	0000h

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SP	81h stack pointer	07h

B register (B):

Bit	name	access	description	Reset value
[7:0]	B	RW	arithmetic operation register, mainly used for multiplication and division, bit-addressable	00h

A accumulator (A, ACC):

Bit	name	access	description	Reset value
[7:0]	A/ACC	RW	arithmetic accumulator, bit addressable	00h

Program Status Register (PSW):

Bit	name	access	description	Reset value
7	CY	RW	Carry flag: used to record the highest bit when performing arithmetic and logic operations Carry or borrow; when performing 8-bit addition, the highest bit is carried, then the bit is set. Otherwise, it is cleared; when 8-bit subtraction is performed, if the bit is borrowed, the bit is set, otherwise it is cleared; Logic instructions can make this bit bit or clear	0
6	AC	RW	Auxiliary carry flag: When recording plus or minus, the lower 4 bits have a carry or borrow from the upper 4 bits. Bit, AC is set, otherwise cleared	0
5	F0	RW	general-purpose flag bit addressable by bit: user-definable, software-clearable or set	0
4	RS1	RW	register set select bit high	0
3	RS0	RW	register set select bit low	0
2	OV	RW	Overflow flag: When adding or subtracting, the operation result exceeds 8 binary digits, then OV is set 1, the flag overflows, otherwise clear 0	0
1	F1	RW	Universal addressable bit-addressable 1: User-definable, software-clearable or set	0
0	P	RO	Parity flag: record the parity of 1 in accumulator A after the execution of the instruction, and an odd number of 1 P Set, even 1 then P clear	0

The state of the processor is stored in the status register PSW and the PSW supports bitwise addressing. The status word includes a carry flag for Auxiliary carry flag, parity flag, overflow flag for BCD code processing, and RS0 and RS1 for working register bank selection.
The area in which the working register set is located can be accessed either directly or indirectly.

Table 5.3.2 RS1 and RS0 Working Register Group Selection Table

RS1	RS0	Working register set
0	0	Group 0 (00h-07h)
0	1	Group 1 (08h-0Fh)
1	0	2 groups (10h-17h)
1	1	3 groups (18h-1Fh)

Table 5.1.3 Operation of the affected flag (X indicates that the flag is related to the operation result)

operating	CY	OV	AC	operating	CY	OV	AC
ADD	X	X	X	SETB C	1		
ADDC	X	X	X	CLR C	0		
SUBB	X	X	X	CPL C	X		
MUL	0	X		MOV C, bit	X		
DIV	0	X		ANL C, bit	X		
DA A	X			ANL C, /bit	X		

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RRC A	X	ORL C, bit	X
RLC A	X	ORL C, /bit	X
CJNE	X		

Data Address Pointer (DPTR):

Bit	name	access	description	Reset value
[7:0]	DPL	RW	data pointer low byte	00h
[7:0]	DPH	RW	data pointer high byte	00h

DPL and DPH form a 16-bit data pointer DPTR for accessing xRAM data memory or program memory, actual DPTR Corresponding to the physical 16-bit data pointers of DPTR0 and DPTR1, dynamically selected by DPS in XBUS_AUX.

Stack pointer (SP):

Bit	name	access	description	Reset value
[7:0]	SP	RW	stack pointer, mainly used for program calls and interrupt calls, and data in and out of the stack	07h

Stack specific functions: protect endpoints and protect the site, and manage them on a first-come, first-out basis. The SP pointer is automatically incremented by 1 when it is pushed onto th Save data or breakpoint information; take the SP pointer to the data unit when popping, and the SP pointer is automatically decremented by 1. The initial value of the SP after reset is 07h. The corresponding default stack storage starts at 08h.

5.4 Unique registers

Global configuration register (GLOBAL_CFG), writable only in safe mode:

Bit	name	access	description	Reset value
[7:6]	Reserved	RO	is a fixed value of 10 for CH552	10b
[7:6]	Reserved	RO	is a fixed value of 11 for CH551	11b
5	bBOOT_LOAD	RO	Boot loader status bit used to distinguish ISP bootloader status or should Program status: Set to 1 when the power is turned on, and cleared to 0 when the software is reset. For chips with an ISP bootloader, this bit is 1 indicating no software reset Yes, usually the ISP bootloader state running after power-on; this bit is 0 Description has been software reset, usually the application status	1
4	bSW_RESET	RW	software reset control bit: Set to 1 to cause software reset, hardware auto-zero	0
3	bCODE_WE	RW	Flash-ROM and DataFlash write enable bits: This bit is 0 for write protection; 1 for Flash-ROM and Data can be overwritten	0
2	bDATA_WE	RW	Flash-ROM's DataFlash area write enable bit: This bit is 0 for write protection; 1 for DataFlash area can be overwritten	0
1	bLDO3V3_OFF	RW	Disable control bits for the USB power regulator LDO: This bit is 0 to allow the LDO, which can be used to generate 3.3V from a 5V supply. USB and internal clock oscillator; 1 for LDO disabled, V33 pin must be input to an external 3.3V supply	0
0	bWDOG_EN	RW	Watchdog reset enable bit: This bit is 0. The watchdog is only used as a timer; this bit Generates a watchdog reset when 1 is allowed to overflow	0

Chip ID (CHIP_ID):

Bit	name	access	description	Reset value
[7:0]	CHIP_ID	RO	for CH552, is a fixed value of 52h, used to identify the chip	52h

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[7:0]	CHIP_ID	RO	for CH551, is a fixed value of 51h, used to identify the chip	51h

Safe Mode Control Register (SAFE_MOD):

Bit	name	access	description	Reset value

[7:0]	SAFE_MOD	WO is used to enter or terminate the security mode	00h

Some SFRs can only write data in safe mode, and are always read-only in non-secure mode. Steps to enter safe mode:

(1), write 55h to the register;

(2), then write AAh to the register;

(3) After that, about 13 to 23 system main frequency cycles are in safe mode, and one or more security classes can be rewritten during the validity period.

SFR or ordinary SFR;

(4) Automatically terminate the security mode after the expiration date;

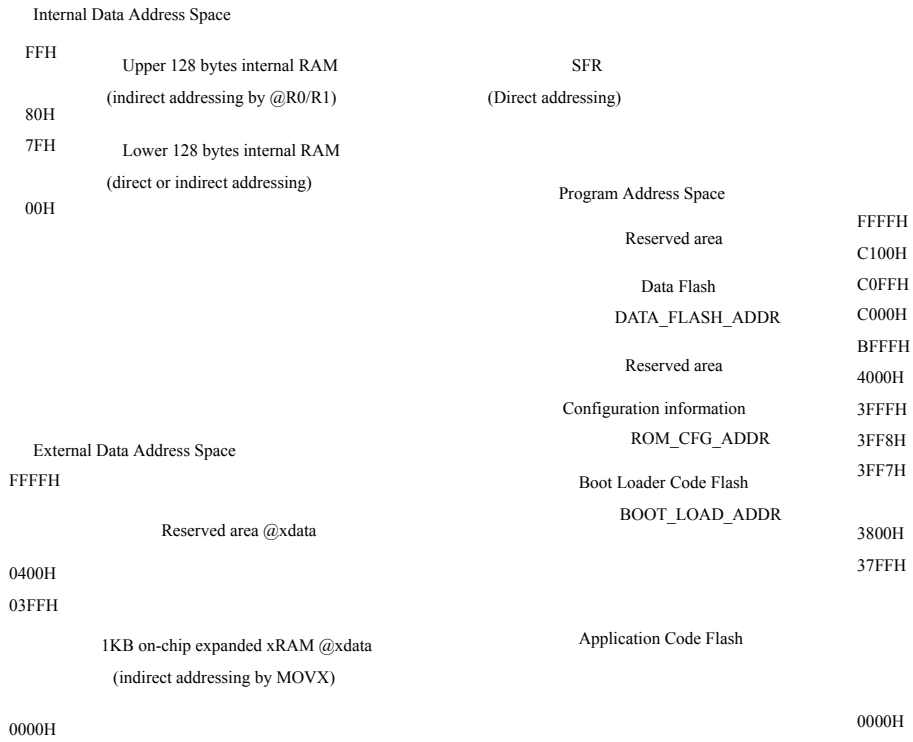
(5), or write an arbitrary value to this register to terminate the security mode early.

6, memory structure

6.1 memory space

The CH552 addressing space is divided into program memory space, internal data storage space, and external data storage space.

Figure 6.1 Memory Structure



6.2 Program Storage Space

The program storage space is 64KB in total, as shown in Figure 6.1, of which 16KB is used for ROM, including Code Flash for saving instruction code.
Zone and configuration information Configuration Information zone.

Code Flash includes the application code of the low address area and the boot code of the high address area. The two areas can also be used.
Merge is used to save a single application code.

For CH551, Code Flash's application code area is only 10KB.

The ROM is an iFlashTM process that can be programmed approximately 200 times at a 5V supply for a finished package with a blank ROM.

The Data Flash address range is from C000h to C0FFH (only the address is valid, actually there is one memory unit every other byte).
Only single-byte (8-bit) read and write operations are supported, and the data remains unchanged after the chip is powered down. Data Flash supports approximately 10,000 erases.

Configuration Information Configuration Information includes 4 groups of 16-bit data located at 3FF8H to 3FFFH addresses, and the last three groups
A read-only unit that provides the chip ID. The configuration data at the 3FF8H address is set by the programmer as needed, refer to Table 6.2.

Table 6.2 Description of flash-ROM configuration information

Bit address	Bit name	Description	suggested value
15	Code_Protect	Code and data protection mode in flash-ROM:	0/1

		0-Prohibit the programmer to read, the program is confidential; 1-Allow readout	
14	No_Boot_Load	Enable the BootLoader boot code startup mode: 0-started from the application at address 0000h; 1- Boot from the 3800h address of the bootloader	1
13	En_Long_Reset	Enable additional delay reset during power-on reset: 0-standard short reset; 1-wide reset, additional 44mS reset time	0
12	En_RST_RESET	Enable RST pin as manual reset input pin: 0-disable; 1-enable RST	0
[11:10]	Reserved	(Automatically set to 00 by the programmer as needed)	00
9	Must_1	(Automatically set to 1 by the programmer as needed)	1
8	Must_0	(Automatically set to 0 by the programmer as needed)	0
[7:0]	All_1	(Automatically set to FFh by the programmer as needed)	FFh

6.3 Data Storage Space

The internal data storage space is 256 bytes in total, as shown in Figure 6.1, all used for SFR and iRAM, where iRAM is used for the stack.

And fast data temporary storage, can be subdivided into working registers R0-R7, bit variables bdata, byte variables data, idata, and so on.

The external data storage space is 64KB in total, as shown in Figure 6.1. Part of it is used for 1KB on-chip expansion xRAM, and the rest is reserved.

For the CH551, the on-chip expansion xRAM is only 512 bytes.

6.4 flash-ROM register

Table 6.4 Flash-ROM Operation Register List

name	address	description	Reset value
ROM_DATA_H	8Fh	flash-ROM data register high byte	Xxh
ROM_DATA_L	8Eh	Flash-ROM data register low byte	Xxh
ROM_DATA	8Eh	ROM_DATA_L and ROM_DATA_H form a 16-bit SFR	Xxxxh
ROM_STATUS	86h	flash-ROM status register (read only)	00h
ROM_CTRL	86h	flash-ROM control register (write only)	00h
ROM_ADDR_H	85h	flash-ROM address register high byte	Xxh
ROM_ADDR_L	84h	Flash-ROM address register low byte	Xxh
ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H form a 16-bit SFR	Xxxxh

flash-ROM address register (ROM_ADDR):

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Bit	name	access	description	Reset value
[7:0]	ROM_ADDR_H	RW	flash-ROM address high byte	Xxh
[7:0]	ROM_ADDR_L	RW	The low byte of the flash-ROM address, only supports even addresses. For Data Flash, the actual offset address 00H-7FH must be shifted to the left 1 bit becomes even address 00H/02H/04H...~FEH and then placed	Xxh

flash-ROM data register (ROM_DATA):

Bit	name	access	description	Reset value
[7:0]	ROM_DATA_H	RW	flash-ROM data to be written high byte	Xxh
[7:0]	ROM_DATA_L	RW	flash-ROM data to be written low byte, For DataFlash, it is the data byte to be written or the read data byte.	Xxh

flash-ROM control register (ROM_CTRL):

Bit	name	access	description	Reset value
[7:0]	ROM_CTRL	WO	flash-ROM control register	00h

flash-ROM status register (ROM_STATUS):

Bit	name	access	description	Reset value
7	Reserved	RO	reservation	0
6	bROM_ADDR_OK	RO	flash-ROM write operation address valid status bit: A bit of 0 indicates that the parameter is invalid; a value of 1 indicates that the address is valid.	0

[5:2]	Reserved	RO	reservation	0000b
1	bROM_CMD_ERR	RO	flash-ROM operation command error status bit: A bit of 0 indicates that the command is valid; a value of 1 indicates an unknown command.	0
0	Reserved	RO	reservation	0

6.5 flash-ROM operation steps

1. Write the flash-ROM code area and write double-byte data to the target address:

(1) If you need to write the flash-ROM code, you must select the 5V power supply voltage;

(2), enable the security mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(3), set the global configuration register GLOBAL_CFG to enable write enable (bCODE_WE or bDATA_WE corresponds to code or data);

(4) Set the address register ROM_ADDR and write the 16-bit target address (the lowest bit is always 0);

(5), set the data register ROM_DATA, write 16 bits of data to be written, steps (4), (5) can be reversed;

(6) Set the operation control register ROM_CTRL to 09Ah to perform the write operation, and the program will automatically suspend the operation during the operation;

(7) After the operation is completed, the program resumes running. At this time, the status register ROM_STATUS can be queried to check the operation status;

To write multiple data, loop (4), (5), (6), (7) steps;

(8), enter safe mode again, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(9) Set the global configuration register GLOBAL_CFG to enable write protection (bCODE_WE=0, bDATA_WE=0).

2. Write the Data Flash data area and write single-byte data to the target address:

(1), enable the security mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(2), set the global configuration register GLOBAL_CFG to enable write enable (bDATA_WE corresponds to data);

(3) Set the address register ROM_ADDR and write the 16-bit target address. The actual offset address 00H-7FH must be shifted to the left by 1 bit.

Even address 00H/02H/04H...~FEH is placed again, and the final address is C000H/C002H/C004...

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(4), set the data register ROM_DATA_L, write 8 bits of data to be written, steps (3), (4) can be reversed;

(5), set the operation control register ROM_CTRL to 09Ah, perform a write operation, and the program automatically pauses during operation;

(6) After the operation is completed, the program resumes running. At this time, the status register ROM_STATUS can be queried to check the operation status;

To write multiple data, loop (3), (4), (5), (6) steps;

(7), enter safe mode again, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(8) Set the global configuration register GLOBAL_CFG to enable write protection (bCODE_WE=0, bDATA_WE=0).

3. Read the Data Flash data area and read single-byte data from the target address:

(1) Set the address register ROM_ADDR and write the 16-bit target address. The actual offset address 00H-7FH must be shifted left by 1 bit.

Even address, the final address is C000H/C002H/C004...

(2) Set the operation control register ROM_CTRL to 08Eh to perform a read operation, and the program automatically pauses during operation;

(3) After the operation is completed, the program resumes running. At this time, bROM_CMD_ERR in the status register ROM_STATUS can be viewed.

Secondary operation state; if the command is valid, the read 8-bit data will be saved in the data register ROM_DATA_L;

(4) If you want to read multiple data, loop (1), (2), and (3) steps.

4, read flash-ROM:

Read the code or data of the target address directly using the MOVC instruction or by pointing to a pointer to the program memory space.

6.6 Onboard programming and ISP downloads

When the configuration information Code_Protect=1, the code in the CH552 chip flash-ROM and the data in the Data Flash can be Read and write by the external programmer through the synchronous serial interface; when the configuration information Code_Protect=0, the code and data in the flash-ROM The data in Flash is protected and cannot be read, but can be erased. If it is erased and then powered back on, the code protection is released.

When the CH552 chip is pre-installed with the BootLoader bootloader, the CH552 can support multiple ISPs such as USB or asynchronous serial ports. The download method loads the application; however, in the absence of a bootloader, the CH552 can only be written to the bootloader by an external dedicated programmer Or an application. In order to support on-board programming, a 5V supply voltage must be temporarily used, and CH552 and programming need to be reserved in the circuit. The four connection pins between the devices, the minimum necessary connection pins are three: P1.4, P1.6, P1.7.

Table 6.6.1 Connection pins to the programmer

Pin	GPIO	Pin description
RST	RST	Reset control pin in programming state, high level allows entry into programming state
SCS	P1.4	Chip select input pin (required) in programming state, default high level, active low
SCK	P1.7	Clock input pin in programming state (required)

MISO	P1.6	Data output pin in programming state (required)

Note: The 5V supply voltage must be temporarily used, whether in board programming or via serial or USB download.

6.7 chip unique ID number

Each microcontroller is shipped with a unique ID number, the chip identification number. The ID data is 5 bytes in total and is stored in the configuration.
Information 3FFAH to 3FFFH address of the Configuration Information area. Where 3FFBH address is reserved, 3FFCH
The 16-bit data of each of the 3FFEH addresses and the 8-bit data of the 3FFAH address are combined into 40-bit chip ID data.

Program space address	ID data description
3FFAh, 3FFBh	ID Last word data, followed by the highest byte of 40-bit ID number, reserved byte
3FFCh, 3FFDh	ID first word data, followed by the lowest byte and the second lowest byte of the ID number
3FFEh, 3FFFh	ID subword data, followed by the second highest byte and high byte of the ID number

This ID data can be obtained by reading Code Flash. The ID number can be used with the download tool to add to the target program.
For dense, general applications, just use the first 32 bits of the ID number, that is, you can ignore the 8-bit data of the 3FFAH address.

7, power management, sleep and reset

7.1 External power input

The CH552 has a built-in 5V to 3.3V low dropout voltage regulator that supports an external 5V or 3.3V or even 2.8V supply voltage.
In, the two power supply voltage input modes refer to the following table.

External supply voltage	VCC pin voltage: external voltage 3V ~ 5V	V33 pin voltage: internal voltage 3.3V
3.3V or 3V	Input an external 3.3V voltage to the voltage regulator,	Input external 3.3V as internal working power supply,
Includes less than 3.6V	Must be grounded to ground not less than 0.1uF decoupling capacitor	Must be grounded to ground not less than 0.1uF decoupling capacitor
5V	Input external 5V voltage to the voltage regulator,	Internal voltage regulator 3.3V output And 3.3V internal working power input,
Including greater than 3.6V	Must be grounded to ground not less than 0.1uF decoupling capacitor	Must be grounded to ground not less than 0.1uF decoupling capacitor

The CH552 is running by default after the power is turned on or the system is reset. Appropriately reduce the performance if the requirements are met
The system's main frequency can reduce the power consumption during operation. When the CH552 does not need to run at all, you can set the PD in PCON to go to sleep.
In the sleep state, external wake-up can be selected through USB, UART0, UART1, SPI0 and some GPIOs.

7.2 Power and Sleep Control Registers

Table 7.2.1 List of Power and Sleep Control Registers

name	address	description	Reset value
WDOG_COUNT	FFh	Watchdog count register	00h
RESET_KEEP	FEh	Reset holding register	00h
WAKE_CTRL	A9h	Sleep wake control register	00h
PCON	87h	Power control register	10h

Watchdog Count Register (WDOG_COUNT):

Bit	name	access	description	Reset value
[7:0]	WDOG_COUNT	RW	The current count of the watchdog, when it is full 0FFh, it will overflow when it is turned to 00h, and it will overflow when it overflows. Set the interrupt flag bWDOG_IF_TO to 1	00h

Reset holding register (RESET_KEEP):

Bit	name	access	description	Reset value
[7:0]	RESET_KEEP	RW	Reset the holding register, the value can be modified manually, except for the power-on reset Any other reset will not affect this value except clear it.	00h

Sleep wake control register (WAKE_CTRL), which can be written only in safe mode:

Bit	name	access	description	Reset value
7	bWAK_BY_USB	RW	USB event wake-up enable, this bit is 0, no wake-up is allowed	0
6	bWAK_RXD1_LO	RW	UART1 Receive Input Low Wake Enable. This bit is 0 to disable wakeup. Select RXD1 or RXD1_ pin according to bUART1_PIN_X=0/1	0

5	bWAK_P1_5_LO	RW P1.5 low wake enable, 0 disable wakeup	0
4	bWAK_P1_4_LO	RW P1.4 low wake enable, 0 disable wakeup	0
3	bWAK_P1_3_LO	RW P1.3 low wake enable, 0 disable wakeup	0
2	bWAK_RST_HI	RW RST high wake-up enable, 0 disable wake-up	0
1	bWAK_P3_2E_3L	RW P3.2 edge change and P3.3 low wake enable, 0 disable wakeup	0
0	bWAK_RXD0_LO	RW UART0 Receive input low wake enable, 0 disable wakeup.	0

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Select RXD0 or RXD0_ pin according to bUART0_PIN_X=0/1

Power Control Register (PCON):

Bit	name	access	description	Reset value
7	SMOD	RW	When using UART0 baud rate with Timer 1, select UART0 mode 1. 2, 3 communication baud rate: 0-slow mode; 1-fast mode	0
6	Reserved	RO reservation		0
5	bRST_FLAG1	R0 chip last reset flag high		0
4	bRST_FLAG0	R0 chip last reset flag low		1
3	GF1	RW universal flag 1: user can define it, can be cleared or set by software		0
2	GF0	RW general flag 0: user can define it himself, can be cleared or set by software		0
1	PD	RW sleep mode enable, set to sleep, wake up, hardware automatically clears after wake-up		0
0	Reserved	RO reservation		0

Table 7.2.2 Description of the last reset flag of the chip

bRST_FLAG1	bRST_FLAG0	Reset flag description
0	0	Software reset, source: bSW_RESET=1 and (bBOOT_LOAD=0 or bWDOG_EN=1)
0	1	Power-on reset, source: VCC pin voltage is lower than the detection level
1	0	Watchdog reset, source: bWDOG_EN=1 and watchdog timeout
1	1	External pin manually reset, source: En_RST_RESET=1 and RST input high

7.3 Reset Control

The CH552 has four reset sources: power-on reset, external reset, software reset, watchdog reset, and the latter three are hot resets.

7.3.1 Power-on reset

The power-on reset POR is generated by the on-chip voltage detection circuit. The POR circuit continuously monitors the supply voltage of the VCC pin, which is lower than the detection
A power-on reset is generated when Vpot is flat, and Tpor is automatically delayed by hardware to maintain the reset state. After the delay is over, CH552 runs.

Only the power-on reset causes the CH552 to reload the configuration information and clear RESET_KEEP. Other thermal resets do not affect.

7.3.2 External reset

An external reset is generated by a high level applied to the RST pin. When the configuration information En_RST_RESET is 1, and on the RST pin
The reset process is triggered when the high level duration is greater than Trst. When the high level signal is removed, the hardware automatically delays Trdl to maintain
Reset state, CH552 starts from 0 address after the delay is over.

7.3.3 Software Reset

The CH552 supports an internal software reset to actively reset the CPU state and re-run without external intervention. Set global
The bSW_RESET in the configuration register GLOBAL_CFG is 1, which is a software reset, and automatically delays Trdl to maintain the reset state.
After the delay expires, CH552 starts from address 0 and the bSW_RESET bit is automatically cleared by hardware.

When bSW_RESET is set to 1, bBOOT_LOAD=0 or bWDOG_EN=1, then bRST_FLAG1/0 will indicate after reset
For software reset; when bSW_RESET is set to 1, if bBOOT_LOAD=1 and bWDOG_EN=0, then bRST_FLAG1/0 will not
A new reset flag is generated, but the previous reset flag is left unchanged.

For chips with an ISP bootloader, after the power-on reset, run the bootloader first, which resets the core as needed.
Chip to switch to the application state, this software reset only causes bBOOT_LOAD to be cleared, does not affect the state of bRST_FLAG1/0 (by
bBOOT_LOAD=1) before reset, so when switching to the application state, bRST_FLAG1/0 still indicates the power-on reset state.

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7.3.4 Watchdog Reset

The watchdog reset is generated when the watchdog timer times out. The watchdog timer is an 8-bit counter whose clock frequency is counted. For the system frequency Fsys/65536, an overflow signal is generated when 0FFh is turned to 00h.

The watchdog timer overflow signal will trigger the interrupt flag bWDOG_IF_TO to be 1, which will reload WDOG_COUNT It is automatically cleared when it enters the corresponding interrupt service routine.

Different timing periods Twdc are achieved by writing different count initial values to WDOG_COUNT. At 6MHz, The watchdog timing period Twdc when writing 00h is about 2.8 seconds, and about 1.4 seconds when writing 80h. Halve at 12MHz.

If bWDOG_EN = 1 when the watchdog timer overflows, a watchdog reset is generated and Trdl is automatically delayed to maintain reset Status, CH552 starts from 0 address after the delay.

To avoid being reset by the watchdog when bWDOG_EN=1, WDOG_COUNT must be reset in time to avoid overflow.

8, system clock

8.1 Clock Block Diagram

Figure 8.1.1 Clock system and structure

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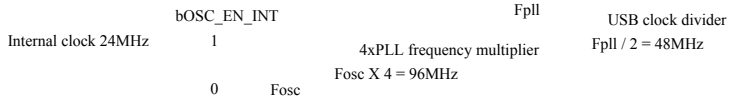

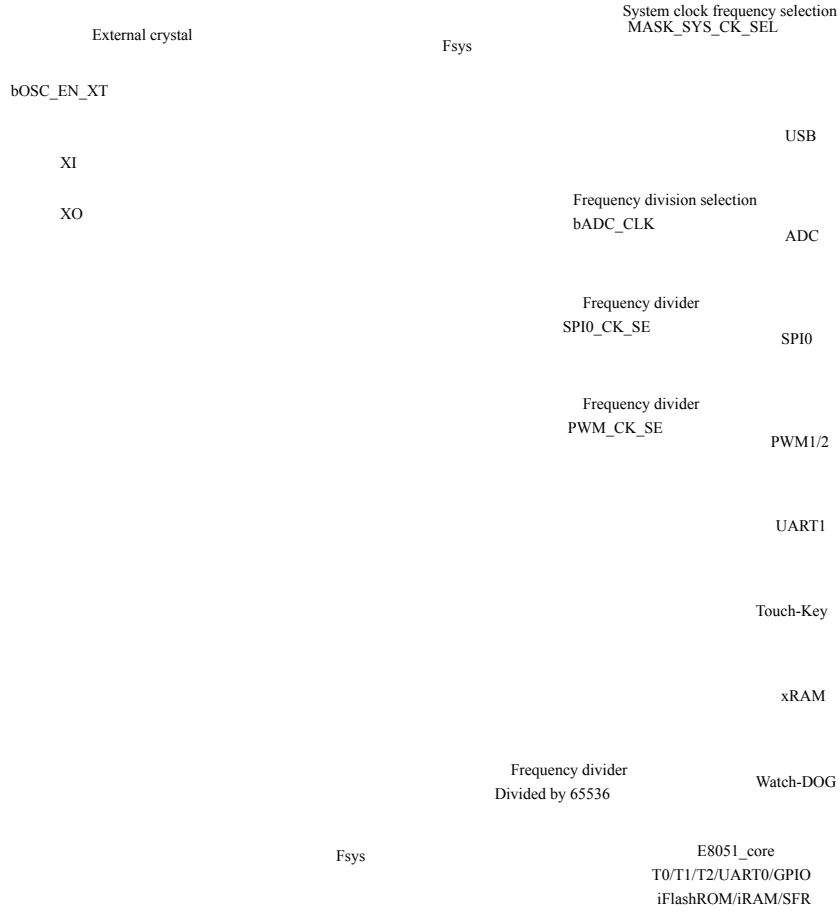

The internal clock or external clock is selected as the original clock Fosc, and then multiplied by 4xPLL to generate Fpll high frequency.
The clock is finally passed through the two-component frequency converter to obtain the system clock Fsys and the clock of the USB module Fusb4x. System clock Fsys directly
Each module is supplied to the CH552.

8.2 Register Description

Table 8.2.1 List of Clock Control Registers

name	address	description	Reset value
CLOCK_CFG	B9h	System clock configuration register	83h

System clock configuration register (CLOCK_CFG), which can be written only in safe mode:

Bit	name	access	description	Reset value

7	bOSC_EN_INT	RW	Internal clock oscillator enabled, this bit is 1 to enable the internal clock oscillator And select the internal clock; this bit is 0 to turn off the internal clock oscillator and And use an external crystal oscillator to provide the clock	1
6	bOSC_EN_XT	RW	The external crystal oscillator is enabled. This bit is 1 for the P1.2/P1.3 pin. For XI/XO and enable the oscillator, external quartz is required between XI and XO. Crystal or ceramic oscillator; this bit is 0 to turn off the external oscillator	0
5	bWDOG_IF_TO	RO	Watchdog timer interrupt flag bit, this bit is 1 for interrupt, by The timer overflow signal is triggered; this bit is 0 for no interrupt. This bit is at Reload the watchdog count register WDOG_COUNT or enter Automatically clear after the corresponding interrupt service routine	0
4	bROM_CLK_FAST	RW	flash-ROM reference clock frequency selection: 0- normal (if Fosc>=16MHz); 1-Speed up (if Fosc<16MHz)	0

3	bRST	R0 RST pin status input bit	0
[2:0]	MASK_SYS_CK_SEL	RW system clock frequency selection, refer to Table 8.2.2 below	011b

Table 8.2.2 System main frequency selection table

MASK_SYS_CK_SEL	System frequency Fsys	Fsys with crystal frequency Fxt when Fosc=24MHz	
000	Fpll / 512	Fxt / 128	187.5KHz
001	Fpll / 128	Fxt / 32	750KHz
010	Fpll / 32	Fxt / 8	3MHz
011	Fpll / 16	Fxt / 4	6MHz
100	Fpll / 8	Fxt / 2	12MHz
101	Fpll / 6	Fxt / 1.5	16MHz
110	Fpll / 4	Fxt / 1	24MHz
111	Fpll / 3	Fxt / 0.75	32MHz

8.3 Clock Configuration

The CH552 chip uses the internal clock by default after power-on. The internal clock frequency is 24MHz. Internal time can be selected by CLOCK_CFG
Clock or external crystal oscillator clock, if the external crystal oscillator is turned off, the XI and XO pins can be used as P1.2 and P1.3
Normal I/O port usage. If an external crystal oscillator is used to provide the clock, the crystal should be bridged between the XI and XO pins.
And connect the oscillating capacitor to the GND pin for the XI and XO pins respectively; if the clock signal is directly input from the outside, it should be from the XI pin.
Input, XO pin is left floating.

Raw clock frequency Fosc = bOSC_EN_INT ? 24MHz : Fxt

PLL frequency Fpll = Fosc * 4 = 96MHz

USB clock frequency Fusb4x = Fpll / 2 = 48MHz

The system frequency Fsys reference table 8.2.2 is obtained by Fpll frequency division.

In the default state after reset, Fosc=24MHz, Fpll=96MHz, Fusb4x=48MHz, Fsys=6MHz.

The steps to switch to the external crystal oscillator to provide the clock are as follows:

(1), enter the safe mode, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;

(2) Set the bOSC_EN_XT in CLOCK_CFG to 1 by using the "Bit OR" operation. The other bits remain unchanged and the crystal oscillator is enabled.

(3), the delay is several milliseconds, usually 5mS ~ 10mS, waiting for the crystal oscillator to work stably;

(4), enter safe mode again, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;

(5) Clear the bOSC_EN_INT in CLOCK_CFG to 0 with the “Bit AND” operation, and the other bits remain unchanged and switch to the external clock.

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(6) Turn off the safety mode and write any value to SAFE_MOD to terminate the safety mode early.

The steps to modify the system's main frequency are as follows:

(1), enter the safe mode, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;

(2) Write a new value to CLOCK_CFG;

(3) Turn off the safety mode and write any value to SAFE_MOD to terminate the safety mode early.

Remarks:

(1) If using a USB module, the Fusb4x must be 48MHz; and when using full-speed USB, the system's main frequency Fsys is not lower than 6MHz; when using low-speed USB, the system's main frequency Fsys is not less than 1.5MHz.

(2), the lower system clock frequency Fsys is preferentially used, thereby reducing the system dynamic power consumption and widening the operating temperature range.

(3) The internal clock oscillator is powered by the V33 power supply, so the V33 voltage change, especially the low voltage, will affect the internal clock frequency.

9, interrupt

The CH552 chip supports 14 sets of interrupt sources, including 6 sets of interrupts compatible with the standard MCS51: INT0, T0, INT1, T1
UART0, T2, and extended 8 groups of interrupts: SPI0, TKEY, USB, ADC, UART1, PWMX, GPIO, WDOG, where GPIO
The interrupt can be selected from 7 I/O pins.

9.1 Register Description

Table 9.1.1 Interrupt Vector Table

Interrupt source	Ingress address	interrupt number	description	Default priority order
INT_NO_INT0	0x0003	0	External interrupt 0	High priority
INT_NO_TMR0	0x000B	1	Timer 0 interrupt	↓
INT_NO_INT1	0x0013	2	External interrupt 1	↓
INT_NO_TMR1	0x001B	3	Timer 1 interrupt	↓
INT_NO_UART0	0x0023	4	UART0 interrupt	↓
INT_NO_TMR2	0x002B	5	Timer 2 interrupt	↓
INT_NO_SPI0	0x0033	6	SPI0 interrupt	↓
INT_NO_TKEY	0x003B	7	Touch button timer interrupt	↓
INT_NO_USB	0x0043	8	USB interrupt	↓
INT_NO_ADC	0x004B	9	ADC interrupt	↓
INT_NO_UART1	0x0053	10	UART1 interrupt	↓
INT_NO_PWMX	0x005B	11	PWM1/PWM2 interrupt	↓
INT_NO_GPIO	0x0063	12	GPIO interrupt	↓
INT_NO_WDOG	0x006B	13	Watchdog timer interrupt	Low priority

Table 9.1.2 Interrupt related register list

name	address	description	Reset value
IP_EX	E9h	Extended interrupt priority control register	00h
IE_EX	E8h	Extended interrupt enable register	00h
GPIO_IE	C7h	GPIO interrupt enable register	00h
IP	B8h	Interrupt priority control register	00h
IE	A8h	Interrupt enable register	00h

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Interrupt Enable Register (IE):

Bit	name	access	description	Reset value
7	EA	RW	Global interrupt enable control bit, this bit is 1 and E_DIS is 0 to allow interrupts; Bit 0 masks all interrupt requests	0
6	E_DIS	RW	Global interrupt disable control bit, this bit is 1 to mask all interrupt requests; this bit is 0 and And an EA of 1 allows an interrupt. This bit is typically used to temporarily during flash-ROM operations Disable interrupt	0
5	ET2	RW	timer 2 interrupt enable bit, this bit is 1 to enable T2 interrupt; 0 mask	0
4	ES	RW	asynchronous serial port 0 interrupt enable bit, this bit is 1 to enable UART0 interrupt; 0 mask	0
3	ET1	RW	timer 1 interrupt enable bit, this bit is 1 to enable T1 interrupt; 0 mask	0
2	EX1	RW	external interrupt 1 enable bit, this bit is 1 to enable INT1 interrupt; 0 mask	0
1	ET0	RW	timer 0 interrupt enable bit, this bit is 1 to enable T0 interrupt; 0 mask	0
0	EX0	RW	external interrupt 0 enable bit, this bit is 1 to enable INT0 interrupt; 0 mask	0

Extended Interrupt Enable Register (IE_EX):

Bit	name	access	description	Reset value
7	IE_WDOG	RW	Watchdog Timer Interrupt Enable bit, this bit is 1 to allow WDOG interrupt; masked to 0	0
6	IE_GPIO	RW	GPIO interrupt enable bit, this bit is 1 to enable interrupts enabled in GPIO_IE; 0 screen Block all interrupts in GPIO_IE	0
5	IE_PWMX	RW	PWM1/PWM2 interrupt enable bit, this bit is 1 to enable PWM1/2 interrupt; 0 mask	0
4	IE_UART1	RW	asynchronous serial port 1 interrupt enable bit, this bit is 1 to enable UART1 interrupt; 0 mask	0
3	IE_ADC	RW	ADC analog-to-digital conversion interrupt enable bit, this bit is 1 to allow ADC interrupt; 0 mask	0
2	IE_USB	RW	USB interrupt enable bit, this bit is 1 to allow USB interrupt; 0 mask	0
1	IE_TKEY	RW	touch button timer interrupt enable bit, this bit is 1 to allow timed interrupt; 0 mask	0
0	IE_SPI0	RW	SPI0 interrupt enable bit, this bit is 1 to enable SPI0 interrupt; 0 mask	0

GPIO Interrupt Enable Register (GPIO_IE):

Bit	name	access	description	Reset value

7	bIE_IO_EDGE	RW	GPIO Edge Interrupt Mode Enable: This bit is 0 to select the level interrupt mode, and the GPIO pin input is active. bIO_INT_ACT is 1 and always requests an interrupt when the GPIO input is inactive bIO_INT_ACT is 0 and the interrupt request is canceled; This bit is set to 1 to select the edge interrupt mode, which is generated when the GPIO pin inputs a valid edge. Interrupt flag bIO_INT_ACT and request interrupt, the interrupt flag cannot be cleared Zero, can only be in reset or level interrupt mode or enter the corresponding interrupt service Program is automatically cleared	0
6	bIE_RXD1_LO	RW	This bit is 1 to enable the UART1 receive pin interrupt (level mode active low, Edge mode falling edge is valid); this bit is 0 disable. according to bUART1_PIN_X=0/1 selects RXD1 or RXD1_ pin	0
5	bIE_P1_5_LO	RW	This bit is set to 1 to enable the P1.5 interrupt (level mode active low, in edge mode The falling edge is valid); this bit is 0 forbidden	0
4	bIE_P1_4_LO	RW	This bit is set to 1 to enable the P1.4 interrupt (level mode active low, in edge mode The falling edge is valid); this bit is 0 forbidden	0

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3	bIE_P1_3_LO	RW	This bit is 1 to enable the P1.3 interrupt (level mode active low, in edge mode The falling edge is valid); this bit is 0 forbidden	0
2	bIE_RST_HI	RW	This bit is set to 1 to enable the RST interrupt (level mode active high, on edge mode) The rising edge is valid; this bit is 0	0
1	bIE_P3_1_LO	RW	This bit is 1 to enable P3.1 interrupt (level mode active low, in edge mode The falling edge is valid); this bit is 0 forbidden	0
0	bIE_RXD0_LO	RW	This bit is set to 1 to enable the UART0 receive pin interrupt (level mode is active low, Edge mode falling edge is valid); this bit is 0 disable. according to bUART0_PIN_X=0/1 select RXD0 or RXD0_ pin	0

Interrupt Priority Control Register (IP):

Bit	name	access	description	Reset value
7	PH_FLAG	RO	high priority interrupt is executing flag	0
6	PL_FLAG	RO	low priority interrupt is executing flag	0
5	PT2	RW	Timer 2 Interrupt Priority Control Bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer 1 Interrupt Priority Control Bit	0
2	PX1	RW	external interrupt 1 interrupt priority control bit	0
1	PT0	RW	timer 0 interrupt priority control bit	0
0	PX0	RW	Interrupt Priority Control bit for External Interrupt 0	0

Extended Interrupt Priority Control Register (IP_EX):

Bit	name	access	description	Reset value
7	bIP_LEVEL	RO	The current interrupt nesting level flag bit, which is 0 means no interruption or nesting Level 2 interrupt; a 1 in this bit indicates the current nested level 1 interrupt	0
6	bIP_GPIO	RW	GPIO interrupt priority control bit	0
5	bIP_PWMX	RW	PWM1/PWM2 Interrupt Priority Control Bit	0
4	bIP_UART1	RW	UART1 interrupt priority control bit	0
3	bIP_ADC	RW	ADC interrupt priority control bit	0
2	bIP_USB	RW	USB interrupt priority control bit	0
1	bIP_TKEY	RW	touch button timer interrupt priority control bit	0
0	bIP_SPI0	RW	SPI0 interrupt priority control bit	0

The IP and IP_EX registers are used to set the interrupt priority level. If a bit is set, the corresponding interrupt source is set to high priority. If a bit is cleared, the corresponding interrupt source is set to low priority. For peer interrupt sources, the system has a default priority order. The default priority order is shown in Table 9.1.1. The combination of PH_FLAG and PL_FLAG indicates the priority of the current interrupt.

Table 9.1.3 Current Interrupt Priority Status Indicator

PH_FLAG	PL_FLAG	Current interrupt priority status
0	0	Currently uninterrupted
0	1	Currently executing low priority interrupts
1	0	High priority interrupt is currently being executed
1	1	Unexpected state, unknown error

10, I / O port

10.1 Introduction to GPIO

The CH552 provides up to 17 I/O pins, some of which have multiplexing. Where the inputs and outputs of ports P1 and P3 are Can be addressed bit by bit. Port P2 is an internal port and is only used to select xRAM pages for MOVX access with R0 or R1.

If the pin is not configured for multiplexing, the default is the general purpose I/O pin state. When used as a general purpose digital I/O All I/O ports have a true “read-modify-write” function that supports SETB or CLR bit manipulation instructions to independently change certain Pin direction or port level, etc.

10.2 GPIO Register

All registers and bits in this section are represented in a common format: lowercase "n" for port number (n=1 or 3) and lowercase "x" The serial number of the representative digit (x=0, 1, 2, 3, 4, 5, 6, 7).

Table 10.2.1 GPIO Register List

name	address	description	Reset value
P1	90h	P1 port input and output registers	FFh
P1_MOD_OC	92h	P1 port output mode register	FFh
P1_DIR_PU	93h	P1 port direction control and pull-up enable register	FFh
P2	A0h	P2 port output register	FFh
P3	B0h	P3 port input and output registers	FFh
P3_MOD_OC	96h	P3 port output mode register	FFh
P3_DIR_PU	97h	P3 port direction control and pull-up enable register	FFh
PIN_FUNC	C6h	Pin function select register	80h
XBUS_AUX	A2h	Bus auxiliary setting register	00h

Pn port input and output registers (Pn):

Bit	name	access	description	Reset value
[7:0]	Pn.0~Pn.7	RW	Pn.x pin status input and data output bits, bit addressable	FFh

Pn port output mode register (Pn_MOD_OC):

Bit	name	access	description	Reset value
[7:0]	Pn_MOD_OC	RW	Pn.x pin output mode setting: 0-push-pull output; 1-open drain output	FFh

Pn port direction control and pull-up enable register (Pn_DIR_PU):

Bit	name	access	description	Reset value
[7:0]	Pn_DIR_PU	RW	is Pn.x pin direction control in push-pull output mode: 0-input; 1-output; In open-drain output mode, the Pn.x pin pull-up resistor enable control: 0-Pull-up resistor disabled; 1-Enable pull-up resistor	FFh

The Pn port configuration is implemented by a combination of Pn_MOD_OC[x] and Pn_DIR_PU[x], as follows.

Table 10.2.2 Port Configuration Register Combinations

Pn_MOD_OC	Pn_DIR_PU	Working mode description
0	0	High-impedance input mode, no pull-up resistors on the pins
0	1	Push-pull output mode with symmetrical drive capability to output or sink large currents

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1	0	Open-drain output, support for high-impedance input, no pull-up resistor on the pin
1	1	Quasi-bidirectional mode (standard 8051), open-drain output, support input, pin pull-up resistor, when The output automatically drives a high level of 2 clock cycles from low to high to speed up conversion

The P1 and P3 ports support pure input or push-pull output as well as quasi-bidirectional modes. Each pin has an internal pull-up that can be freely controlled The resistors, as well as the protection diodes connected to VCC and GND.

Figure 10.2.1 shows the equivalent schematic of the P1.x pin of the P1 port. It can be applied to the P3 port after AIN is removed. VCC in the figure After changing to V33, it is applicable to P3.6 and P3.7, that is, the pull-up of P3.6 and P3.7 or the input or output high level can only reach V33 voltage.

P3.6 and P3.7 optional standard pull-up resistors (to V33), 15KΩ pull-down resistors, or 1.5KΩ for one of the pins Pull the resistor (to V33). The standard pull-up resistor is only valid in bUSB_IO_EN=0, ie GPIO mode, bit 7 by P3_DIR_PU 6 Control; pull-down resistor controlled by bUD_PD_DIS when bUC_RESET_SIE=0, independent of bUSB_IO_EN; 1.5KΩ strong pull-up The resistance takes precedence over the pull-down resistor and is controlled by bUC_DEV_PU_EN when bUC_RESET_SIE=0, regardless of bUSB_IO_EN.

Figure 10.2.1 I/O pin equivalent schematic

10.4 GPIO Reuse and Mapping

Some of the CH552's I/O pins have an alternate function. After power-on, the default is a general-purpose I/O pin. After different function modules are enabled, the phase is The pins should be configured as function pins corresponding to the respective function modules.

Pin Function Select Register (PIN_FUNC):

Bit	name	access	description	Reset value
7	bUSB_IO_EN	RW	USB UDP/UDM pin enable bit, this bit is 0, then P3.6/P3.7 is used for GPIO. Support P3_DIR_PU control pull-up resistor, support P3_MOD_OC; this bit is 1 Then P3.6/P3.7 is used for UDP/UDM, controlled by USB module, P3_DIR_PU And P3_MOD_OC is invalid for it	1
6	bIO_INT_ACT	R0	GPIO interrupt request activation status: When bIE_IO_EDGE=0, this bit is 1 to indicate the GPIO input active level. Interrupt the request, 0 is the input invalid level; When bIE_IO_EDGE=1, this bit is used as the edge interrupt flag, and 1 is checked. The valid edge is detected. This bit cannot be cleared by software. It can only be reset or level.	0

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Automatically cleared in break mode or when entering the corresponding interrupt service routine

UART1 pin mapping enable bit, this bit is 0, RXD1/TXD1 is used

5	bUART1_PIN_X	RW	P1.6/P1.7; this bit is 1 and RXD1/TXD1 uses P3.4/P3.2	0
4	bUART0_PIN_X	RW	UART0 pin mapping enable bit, this bit is 0 and RXD0/TXD0 is used. P3.0/P3.1; this bit is 1 and RXD0/TXD0 uses P1.2/P1.3	0
3	bPWM2_PIN_X	RW	PWM2 pin mapping enable bit, this bit is 0, PWM2 uses P3.4; this bit is 1 PWM2 uses P3.1	0
2	bPWM1_PIN_X	RW	PWM1 pin mapping enable bit. When this bit is 0, PWM1 uses P1.5; this bit is 1 PWM1 uses P3.0	0
1	bT2EX_PIN_X	RW	T2EX/CAP2 pin mapping enable bit, this bit is 0 and T2EX/CAP2 is used. P1.1; this bit is 1 and T2EX/CAP2 uses RST	0
0	bT2_PIN_X	RW	T2/CAP1 pin mapping enable bit, this bit is 0, then T2/CAP1 uses P1.0; This bit is 1 and T2/CAP1 uses P1.4.	0

Table 10.4.1 GPIO Pin Multiplexing Function List

GPIO	Other features: prioritize from left to right
RST	RST, bT2EX_, bCAP2_, bRST
P1[0]	T2/bT2, CAP1/bCAP1, TIN0, P1.0
P1[1]	T2EX/bT2EX, CAP2/bCAP2, TIN1, VBUS2, AIN0, P1.1
P1[2]	XI, RXD_/bRXD_, P1.2
P1[3]	XO, TXD_/bTXD_, P1.3
P1[4]	T2_/bT2_, CAP1_/bCAP1_, SCS/bSCS, TIN2, UCC1, AIN1, P1.4
P1[5]	MOSI/bMOSI, PWM1/bPWM1, TIN3, UCC2, AIN2, P1.5
P1[6]	MISO/bMISO, RXD1/bRXD1, TIN4, P1.6
P1[7]	SCK/bSCK, TXD1/bTXD1, TIN5, P1.7
P3[0]	PWM1_/bPWM1_, RXD/bRXD, P3.0
P3[1]	PWM2_/bPWM2_, TXD/bTXD, P3.1
P3[2]	TXD1_/bTXD1_, INT0/bINT0, VBUS1, AIN3, P3.2
P3[3]	INT1/bINT1, P3.3
P3[4]	PWM2/bPWM2, RXD1_/bRXD1_, T0/bT0, P3.4
P3[5]	T1/bT1, P3.5
P3[6]	UDP/bUDP, P3.6
P3[7]	UDM/bUDM, P3.7

The priority order from left to right as described in the above table refers to the priority order when multiple functional modules compete for the GPIO. E.g, When P3.1 is used for TXD serial port transmission, P3.0 can still be used for higher priority PWM1 output.

11, external bus

The CH552 does not provide bus signals to the outside of the chip. It does not support the external bus, but can access the on-chip xRAM normally.

External bus auxiliary setting register (XBUS_AUX):

Bit	name	access	description	Reset value
7	bUART0_TX	R0	indicates the transmission status of UART0, and 1 indicates that it is transmitting.	0
6	bUART0_RX	R0	indicates the reception status of UART0, and 1 indicates that it is receiving.	0

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5	bSAFE_MOD_ACT	R0	indicates the security mode status, and 1 indicates that the security mode is currently in use.	0
4	Reserved	RO	reservation	0
3	GF2	RW	Universal Flag 2: User can define it by itself, can be cleared or set by software.	0
2	bDPTR_AUTO_INC	RW	enable DPTR automatically increments after the MOVX_@DPTR instruction is completed	0
1	Reserved	RO	reservation	0
0	DPS	RW	Dual DPTR data pointer selection bits: This bit is 0 to select DPTR0; this bit is 1 to select DPTR1	0

12, timer Timer

12.1 Timer0/1

Timer0/1 is two 16-bit Timer/Event Counters. Timer0 and Timer1 are configured by TCON and TMOD.
Start/overset of T0 and T1 interrupt and overflow interrupt and external interrupt control. Each timer is composed of 2 8-bit register banks

A 16-bit timing unit. The high byte counter of timer 0 is TH0, the low byte is TL0; the high byte counter of timer 1 is

TH1, the low byte is TL1. Timer 1 can also be used as the baud rate generator for UART0.

Table 12.1.1 Timer0/1 Related Register List

name	address	description	Reset value
TH1	8Dh	Timer1 count high byte	Xxh
TH0	8Ch	Timer0 count high byte	Xxh
TL1	8Bh	Timer1 count low byte	Xxh
TL0	8Ah	Timer0 count low byte	Xxh
TMOD	89h	Timer0/1 mode register	00h
TCON	88h	Timer0/1 Control Register	00h

Timer/Event Counter 0/1 Control Register (TCON):

Bit	name	access	description	Reset value
7	TF1	RW	Timer1 overflow interrupt flag, automatically cleared after entering Timer 1 interrupt	0
6	TR1	RW	Timer1 start/stop bit, set to start, set or cleared by software	0
5	TF0	RW	Timer0 overflow interrupt flag bit, automatically cleared after entering timer 0 interrupt	0
4	TR0	RW	Timer0 start/stop bit, set to start, set or cleared by software	0
3	IE1	RW	INT1 Interrupt request flag bit of external interrupt 1, automatically cleared after entering interrupt	0
2	IT1	RW	INT1 external interrupt 1 trigger mode control bit, this bit is 0 select external interrupt is low Level trigger; this bit is 1 select external interrupt for falling edge trigger	0
1	IE0	RW	INT0 Interrupt request flag bit of external interrupt 0, automatically cleared after entering interrupt	0
0	IT0	RW	INT0 external interrupt 0 trigger mode control bit, this bit is 0 select external interrupt is low Level trigger; this bit is 1 select external interrupt for falling edge trigger	0

Timer/Counter 0/1 Mode Register (TMOD):

Bit	name	access	description	Reset value
7	bT1_GATE	RW	The gate enable bit controls whether Timer1 startup is affected by the external interrupt signal INT1 ring. If this bit is 0, the Timer/Event Counter 1 is enabled regardless of INT1; this bit is 1 Then the INT1 pin is high and TR1 is 1 to start.	0
6	bT1_CT	RW	Timing or counting mode selection bit, this bit is 0, working in timing mode; this bit is 1 Operates in counting mode, using the falling edge of the T1 pin as the clock	0

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5	bT1_M1	RW	Timer/Counter 1 mode selects high	0
4	bT1_M0	RW	Timer/Event Counter 1 mode selects low bit	0
3	bT0_GATE	RW	The gate enable bit controls whether Timer0 startup is affected by the external interrupt signal INT0 ring. If this bit is 0, the timer/event counter 0 is enabled regardless of INT0; this bit is 1 Then the INT0 pin is high and TR0 is 1 to start.	0
2	bT0_CT	RW	Timing or counting mode selection bit, this bit is 0, working in timing mode; this bit is 1 Operates in counting mode, using the falling edge of the T0 pin as the clock	0
1	bT0_M1	RW	Timer/Counter 0 mode selects high	0
0	bT0_M0	RW	Timer/Counter 0 mode selects low	0

Table 12.1.2 bTn_M1 and bTn_M0 Select Timern Operating Mode (n=0, 1)

bTn_M1	bTn_M0	Timern working mode (n=0, 1)
0	0	Mode 0: 13-bit timer/counter n, the counting unit consists of the lower 5 bits of TLn and THn, the height of TLn 3 The bit is invalid. When the count changes from 13 bits to all 0s, the overflow flag TFn is set and the initial value needs to be reset.
0	1	Mode 1: 16-bit timer/counter n, the counting unit consists of TLn and THn. Counting from 16 bits to 1 When all becomes 0, the overflow flag TFn is set and the initial value needs to be reset.
1	0	Mode 2: 8-bit reload timer/counter n, the counting unit uses TLn, THn as the reload counting unit. When the count changes from 8 bits to 1 and all 0s, the overflow flag TFn is set and the initial value is automatically loaded from THn.
1	1	Mode 3: If it is timer/counter 0, then the timer/counter 0 is divided into 2 parts TL0 and TH0, TL0 is used as an 8-bit timer/counter, occupies all control bits of Timer0; TH0 also does another Used by 8-bit timers, occupying TR1, TF1 and interrupt resources of Timer1, and Timer1 is still

Available, except that the start control bit TR1 and the overflow flag bit TF1 cannot be used.

In the case of Timer/Event Counter 1, entering Mode 3 will stop Timer/Event Counter 1.

Timern counts the low byte (TLn) (n=0, 1):

Bit	name	access	description	Reset value
[7:0]	TLn	RW	Timern count low byte	Xxh

Timern counts the high byte (THn) (n=0, 1):

Bit	name	access	description	Reset value
[7:0]	THn	RW	Timern count high byte	Xxh

12.2 Timer2

Timer2 is a 16-bit auto-reload timer/counter that is configured with the T2CON and T2MOD registers.

The section counter is TH2 and the low byte is TL2. Timer2 can be used as the baud rate generator of UART0 and has 2 signal level captures.

The capture function, the capture count is stored in the RCAP2 and T2CAP1 registers.

Table 12.2.1 Timer2 Related Register List

name	address	description	Reset value
TH2	CDh	Timer2 counter high byte	00h
TL2	CCh	Timer2 counter low byte	00h
T2COUNT	CCh	TL2 and TH2 form a 16-bit SFR	0000h
T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	Xxh
T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	Xxh
T2CAP1	CEh	T2CAP1L and T2CAP1H form a 16-bit SFR	Xxxxh

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RCAP2H	CBh	Count reload/capture 2 data register high byte	00h
RCAP2L	CAh	Count reload/capture 2 data register low byte	00h
RCAP2	CAh	RCAP2L and RCAP2H form a 16-bit SFR	0000h
T2MOD	C9h	Timer2 mode register	00h
T2CON	C8h	Timer2 Control Register	00h

Timer/Event Counter 2 Control Register (T2CON):

Bit	name	access	description	Reset value
7	TF2	RW	When bT2_CAP1_EN=0, it is the overflow interrupt flag of Timer2, when Timer2 When the count is changed from 1 bit to 1 and all 0s, the overflow flag is set to 1. To clear the software; when RCLK=1 or TCLK=1, this bit will not be set.	0
7	CAP1F	RW	When bT2_CAP1_EN=1, it is the Timer2 capture 1 interrupt flag, valid by T2 Edge triggered, requires software to clear	0
6	EXF2	RW	Timer2 external trigger flag, triggered by T2EX valid edge when EXEN2=1 Set to 1, need software to clear	0
5	RCLK	RW	UART0 receive clock selection, this bit is 0. Select Timer1 overflow pulse to generate wave. Rate; this bit is 1 to select the Timer2 overflow pulse to generate the baud rate.	0
4	TCLK	RW	UART0 transmit clock selection, this bit is 0. Select Timer1 overflow pulse to generate wave. Rate; this bit is 1 to select the Timer2 overflow pulse to generate the baud rate.	0
3	EXEN2	RW	T2EX Trigger Enable bit, this bit is 0, ignore T2EX; this bit is 1 enable at T2EX Trigger overload or capture on valid edges	0
2	TR2	RW	Timer2 start/stop bit, set to start, set or cleared by software	0
1	C_T2	RW	Timer2 clock source select bit, this bit is 0 using the internal clock; this bit is 1 Counting with edges based on the falling edge of the T2 pin	0
0	CP_RL2	RW	Timer2 function select bit, if RCLK or TCLK is 1, then this bit should be strong The system is 0. When this bit is 0, Timer2 acts as a timer/counter and when the counter Automatically reloads the initial value when overflow or T2EX level change; this bit is 1 Enable the Capture 2 function of Timer2 to capture the valid edge of T2EX	0

Timer/Counter 2 Mode Register (T2MOD):

Bit	name	access	description	Reset value
7	bTMR_CLK	RW	The fastest clock mode enable of the T0/T1/T2 timer that has selected the fast clock. Bit 1 uses the system frequency Fsys without division as the count clock; this bit A value of 0 uses a divided clock. This bit has no effect on the timer that selects the standard clock.	0
6	bT2_CLK	RW	Timer2 internal clock frequency selection bit, this bit is 0 standard clock, timing / meter The number mode is Fsys/12, and the UART0 clock mode is Fsys/4; this bit is 1 fast. Speed clock, timing / counting mode is Fsys / 4 (bTMR_CLK = 0) or Fsys (bTMR_CLK=1), UART0 clock mode is Fsys/2 (bTMR_CLK=0) Or Fsys (bTMR_CLK=1)	0
5	bT1_CLK	RW	Timer1 internal clock frequency selection bit, this bit is 0 select standard clock Fsys/12; Select 1 fast clock Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)	0
4	bT0_CLK	RW	Timer0 internal clock frequency selection bit, this bit is 0 select standard clock Fsys/12; Select 1 fast clock Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)	0

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3	bT2_CAP_M1	RW	Timer2 capture mode high	Capture mode selection: X0: from falling edge to falling edge	0
2	bT2_CAP_M0	RW	Timer2 capture mode low	01: From any edge to any edge, that is, level change 11: From rising edge to rising edge	0
1	T2OE	RW	Timer2 clock output enable bit, this bit is 0 disable output; this bit is 1 enable T2 pin output clock at half the rate of Timer2 overflow		0
0	bT2_CAP1_EN	RW	Capture when RCLK=0, TCLK=0, CP_RL2=1, C_T2=0, T2OE=0 1 Mode enable, this bit is 1 Enable Capture 1 function captures T2 active edge; this bit Disable capture for 0 1		0

Count Reload/Capture 2 Data Register (RCAP2):

Bit	name	access	description	Reset value
[7:0]	RCAP2H	RW	In the Timer/Counter mode, it is the high byte of the reload value; in Capture mode it is The high byte of the timer captured by CAP2	00h
[7:0]	RCAP2L	RW	In the Timer/Counter mode, it is the low byte of the reload value; in Capture mode it is The low byte of the timer captured by CAP2	00h

Timer2 counter (T2COUNT):

Bit	name	access	description	Reset value
[7:0]	TH2	RW	current counter high byte	00h
[7:0]	TL2	RW	current counter low byte	00h

Timer2 captures 1 data (T2CAP1):

Bit	name	access	description	Reset value
[7:0]	T2CAP1H	RO	CAP1 High byte of timer captured	Xxh
[7:0]	T2CAP1L	RO	CAP1 Captured low byte of timer	Xxh

12.3 PWM function

The CH552 provides two 8-bit PWMs. The PWM can select the default output polarity to be low or high and can be dynamically modified.

The output duty cycle of the PWM is integrated with low-pass filtering by a simple RC resistor and capacitor to obtain various output voltages, which is equivalent to low Fast digital to analog converter DAC.

PWM1 output duty cycle = PWM_DATA1 / 256, support range 0% to 99.6%.

PWM2 output duty cycle = PWM_DATA2 / 256, support range 0% to 99.6%.

In practical applications, it is recommended to allow the PWM pin output and set the PWM output pin to push-pull output mode.

12.3.1 PWM1 and PWM2

Table 12.3.1 List of PWM1 and PWM2 Related Registers

name	address	description	Reset value
PWM_CK_SE	9Eh	PWM Clock Divider Setting Register	00h
PWM_CTRL	9Dh	PWM Control Register	02h
PWM_DATA1	9Ch	PWM1 Data Register	Xxh
PWM_DATA2	9Bh	PWM2 Data Register	Xxh

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PWM2 data register (PWM_DATA2):

Bit	name	access	description	Reset value
[7:0]	PWM_DATA2	RW	Store PWM2 current data, PWM2 output active level duty cycle = PWM_DATA2 / 256	Xxh

PWM1 data register (PWM_DATA1):

Bit	name	access	description	Reset value
[7:0]	PWM_DATA1	RW	Store the current data of PWM1, PWM1 output active level duty cycle = PWM_DATA1/256	Xxh

PWM Control Register (PWM_CTRL):

Bit	name	access	description	Reset value
7	bPWM_IE_END	RW	This bit is 1 to enable the end of the PWM cycle or the MFM buffer empty interrupt	0
6	bPWM2_POLAR	RW	Control PWM2 output polarity, this bit is 0, the default is low level, high level has Effect; this bit is 1 default high level, active low	0
5	bPWM1_POLAR	RW	Control PWM1 output polarity, this bit is 0, the default is low level, high level has Effect; this bit is 1 default high level, active low	0
4	bPWM_IF_END	RW	The end of the PWM cycle is interrupted. The bit is 1 to indicate that there is an interrupt. 1 Cleared when clearing or reloading PWM_DATA1 data	0
3	bPWM2_OUT_EN	RW	PWM2 output enable, this bit is 1 to enable PWM2 output	0
2	bPWM1_OUT_EN	RW	PWM1 output enable, this bit is 1 to enable PWM1 output	0
1	bPWM_CLR_ALL	RW	This bit is '1' clears the PWM1 and PWM2 counts and FIFOs and requires software clear	0
0	Reserved	RO	reservation	0

PWM clock divider setting register (PWM_CK_SE):

Bit	name	access	description	Reset value
[7:0]	PWM_CK_SE	RW	sets the PWM clock division divisor	00h

12.4 Timer function

12.4.1 Timer0/1

(1) Set T2MOD to select the internal clock frequency of Timer. If bTn_CLK(n=0/1) is 0, then the clock corresponding to Timer0/1 Fsys/12; if bTn_CLK is 1, then Fsys/4 or Fsys is selected as the clock by bTMR_CLK=0 or 1.

(2) Set TMOD to configure the working mode of Timer.

Mode 0: 13-bit timer/counter

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Figure 12.4.1.1 Timer0/1 Mode 0

Mode 1: 16-bit timer/counter

Figure 12.4.1.2 Timer0/1 Mode 1

Mode 2: Automatically reload 8-bit timer/counter

Figure 12.4.1.3 Timer0/1 Mode 2

Mode 3: Timer0 is decomposed into two independent 8-bit timer/counters and borrows the TR1 control bit of Timer1; Timer1 is connected. Whether to start mode 3 instead of the borrowed TR1 control bit, Timer1 enters mode 3 and Timer1 stops running.

Figure 12.4.1.4 Timer0 Mode 3

(3) Set the timer/counter initial values TLn and THn (n=0/1).

(4) Set the bit TRn (n=0/1) in TCON to enable or stop the timer/counter, which can be queried or passed through the bit TFn(n=0/1). The detection is performed in an interrupt mode.

12.4.2 Timer2

Timer2 16-bit reload timer/counter mode:

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(1) Set the bits RCLK and TCLK in T2CON to 0, and select the non-serial port baud rate generator mode.

(2) Set the bit C_T2 in T2CON to 0. Select to use the internal clock, go to step (3); also set to 1 to select the falling edge of the T2 pin.

As the count clock, skip step (3).

(3) Set T2MOD to select the internal clock frequency of Timer. If bT2_CLK is 0, then the clock of Timer2 is Fsys/12;

If bT2_CLK is 1, then Fsys/4 or Fsys is selected as the clock by bTMR_CLK=0 or 1.

(4) Set the bit CP_RL2 of T2CON to 0, and select the 16-bit reload timer/counter function of Timer2.

(5) Set RCAP2L and RCAP2H as the reload value after the timer overflows, and set TL2 and TH2 as the initial values of the timer (generally

RCAP2L is the same as RCAP2H). Set TR2 to 1 to enable Timer2.

(6) The current timer/counter status can be obtained by querying the TF2 or Timer 2 interrupt.

Figure 12.4.2.1 Timer2 16-bit Reload Timer/Counter

Timer2 clock output mode:

Refer to the 16-bit reload timer/counter mode and set the bit T2OE in T2MOD to 1, enabling the output from the T2 pin.

The divide-by-2 clock of the TF2 frequency.

Timer2 serial port 0 baud rate generator mode:

(1) Set the bit C_T2 in T2CON to 0 to select the internal clock, or set the falling edge of the T2 pin as the clock.

Set the bit rate RCLK and TCLK in T2CON to 1 or one of them to 1 to select the serial port baud rate generator mode.

(2) Set T2MOD to select the internal clock frequency of Timer. If bT2_CLK is 0, then the clock of Timer2 is Fsys/4;

If bT2_CLK is 1, then Fsys/2 or Fsys is selected as the clock by bTMR_CLK=0 or 1.

(3) Set RCAP2L and RCAP2H as the reload value after the timer overflows. Set TR2 to 1 to enable Timer2.

Figure 12.4.2.2 Timer2 UART0 Baud Rate Generator

Timer2 dual channel capture mode:

(1) Set the bits RCLK and TCLK in T2CON to 0, and select the non-serial port baud rate generator mode.

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(2) Set the bit C_T2 in T2CON to 0 to select the internal clock, go to step (3); or set it to 1 to select the falling of the T2 pin.

As the count clock, skip step (3).

(3) Set T2MOD to select the internal clock frequency of Timer. If bT2_CLK is 0, then the clock of Timer2 is Fsys/12;

If bT2_CLK is 1, then Fsys/4 or Fsys is selected as the clock by bTMR_CLK=0 or 1.

(4) Set the bits bT2_CAP_M1 and bT2_CAP_M0 of T2MOD to select the corresponding edge capture mode.

(5) Set the bit CP_RL2 of T2CON to 1, and select the capture function of Timer2 to the T2EX pin.

(6) Set TL2 and TH2 to the initial value of the timer, set TR2 to 1, and enable Timer2.

(7) When CAP2 capture is completed, RCAP2L and RCAP2H will save the count values of TL2 and TH2 at that time, and set EXF2 to generate

Interrupt, the difference between the next captured RCAP2L and RCAP2H and the last captured RCAP2L and RCAP2H,

Is the signal width between two valid edges.

(8) If the bit C_T2 in T2CON is 0 and the bit bT2_CAP1_EN in T2MOD is 1, then Timer2 will be enabled at the same time.

For the capture function of the T2 pin, when CAP1 capture is complete, T2CAP1L and T2CAP1H will save the count of TL2 and TH2 at that time.
The value, with CAP1F set, generates an interrupt.

Figure 12.4.2.3 Timer2 Capture Mode

13, Universal Asynchronous Receiver UART

13.1 Introduction to UART

The CH552 chip provides two full-duplex asynchronous serial ports: UART0 and UART1. CH551 only provides UART0.

UART0 is a standard MCS51 serial port whose data reception and transmission is achieved by SBUF access to physically separate receive/transmit registers.
of. The data written to SBUF is loaded into the transmit register, and the read to SBUF corresponds to the receive buffer register.

UART1 simplifies the MCS51 serial port, and its data reception and transmission is realized by SBUF1 accessing physically separate receive/transmit registers.
of. The data written to SBUF1 is loaded into the transmit register, and the read to SBUF1 corresponds to the receive buffer register. Compared to UART1
UART0 has removed the multi-machine communication mode and fixed baud rate, and UART1 has an independent baud rate generator.

13.2 UART Register

Table 13.2.1 List of UART Related Registers

name	address	description	Reset value
SCON	98h	UART0 control register	00h
SBUF	99h	UART0 data register	Xxh

SCON1	C0h	UART1 control register	40h
SBUF1	C1h	UART1 data register	Xxh
SBAUD1	C2h	UART1 baud rate setting register	Xxh

13.2.1 UART0 Register Description

UART0 Control Register (SCON):

Bit	name	access	description	Reset value
7	SM0	RW	UART0 working mode select bit 0, this bit is 0 to select 8-bit data asynchronous communication; this bit is 1 Select 9-bit data asynchronous communication	0
6	SM1	RW	UART0 working mode select bit 1, this bit is 0 set fixed baud rate; this bit is set to 1 Variable baud rate, generated by timer T1 or T2	0
5	SM2	RW	UART0 multi-machine communication control bit: When receiving data in modes 2 and 3, when SM2=1, if RB8 is 0, then RI is not Set to 1, the reception is invalid; if RB8 is 1, then RI is set to 1, the reception is valid; when SM2=0 When RB8 is 0 or 1, the RI is set when receiving data, and the reception is valid. In mode 1, if SM2=1, then the reception is only received when a valid stop bit is received. effective; In mode 0, the SM2 bit must be set to 0.	0
4	REN	RW	UART0 allows the reception of control bits, which is 0 to disable reception; this bit is 1 to allow reception	0

3	TB8	RW	Bit 9 of the transmitted data, TB8 is used to write the 9th of the transmitted data in modes 2 and 3. Bit, which can be a parity bit; in multi-machine communication, it is used to indicate that the host is transmitting the ground. The address byte is also the data byte, TB8=0 is the data, TB8=1 is the address	0
2	RB8	RW	The 9th bit of the received data, in modes 2 and 3, RB8 is used to store the 9th of the received data. Bit; in mode 1, if SM2=0, then RB8 is used to store the received stop bit; In mode 0, RB8 is not used	0
1	TI	RW	Transmit interrupt flag bit, set by hardware after a data byte is sent, requires software clear zero	0
0	RI	RW	Receive interrupt flag bit, set by hardware after a data byte is valid, software required Clear	0

Table 13.2.1.1 UART0 Working Mode Selection

SM0	SM1	description
0	0	Mode 0, shift register mode, baud rate fixed is Fsys/12
0	1	Mode 1, 8-bit asynchronous communication mode, variable baud rate, generated by timer T1 or T2
1	0	Mode 2, 9-bit asynchronous communication, baud rate is Fsys/128 (SMOD=0) or Fsys/32 (SMOD=1)
1	1	Mode 3, 9-bit asynchronous communication, variable baud rate, generated by timer T1 or T2

In modes 1 and 3, when RCLK=0 and TCLK=0, the UART0 baud rate is generated by timer T1. Should set T1 to
Mode 2 automatically reloads the 8-bit timer mode. Both bT1_CT and bT1_GATE must be 0, which are divided into the following types of clock conditions.

Table 13.2.1.2 Calculation Formula for UART0 Baud Rate Generated by T1

bTMR_CLK	bT1_CLK	SMOD	description
1	1	0	TH1 = 256 - Fsys / 32 / baud rate
1	1	1	TH1 = 256 - Fsys / 16 / baud rate
0	1	0	TH1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	TH1 = 256 - Fsys / 4 / 16 / baud rate

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X	0	0	TH1 = 256 - Fsys / 12 / 32 / baud rate
X	0	1	TH1 = 256 - Fsys / 12 / 16 / baud rate

In modes 1 and 3, when RCLK=1 or TCLK=1, the UART0 baud rate is generated by timer T2. Should set T2 to
The 16-bit automatic re-carrier rate generator mode, C_T2 and CP_RL2 must both be 0, divided into the following types of clock conditions.

Table 13.2.1.3 Calculation Formula for UART0 Baud Rate Generated by T2

bTMR_CLK	bT2_CLK	description
1	1	RCAP2 = 65536 - Fsys / 16 / baud rate
0	1	RCAP2 = 65536 - Fsys / 2 / 16 / baud rate
X	0	RCAP2 = 65536 - Fsys / 4 / 16 / baud rate

UART0 Data Register (SBUF):

Bit	name	access	description	Reset value
[7:0]	SBUF	RW	UART0 data register, including two physically separate registers for transmission and reception Device. Write data to SBUF corresponding to the transmit data register; read data from SBUF Corresponding receive data register	Xxh

13.2.2 UART1 Register Description

UART1 Control Register (SCON1):

Bit	name	access	description	Reset value
7	U1SM0	RW	UART1 working mode selection bit, this bit is 0 to select 8-bit data asynchronous communication; this bit is 1 Select 9-bit data asynchronous communication	0
6	Reserved	RO	reservation	1
5	U1SMOD	RW	Selects the communication baud rate of UART1: 0-slow mode; 1-fast mode	0
4	U1REN	RW	UART1 allows the reception of control bits, which is 0 to disable reception; this bit is 1 to allow reception	0
3	U1TB8	RW	The 9th bit of the transmitted data, in the 9-bit data mode, the TB8 is used to write the data to be transmitted. 9 bits, which can be parity; TB8 is ignored in 8-bit data mode	0

2	U1RB8	RW	The 9th bit of the received data, in the 9-bit data mode, the RB8 is used to store the received data 9 bits; RB8 is used to store received stop bits in 8-bit data mode	0
1	U1TI	RW	Transmit interrupt flag bit, set by hardware after a data byte is sent, requires software clear zero	0
0	U1RI	RW	Receive interrupt flag bit, set by hardware after a data byte is valid, software required Clear	0

The UART1 baud rate is generated by the SBAUD1 setting and is divided into two cases based on the U1SMOD selection:

When U1SMOD=0, SBAUD1 = 256 - Fsys / 32 / baud rate;

When U1SMOD=1, SBAUD1 = 256 - Fsys / 16 / baud rate.

UART1 Data Register (SBUF1):

Bit	name	access	description	Reset value
[7:0]	SBUF1	RW	UART1 data register, including two physically separate registers for transmission and reception Device. Write data to SBUF1 corresponding to the transmit data register; read from SBUF1 Corresponding receive data register	XXh

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13.3 UART Application

UART0 application:

(1) Select the baud rate generator of UART0, you can choose from the timer T1 or T2, and configure the corresponding counter.

(2) Turn on the timer T1 or T2.

(3) Set SM0, SM1, SM2 of SCON to select the working mode of serial port 0. Set REN to 1 to enable UART0 reception.

(4), you can set the serial port interrupt or query the RI and TI interrupt status.

(5), read and write SBUF to achieve serial data transmission and reception, the allowable baud rate error of the serial port receiving signal is not more than 2%.

UART1 application:

(1) Select U1SMOD according to the baud rate and set SBAUD1.

(2) Set U1SM0 of SCON1 to select the working mode of serial port 1. Set U1REN to 1 to enable UART1 reception.

(3), you can set the serial port 1 interrupt or query the U1RI and U1TI interrupt status.

(4), read and write SBUF1 to achieve serial port 1 data transmission and reception, the allowable baud rate error of the serial port receiving signal is not more than 2%.

14, synchronous serial interface SPI

14.1 Introduction to SPI

The CH552 chip provides an SPI interface for high-speed synchronous data transfer with peripherals.

(1), support master host mode and slave slave mode;

(2), support mode 0 and mode 3 clock mode;

(3), optional 3-wire full-duplex or 2-wire half-duplex mode;

(4), the optional MSB high bit is sent first or the LSB low bit is sent first;

(5), the clock frequency is adjustable, up to nearly half of the system's main frequency;

(6), built-in 1 byte receive FIFO and 1 byte transmit FIFO;

(7) Support the first byte preload data in slave mode, so that the host can get the return data immediately in the first byte.

14.2 SPI Register

Table 14.2.1 SPI Related Register List

name	address	description	Reset value
SPI0_SETUP	FCh	SPI0 setup register	00h
SPI0_S_PRE	FBh	SPI0 Slave Mode Preset Data Register	20h
SPI0_CK_SE	FBh	SPI0 clock divider setting register	20h
SPI0_CTRL	FAh	SPI0 Control Register	02h
SPI0_DATA	F9h	SPI0 Data Transceiver Register	Xxh
SPI0_STAT	F8h	SPI0 Status Register	08h

SPI0 setting register (SPI0_SETUP):

Bit	name	access	description	Reset value
7	bS0_MODE_SLV	RW	SPI0 master-slave mode select bit, this bit is 0 and SPI0 is in master mode; Bit 1 is SPI0 is slave mode / device mode	0
6	bS0_IE_FIFO_OV	RW	FIFO overflow interrupt enable bit in slave mode, this bit is 1 enable FIFO Overflow interrupt; this bit is 0, FIFO overflow does not generate an interrupt	0
5	bS0_IE_FIRST	RW	Receive the first byte completion interrupt enable bit in slave mode, this bit is 1 slave The interrupt is triggered when the first data byte is received in the mode; if the bit is 0, the connection is No interrupt is generated when the first byte is received	0

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4	bS0_IE_BYTE	RW	Data byte transfer complete interrupt enable bit, this bit is 1 to allow byte transfer Interrupt; this bit is 0, the byte transfer is completed without interrupt	0
3	bS0_BIT_ORDER	RW	The bit order control bit of the data byte. If the bit is 0, the MSB high bit is first; this bit 1 for the LSB low	0
2	Reserved	RO	reservation	0
1	bS0_SLV_SELT	R0	In the slave mode, the chip selects the active status bit. If the bit is 0, it is not currently selected. Medium; this bit is 1 indicating that it is currently selected	0
0	bS0_SLV_PRELOAD	R0	Preload data status bit in slave mode, this bit is 1 indicating that it is currently in the slice Preload status after the selection is valid and before the data has been transferred	0

SPI0 clock division setting register (SPI0_CK_SE):

Bit	name	access	description	Reset value
[7:0]	SPI0_CK_SE		Set SPI0 clock division factor in RW host mode	20h

SPI0 slave mode preset data register (SPI0_S_PRE):

Bit	name	access	description	Reset value
[7:0]	SPI0_S_PRE		RW preloaded first transfer data in slave mode	20h

SPI0 Control Register (SPI0_CTRL):

Bit	name	access	description	Reset value
7	bS0_MISO_OE	RW	MISO output enable control bit for SPI0, this bit is 1 enable output; this bit 0 forbidden output	0
6	bS0_MOSI_OE	RW	The MOSI output enable control bit of SPI0, this bit is 1 enable output; this bit 0 forbidden output	0
5	bS0_SCK_OE	RW	SCK output enable control bit of SPI0, this bit is 1 enable output; this bit 0 forbidden output	0
4	bS0_DATA_DIR	RW	SPI0 data direction control bit, this bit is 0 to output data, only write FIFO As a valid operation, initiate an SPI transfer; this bit is 1 to enter data. Write or read FIFO as a valid operation, start an SPI transfer	0
3	bS0_MST_CLK	RW	SPI0 master clock mode control bit, this bit is 0, mode 0, SCK is idle Default low level; this bit is 1 mode 3, SCK default high level	0
2	bS0_2_WIRE	RW	2-line half-duplex mode enable bit for SPI0, this bit is 0, 3-wire full-duplex Mode, including SCK, MOSI, MISO; this bit is 1 2-line half-duplex Style, including SCK, MISO	0
1	bS0_CLR_ALL	RW	This bit is '1' clears the SPI0 interrupt flag and FIFO and requires software clear	1
0	bS0_AUTO_IF	RW	Allows automatic clearing of the byte receive completion interrupt flag by FIFO active operation Enable bit, this bit is 1 and is automatically cleared when the FIFO is valid for read and write operations. Byte reception completion interrupt flag S0_IF_BYTE	0

SPI0 Data Transceiver Register (SPI0_DATA):

Bit	name	access	description	Reset value
[7:0]	SPI0_DATA	RW	Including sending and receiving two physically separate FIFOs, corresponding to read operations Receive data FIFO; write operation corresponds to send data FIFO, valid read and write operations	Xxh

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Can initiate an SPI transfer

SPI0 Status Register (SPI0_STAT):

Bit	name	access	description	Reset value
7	S0_FST_ACT	R0	This bit is 1 to indicate that the current state is the first byte received in slave mode.	0
6	S0_IF_OV	RW	FIFO overflow flag in slave mode, this bit is 1 for FIFO overflow Break; this bit is 0 without interruption. Direct bit access clear or write 1 clear. when When bS0_DATA_DIR=0, the interrupt is triggered by the transmit FIFO null; when Interrupt interrupted by receive FIFO when bS0_DATA_DIR=1	0
5	S0_IF_FIRST	RW	Receive the first byte completion interrupt flag bit in slave mode, this bit is 1 to indicate Received the first byte. Direct bit access clear or write 1 clear	0
4	S0_IF_BYTE	RW	Data byte transfer completion interrupt flag, this bit is 1 to indicate a byte The transfer is complete. Direct bit access clear or write 1 clear, or Cleared by FIFO valid operation when bS0_AUTO_IF=1	0
3	S0_FREE	R0	SPI0 idle flag, this bit is 1 means there is no SPI shift currently. Often in the gap between data bytes	1
2	S0_T_FIFO	R0	SPI0 Transmit FIFO count, valid value is 0 or 1	0
1	Reserved	R0	reserved	0
0	S0_R_FIFO	R0	SPI0 Receive FIFO count, valid value is 0 or 1	0

14.3 SPI Transfer Format

SPI master mode supports both mode 0 and mode 3 transfer formats, which can be set by setting the SPI control register SPIn_CTRL

The bit bSn_MST_CLK is selected and CH552 always samples MISO data on the rising edge of CLK. The data transfer format is shown below.

Mode 0: bSn_MST_CLK = 0

Figure 14.3.1 SPI Mode 0 Timing Diagram

Mode 3: bSn_MST_CLK = 1

Figure 14.3.2 SPI Mode 3 Timing Diagram

14.4 SPI Configuration

14.4.1 SPI Host Mode Configuration

In SPI master mode, the SCK pin outputs the serial clock and the chip select output pin can be designated as any I/O pin.

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SPI0 configuration steps:

(1) Set the SPI clock divider setting register SPI0_CK_SE to configure the SPI clock frequency.
(2) Set the bit bS0_MODE_SLV of the SPI setting register SPI0_SETUP to 0 and configure it to master mode.
(3) Set the bit bS0_MST_CLK of the SPI control register SPI0_CTRL to set to mode 0 or 3 according to requirements.
(4) Set the bits bS0_SCK_OE and bS0_MOSI_OE of the SPI control register SPI0_CTRL to 1, and the bS0_MISO_OE bit to 0.
Set the P1 port direction bSCK, bMOSI as the output, bMISO as the input, and the chip select pin as the output.

Data transmission process:
(1) Write the SPI0_DATA register, write the data to be sent to the FIFO, and automatically initiate an SPI transfer.
(2) Wait for S0_FREE to be 1, indicating that the transmission is complete and you can continue to send the next byte.

Data receiving process:
(1) Write the SPI0_DATA register and write any data such as 0FFh to the FIFO to initiate an SPI transfer.
(2) Wait for S0_FREE to be 1, indicating that the reception is complete, you can read SPI0_DATA to get the received data.
(3) If the previous bS0_DATA_DIR has been set, the above read operation will also start the next SPI transfer, otherwise it will not start.

14.4.2 SPI Slave Mode Configuration

Only SPI0 supports slave mode. In slave mode, the SCK pin is used to receive the serial clock of the connected SPI master.
(1) Set the bit bS0_MODE_SLV of the SPI0 setting register SPI0_SETUP to 1, and configure it to the slave mode.
(2) Set the bits bS0_SCK_OE and bS0_MOSI_OE of the SPI0 control register SPI0_CTRL to 0, and set bS0_MISO_OE to
1. Set the P1 port direction bSCK, bMOSI and bMISO and the chip select pin as inputs. When SCS chip selection is valid (low power
When it is flat, MISO will automatically enable the output. It is also recommended to set the MISO pin to high-impedance input mode (P1_MOD_OC[6]=0,
P1_DIR_PU[6]=0), so that MISO does not output during chip select invalid, which is convenient for sharing the SPI bus.
(3) Optionally, set the SPI slave mode preset data register SPI0_S_PRE for the first time automatically loaded into the buffer after being selected by the chip.
Used for external output. After 8 serial clocks, that is, the first data byte transmission is completed, CH552 gets the external SPI.
The first byte of data sent by the host (probably the command code), the external SPI host exchanges the preset data in SPI0_S_PRE (can
Can be the status value). Bit 7 of register SPI0_S_PRE will be automatically loaded during SCK low after SPI Chip Select is active
On the MISO pin, for SPI Mode 0, if CH552 is preset with Bit 7 of SPI0_S_PRE, the external SPI master will
When the SPI chip select is valid but data has not been transferred, the bit 7 of SPI0_S_PRE can be obtained by querying the MISO pin.
The value is set so that the value of bit 7 of SPI0_S_PRE can be obtained by only validating the SPI chip select.

Data transmission process:
Query S0_IF_BYTE or wait for an interrupt. After each SPI data byte transfer is completed, write the SPI0_DATA register to
The FIFO writes the data to be sent. Or wait for S0_FREE to change from 0 to 1, and continue to send the next byte.

Data receiving process:
Query S0_IF_BYTE or wait for an interrupt. After each SPI data byte transfer is completed, read the SPI0_DATA register.
The FIFO gets the received data. Query the S0_R_FIFO to see if there are any remaining bytes in the FIFO.

15. Analog-to-Digital Converter ADC and Voltage Comparator (CH551 is not applicable)

15.1 Introduction to ADC

The CH552 provides an 8-bit analog-to-digital converter that includes a voltage comparator and an ADC module. The converter has 4 simulations
The signal input channel can be time-separated and supports the 0 to VCC analog input voltage range.

15.2 ADC Register

Table 15.2.1 List of ADC Related Registers

name	address	description	Reset value
ADC_CTRL	80h	ADC control register	X0h
ADC_CFG	9AH	ADC configuration register	00h
ADC_DATA	9Fh	ADC data register	Xxh

ADC Control Register (ADC_CTRL):

Bit	name	access	description	Reset value

7	CMPO	RO	Voltage comparator result output bit, this bit is 0, indicating the positive phase input The voltage is lower than the voltage at the inverting input; this bit is 1 indicating the positive phase The voltage at the input is higher than the voltage at the inverting input	x
6	CMP_IF	RW	Voltage comparator result change flag, this bit is 1 for voltage comparison The result of the change has changed, direct bit access clear	0
5	ADC_IF	RW	ADC conversion completion interrupt flag, this bit is 1 for one ADC conversion Change completed, direct bit access clear	0
4	ADC_START	RW	ADC start control bit, set to 1 to initiate an ADC conversion, this bit is Automatically clear after ADC conversion is complete	0
3	CMP_CHAN	RW voltage comparator inverting input selection: 0-AIN1; 1-AIN3		0
2	Reserved	R0 reserved		0
1	ADC_CHAN1	RW voltage comparator positive input and ADC input channel select high		0
0	ADC_CHAN0	RW voltage comparator positive input and ADC input channel select low		0

The voltage comparator non-inverting input and ADC channel are selected by ADC_CHAN1 and ADC_CHAN0.

ADC_CHAN1	ADC_CHAN0	Select voltage comparator non-inverting input and ADC input channel
0	0	AIN0 (P1.1)
0	1	AIN1 (P1.4)
1	0	AIN2 (P1.5)
1	1	AIN3 (P3.2)

ADC Configuration Register (ADC_CFG):

Bit	name	access	description	Reset value
[7:4]	Reserved	R0 reserved		0000b
3	ADC_EN	RW	The power control bit of the ADC module. This bit is 0 to turn off the ADC mode. The power of the block goes to sleep; this bit is 1 to turn on	0
2	CMP_EN	RW	Power comparator control bit, this bit is 0 to indicate the turn-off voltage The comparator's power supply goes to sleep; this bit is 1 for open	0
1	Reserved	R0 reserved		0
0	ADC_CLK	RW	ADC reference clock frequency selection bit, this bit is 0 to select slow clock, 384 Fosc cycles per ADC; this bit is 1 for fast time Clock, 96 Fosc cycles per ADC	0

ADC Data Register (ADC_DATA):

Bit	name	access	description	Reset value

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[7:0]	ADC_DATA	RO ADC sampling result data	Xxh

15.3 ADC Features

ADC sampling mode configuration steps:

(1) Set the ADC_EN bit in the ADC_CFG register to 1, turn on the ADC module, and set the bADC_CLK selection frequency.

(2) Set ADC_CHAN1/0 in the ADC_CTRL register to select the input channel.

(3) Optional, clear the interrupt flag ADC_IF. Optionally, if you use interrupt mode, you also need to enable interrupts here.

(4) Set ADC_START in the ADC_CTRL register to start an ADC conversion.

(5) Wait for ADC_START to become 0, or ADC_IF is set to 1 (if it was previously cleared), indicating that the ADC conversion is complete, can pass
ADC_DATA reads the result data. This data is the value of the input voltage relative to the 255 aliquot of the VCC supply voltage, for example, the junction
The data is 47, indicating that the input voltage is close to 47/255 of the VCC voltage. If the VCC supply voltage is also undefined, then
Another determined reference voltage value is measured, and the measured input voltage value and the VCC power supply voltage value are calculated proportionally.

(6) If the ADC_START is set again, the next ADC conversion can be started.

Voltage comparator mode configuration steps:

(1) Set the CMP_EN bit in the ADC_CFG register to 1, and turn on the voltage comparator module.

(2) Set ADC_CHAN1/0 and CMP_CHAN in the ADC_CTRL register to select the positive and negative inputs.

(3), optional, clear flag CMP_IF.

(4) The status of the CMPO bit can be queried at any time to obtain the result of the current comparator.
(5) If CMP_IF becomes 1, it means that the result of the comparator has changed.

The above selected analog signal input channel, where the GPIO pin is located must be set to high-impedance input mode, or open-drain output mode and It is in the state of output 1 (equivalent to high-impedance input), Pn_DIR_PU[x]=0, and it is recommended to turn off the pull-up and pull-down resistors.

16, USB controller

16.1 Introduction to the USB Controller

The CH552 has a built-in USB controller and USB transceiver with the following features:

(1) Support USB Device device function, support USB 2.0 full speed 12Mbps or low speed 1.5Mbps;

(2) Support USB control transmission, batch transmission, interrupt transmission, synchronization/real-time transmission;

(3) Supports up to 64 bytes of data packets, built-in FIFO, support for interrupts and DMA.

The CH552's USB related registers are divided into two sections: the USB Global Register and the USB Endpoint Register.

16.2 Global Registers

Table 16.2.1 USB Global Register List (marked gray is controlled by bUC_RESET_SIE reset)

name	address	description	Reset value
USB_C_CTRL	91h	USB type-C configuration channel control register	0000 0000b
USB_INT_FG	D8h	USB Interrupt Flag Register	0010 0000b
USB_INT_ST	D9h	USB Interrupt Status Register (Read Only)	00xx xxxxb
USB_MIS_ST	DAh	USB Miscellaneous Status Register (Read Only)	Xx10 1000b
USB_RX_LEN	DBh	USB Receive Length Register (Read Only)	0xxx xxxxb
USB_INT_EN	E1h	USB Interrupt Enable Register	0000 0000b
USB_CTRL	E2h	USB Control Register	0000 0110b
USB_DEV_AD	E3h	USB Device Address Register	0000 0000b

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USB type-C configuration channel control register (USB_C_CTRL): (CH551 not applicable)

Bit	name	access	description	Reset value
7	bVBUS2_PD_EN	RW	This bit is 1 to enable the internal 10K pull-down resistor on the VBUS2 pin; 0 is disabled	0
6	bUCC2_PD_EN	RW	This bit is 1 to enable the internal 5.1K pull-down resistor of the UCC2 pin; 0 is disabled	0
5	bUCC2_PU1_EN	RW	This bit is the internal pull-up resistor control select high of the UCC2 pin.	0
4	bUCC2_PU0_EN	RW	This bit is the internal pull-up resistor control low select for the UCC2 pin.	0
3	bVBUS1_PD_EN	RW	This bit is 1 to enable the internal 10K pull-down resistor of the VBUS1 pin; 0 is disabled	0
2	bUCC1_PD_EN	RW	This bit is 1 to enable the internal 5.1K pull-down resistor of the UCC1 pin; 0 is disabled	0
1	bUCC1_PU1_EN	RW	This bit is the internal pull-up resistor control high select for the UCC1 pin.	0
0	bUCC1_PU0_EN	RW	This bit is the internal pull-up resistor control low select for the UCC1 pin.	0

The pull-up resistor inside the UCCn pin is selected by bUCCn_PU1_EN and bUCCn_PU0_EN.

bUCCn_PU1_EN	bUCCn_PU0_EN	Select the pull-up resistor inside the UCCn pin
0	0	Disable internal pull-up resistor
0	1	Enable internal 56KΩ pull-up resistor to provide default USB current
1	0	Enable internal 22KΩ pull-up resistor to indicate 1.5A current
1	1	Enable internal 10KΩ pull-up resistor to indicate 3A current

The above USB type-C pull-up and pull-down resistors are controlled independently of the Pn_DIR_PU port direction control and pull-up enable register.
Port pull-up resistor, when a pin is used for USB type-C, the corresponding port pull-up resistor should be disabled for this pin.
The pin enables the high-impedance input mode (avoid the pin output low or high).

Refer to the USB type-C application notes and routines for detailed control and input detection of the USB type-C configuration channel.

USB interrupt flag register (USB_INT_FG):

Bit	name	access	description	Reset value
7	U_IS_NAK	RO	A 1 in this bit indicates that a NAK busy response was received during the current USB transfer; A bit of 0 indicates that a non-NAK response was received	0

6	U_TOG_OK	RO	Current USB transfer DATA0/1 sync flag match status, this bit is 1 Synchronous, data is valid; this bit is 0 means not synchronized, data may be invalid	0
5	U_SIE_FREE	RO	Idle status bit of the USB protocol processor, this bit is 0 for busy, ongoing USB transfer; this bit is 1 for USB idle	1
4	UIF_FIFO_OV	RW	USB FIFO overflow interrupt flag, this bit is 1 for FIFO overflow interrupt; This bit is 0 without interruption. Direct bit access clear or write 1 clear	0
3	Reserved	RO reservation		0
2	UIF_SUSPEND	RW	USB bus suspend or wake event interrupt flag, this bit is 1 for medium Broken, this interrupt is triggered by a USB suspend event or wakeup event; this bit is 0 No interruption. Direct bit access clear or write 1 clear	0
1	UIF_TRANSFER	RW	USB transfer completion interrupt flag, this bit is 1 to indicate an interrupt, the interrupt is A USB transfer is completed; this bit is 0 for no interrupt. Direct visit Q clear or write 1 clear	0
0	UIF_BUS_RST	RW	USB bus reset event interrupt flag bit, this bit is 1 means there is an interrupt, the middle The break is triggered by a USB bus reset event; a 0 in this bit indicates no interrupt direct Bit access clear or write 1 clear	0

USB Interrupt Status Register (USB_INT_ST):

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Bit	name	access	description	Reset value
7	bUIS_IS_NAK	RO	A 1 in this bit indicates that a NAK busy response was received during the current USB transfer. Same as U_IS_NAK	0
6	bUIS_TOG_OK	RO	Current USB transfer DATA0/1 sync flag match status, this bit is 1 Indicates synchronization; a 0 in this bit indicates no synchronization. Same as U_TOG_OK	0
5	bUIS_TOKEN1	RO	Token PID ID of the current USB transfer transaction	x
4	bUIS_TOKEN0	R0	Token PID ID of the current USB transfer transaction low	x
[3:0]	MASK_UIS_ENDP	RO	The endpoint number of the current USB transfer transaction, 0000 represents the endpoint 0;...; 1111 indicates endpoint 15	Xxxxb

bUIS_TOKEN1 and bUIS_TOKEN0 form MASK_UIS_TOKEN, which is used to identify the token PID of the current USB transfer transaction: 00 means OUT package; 01 means SOF package; 10 means IN package; 11 means SETUP package.

USB Miscellaneous Status Register (USB_MIS_ST):

Bit	name	access	description	Reset value
[7:6]	Reserved	RO reservation		Xxb
5	bUMS_SIE_FREE	RO	Idle status bit of the USB protocol processor, this bit is 0 for busy, positive USB transfer is in progress; this bit is 1 for USB idle. with U_SIE_FREE	1
4	bUMS_R_FIFO_RDY	RO	USB Receive FIFO Data Ready Status bit, this bit is 0 for reception FIFO is empty; this bit is 1 to indicate that the receive FIFO is not empty	0
3	bUMS_BUS_RESET	RO	USB bus reset status bit, this bit is 0 means there is currently no USB total Line reset; this bit is 1 indicating that the USB bus is currently reset	1
2	bUMS_SUSPEND	RO	USB suspend status bit, this bit is 0 to indicate that there is currently USB activity; A bit of 1 indicates that there has been no USB activity for a while, requesting to hang	0
[1:0]	Reserved	RO reservation		00b

USB Receive Length Register (USB_RX_LEN):

Bit	name	access	description	Reset value
[7:0]	bUSB_RX_LEN	RO	The number of bytes of data received by the current USB endpoint	Xxh

USB interrupt enable register (USB_INT_EN):

Bit	name	access	description	Reset value
7	bUIE_DEV_SOF	RW	This bit is 1 to enable reception of SOF packet interrupt; 0 is disabled	0
6	bUIE_DEV_NAK	RW	This bit is 1 to enable the reception of a NAK interrupt; 0 is disabled	0
5	Reserved	RO reservation		0

4	bUIE_FIFO_OV	RW This bit is 1 to enable the FIFO overflow interrupt; this bit is 0 disable enable	0
3	Reserved	RO reservation	0
2	bUIE_SUSPEND	RW This bit is 1 to enable USB bus suspend or wake event interrupt; 0 is disabled	0
1	bUIE_TRANSFER	RW This bit is 1 to enable USB transfer completion interrupt; this bit is 0 disable	0
0	bUIE_BUS_RST	RW This bit is 1 to enable the USB bus reset event interrupt; this bit is 0 disable	0

USB Control Register (USB_CTRL):

Bit	name	access	description	Reset value

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7	Reserved	RO reservation		0
6	bUC_LOW_SPEED	RW	USB bus signal transmission rate selection bit, this bit is 0 to select full speed 12Mbps; This bit is 1 select low speed 1.5Mbps	0
5	bUC_DEV_PU_EN	RW	USB device enable and internal pull-up resistor control bits, this bit enables USB Device transfer and enable internal pull-up resistor	0
5	bUC_SYS_CTRL1	RW USB system control high		0
4	bUC_SYS_CTRL0	RW USB system controls low position		0
3	bUC_INT_BUSY	RW	The USB transfer completion interrupt flag is automatically cleared before it is cleared. This bit is 1 is automatically paused before the interrupt flag UIF_TRANSFER is cleared. The response is busy with NAK; if the bit is 0, it is not suspended.	0
2	bUC_RESET_SIE	RW	USB protocol processor software reset control bit, this bit is 1 to force reset USB Protocol processor and most USB control registers, need to be cleared by software	1
1	bUC_CLR_ALL	RW This bit is 1 to clear the USB interrupt flag and FIFO, which requires software clear		1
0	bUC_DMA_EN	RW This bit is 1 enables USB DMA and DMA interrupts; 0 disables enable		0

The USB system control combination consists of bUC_SYS_CTRL1 and bUC_SYS_CTRL0:

bUC_SYS_CTRL1	bUC_SYS_CTRL0	USB system control description
0	0	Disable USB device function, turn off internal pull-up resistor
0	1	Enable USB device function, turn off internal pull-up, add external pull-up
1	X	Enable the USB device function to enable the internal 1.5KΩ pull-up resistor. This pull-up resistor takes precedence over the pull-down resistor and can also be used in GPIO mode.

USB device address register (USB_DEV_AD):

Bit	name	access	description	Reset value
7	bUDA_GP_BIT	RW USB universal flag: user-definable, software clear or set		0
[6:0]	MASK_USB_ADDR	RW Address of the USB device		00h

16.3 Endpoint Register

CH552 provides five sets of bidirectional endpoints for endpoints 0, 1, 2, 3, and 4. The maximum packet length for all endpoints is 64 bytes.

Endpoint 0 is the default endpoint and supports control transfers. Send and receive share a 64-byte data buffer.

Endpoint 1, Endpoint 2, Endpoint 3 each include a transmitting endpoint IN and a receiving endpoint OUT, each of which has a unique transmission and reception.
A 64-byte or dual 64-byte data buffer that supports control transfers, bulk transfers, interrupt transfers, and real-time/synchronous transfers.

Endpoint 4 includes a transmit endpoint IN and a receive endpoint OUT, each with a separate 64-byte data buffer.
Punch zone, support control transfer, bulk transfer, interrupt transfer and real-time / synchronous transfer.

Each group of endpoints has a control register UEPn_CTRL and a transmit length register UEPn_T_LEN (n=0/1/2/3/4).
Set the synchronization trigger bit of the endpoint, the response to the OUT transaction and the IN transaction, and the length of the transmitted data.

The USB bus pull-up resistor necessary as a USB device can be set by software at any time, whether it is enabled or not, when the USB control register
When bUC_DEV_PU_EN in USB_CTRL is set to 1, CH552 is internally used as the DP pin of the USB bus according to bUD_LOW_SPEED or
The DM pin is connected to a pull-up resistor and the USB device function is enabled.

When a USB bus reset, USB bus suspend or wake event is detected, or when USB successfully processes data transmission or data
After receiving, the USB protocol processor will set the corresponding interrupt flag and generate an interrupt request. The application can be queried directly or on USB
Query and analyze the interrupt flag register USB_INT_FG in the interrupt service routine, according to UIF_BUS_RST and UIF_SUSPEND
Should be handled; and, if UIF_TRANSFER is valid, then you need to continue to analyze the USB interrupt status register USB_INT_ST,
Corresponding processing is performed according to the current endpoint number MASK_UIS_ENDP and the current transaction token PID identifier MASK_UIS_TOKEN. If something
First set the synchronization trigger bit bUEP_R_TOG of the OUT transaction of each endpoint, then you can pass U_TOG_OK or bUIS_TOG_OK

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Determining whether the synchronization trigger bit of the currently received data packet matches the synchronization trigger bit of the endpoint, and if the data is synchronized, the data Valid; if the data is out of sync, the data should be discarded. Every time you finish processing USB transmission or receiving interrupt, you should correct it correctly.
Changing the synchronization trigger bit of the corresponding endpoint, for synchronizing the data packet sent next time and detecting whether the data packet received next time is synchronized
In addition, by setting bUEP_AUTO_TOG, it is possible to automatically flip the corresponding synchronization trigger bit after successful transmission or successful reception.

The data that each endpoint is ready to send is in its own buffer. The length of the data to be sent is independently set in UEPn_T_LEN.
The data received by each endpoint is in its own buffer, but the length of the received data is in the USB Receive Length Register.
In USB_RX_LEN, it can be distinguished according to the current endpoint number when the USB receives an interrupt.

Table 16.3.1 List of USB Device Endpoint Related Registers (marked by bUC_RESET_SIE reset control)

name	address	description	Reset value
UDEV_CTRL	D1h	USB device physical port control register	10xx 0000b
UEP1_CTRL	D2h	Endpoint 1 Control Register	0000 0000b
UEP1_T_LEN	D3h	Endpoint 1 Transmit Length Register	0xxx xxxxb
UEP2_CTRL	D4h	Endpoint 2 Control Register	0000 0000b
UEP2_T_LEN	D5h	Endpoint 2 Transmit Length Register	0000 0000b
UEP3_CTRL	D6h	Endpoint 3 Control Register	0000 0000b
UEP3_T_LEN	D7h	Endpoint 3 Transmit Length Register	0xxx xxxxb
UEP0_CTRL	DCh	Endpoint 0 Control Register	0000 0000b
UEP0_T_LEN	DDh	Endpoint 0 Transmit Length Register	0xxx xxxxb
UEP4_CTRL	DEh	Endpoint 4 Control Register	0000 0000b
UEP4_T_LEN	DFh	Endpoint 4 Transmit Length Register	0xxx xxxxb
UEP4_1_MOD	EAh	Endpoint 1, 4 mode control register	0000 0000b
UEP2_3_MOD	EBh	Endpoint 2, 3 mode control registers	0000 0000b
UEP0_DMA_H	EDh	Endpoints 0 and 4 buffer start address high byte	0000 00xxb
UEP0_DMA_L	ECh	Endpoint 0 and 4 buffer start address low byte	Xxxx xxxxb
UEP0_DMA	ECh	UEP0_DMA_L and UEP0_DMA_H form a 16-bit SFR	0xxxh
UEP1_DMA_H	EFh	Endpoint 1 buffer start address high byte	0000 00xxb
UEP1_DMA_L	EEh	Endpoint 1 buffer start address low byte	Xxxx xxxxb
UEP1_DMA	EEh	UEP1_DMA_L and UEP1_DMA_H form a 16-bit SFR	0xxxh
UEP2_DMA_H	E5h	Endpoint 2 buffer start address high byte	0000 00xxb
UEP2_DMA_L	E4h	Endpoint 2 buffer start address low byte	Xxxx xxxxb
UEP2_DMA	E4h	UEP2_DMA_L and UEP2_DMA_H form a 16-bit SFR	0xxxh
UEP3_DMA_H	E7h	Endpoint 3 buffer start address high byte	0000 00xxb
UEP3_DMA_L	E6h	Endpoint 3 buffer start address low byte	Xxxx xxxxb
UEP3_DMA	E6h	UEP3_DMA_L and UEP3_DMA_H form a 16-bit SFR	0xxxh

USB device physical port control register (UDEV_CTRL), controlled by bUC_RESET_SIE reset:

Bit	name	access	description	Reset value
7	bUD_PD_DIS	RW	USB device port UDP/UDM pin internal pull-down resistor disable bit, this bit is 1 Disable internal pull-down resistor; this bit is '0' to enable the internal pull-down resistor. This bit is not Controlled by bUSB_IO_EN, it can also be used to provide pull-down resistors in GPIO mode.	1
6	Reserved	RO	reservation	0
5	bUD_DP_PIN	RO	current UDP pin status, 0 for low level; 1 for high level	x
4	bUD_DM_PIN	RO	current UDM pin status, 0 for low level; 1 for high level	x
3	Reserved	RO	reservation	0

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2	bUD_LOW_SPEED	RW	USB device physical port low speed mode enable bit, this bit is 1 select 1.5Mbps Low speed mode; this bit is 0 selects 12Mbps full speed mode	0
1	bUD_GP_BIT	RW	device universal flag: user can define it, can be cleared or set by software	0
0	bUD_PORT_EN	RW	USB device physical port enable bit, this bit is 1 to enable the physical port; this bit is 0 disable physical port	0

Endpoint n Control Register (UEPn_CTRL):

Bit	name	access	description	Reset value
7	bUEP_R_TOG	RW	USB endpoint n receiver (processing SETUP / OUT transaction) expected synchronization trigger Bit, this bit is 0 for DATA0; 1 is for DATA1	0
6	bUEP_T_TOG	RW	The sync trigger bit prepared by the sender of the USB endpoint n (processing the IN transaction), Bit 0 means send DATA0; 1 means send DATA1	0
5	Reserved	RO	reservation	0
4	bUEP_AUTO_TOG	RW	The sync trigger bit automatically flips the enable control bit, which is 1 to indicate that it is being sent Automatically flip the corresponding sync trigger bit after successful work or reception; 0 means no Automatically flip, but can be switched manually. Only supports endpoint 1/2/3	0
3	bUEP_R_RES1	RW	Receiver of Endpoint n has high control response to SETUP/OUT transaction	0
2	bUEP_R_RES0	RW	The receiver of endpoint n controls the low response to the SETUP/OUT transaction	0
1	bUEP_T_RES1	RW	The transmitter of endpoint n has a high control response to the IN transaction.	0
0	bUEP_T_RES0	RW	The transmitter of endpoint n controls the low response to the IN transaction.	0

MASK_UEP_R_RES consisting of bUEP_R_RES1 and bUEP_R_RES0 is used to control the receiver pair SETUP/OUT of endpoint n How the transaction responds: 00 means reply ACK or ready; 01 means timeout/no response, used to implement real-time/synchronous transfer of non-endpoint 0 Loss; 10 means answering NAK or busy; 11 means answering STALL or error.

The MASK_UEP_T_RES consisting of bUEP_T_RES1 and bUEP_T_RES0 is used to control the sender of the endpoint n to the IN transaction. Response mode: 00 means to acknowledge DATA0/DATA1 or data ready and expect ACK; 01 means to acknowledge DATA0/DATA1 and expect no ringing Should be used to implement real-time/synchronous transmission of non-endpoint 0; 10 means answering NAK or busy; 11 means answering STALL or error.

Endpoint n Transmit Length Register (UEPn_T_LEN):

Bit	name	access	description	Reset value
[7:0]	bUEPn_T_LEN	RW	Set the number of data bytes that the USB endpoint n is ready to send (n=0/1/3/4)	00h
	bUEP2_T_LEN		Set the number of bytes of data that USB Endpoint 2 is ready to send	00h

USB Endpoint 1, 4 Mode Control Register (UEP4_1_MOD):

Bit	name	access	description	Reset value
7	bUEP1_RX_EN	RW	This bit is 0 to disable Endpoint 1 reception; to 1 Enable Endpoint 1 Receive (OUT)	0
6	bUEP1_TX_EN	RW	This bit is 0 to disable Endpoint 1 transmission; to 1 Enable Endpoint 1 Transmit (IN)	0
5	Reserved	RO	reservation	0
4	bUEP1_BUF_MOD	RW	Endpoint 1 Data Buffer Mode Control Bit	0
3	bUEP4_RX_EN	R0	This bit is 0 to disable Endpoint 4 reception; to 1 Enable Endpoint 4 Receive (OUT)	0
2	bUEP4_TX_EN	RW	This bit is 0 to disable Endpoint 4 transmission; to 1 Enable Endpoint 4 Transmit (IN)	0
[1:0]	Reserved	RO	reservation	00b

The data buffer modes of USB endpoints 0 and 4 are controlled by the combination of bUEP4_RX_EN and bUEP4_TX_EN, refer to the table below.

Table 16.3.2 Endpoints 0 and 4 Buffer Mode

bUEP4_RX_EN	bUEP4_TX_EN	Structure description: from UEP0_DMA as the starting address from low to high

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0	0	Endpoint 0 Single 64-byte Transceiver Buffer (IN and OUT)
1	0	Endpoint 0 Single 64 Byte Transceiver Buffer; Endpoint 4 Single 64 Byte Receive Buffer (OUT)
0	1	Endpoint 0 Single 64-byte transmit and receive shared buffer; Endpoint 4 Single 64-byte transmit buffer (IN)
1	1	Endpoint 0 single 64-byte transmit and receive shared buffer; endpoint 4 single 64-byte receive buffer (OUT); Endpoint 4 Single 64-byte transmit buffer (IN). All 192 bytes are arranged as follows: UEP0_DMA+0 address: Endpoint 0 transceiver sharing; UEP0_DMA+64 address: Endpoint 4 receives; UEP0_DMA+128 Address: Endpoint 4 Send

USB Endpoint 2, 3 Mode Control Register (UEP2_3_MOD):

Bit	name	access	description	Reset value
7	bUEP3_RX_EN	RW	This bit is 0 to disable Endpoint 3 reception; to 1 Enable Endpoint 3 Receive (OUT)	0
6	bUEP3_TX_EN	RW	This bit is 0 to disable Endpoint 3 transmission; 1 is enabled Endpoint 3 Transmit (IN)	0
5	Reserved	RO	reservation	0
4	bUEP3_BUF_MOD	RW	Endpoint 3 Data Buffer Mode Control Bit	0
3	bUEP2_RX_EN	R0	This bit is 0 to disable Endpoint 2 reception; to 1 Enable Endpoint 2 Receive (OUT)	0
2	bUEP2_TX_EN	RW	This bit is 0 to disable Endpoint 2 transmission; 1 is to enable Endpoint 2 Transmit (IN)	0
1	Reserved	RO	reservation	0
0	bUEP2_BUF_MOD	RW	Endpoint 2 Data Buffer Mode Control Bit	0

Control USB endpoints 1, 2, 3 by bUEPn_RX_EN and bUEPn_TX_EN and bUEPn_BUF_MOD (n=1/2/3) respectively

For the data buffer mode, refer to the table below. Among the double 64-byte buffer mode, USB data transmission will be based on bUEP_*_TOG=0

Select the first 64-byte buffer and select the next 64-byte buffer according to bUEP_*_TOG=1 for automatic switching.

Table 16.3.3 Endpoint n Buffer Mode (n=1/2/3)

bUEPn_RX_EN	bUEPn_TX_EN	bUEPn_BUF_MOD	Structure description: starting from UEPn_DMA starting from low to high
0	0	x	Endpoint is disabled, UEPn_DMA buffer is not used
1	0	0	Single 64-byte receive buffer (OUT)
1	0	1	Dual 64-byte receive buffer, selected by bUEP_R_TOG
0	1	0	Single 64-byte transmit buffer (IN)
0	1	1	Dual 64-byte transmit buffer, selected by bUEP_T_TOG
1	1	0	Single 64-byte receive buffer; single 64-byte transmit buffer
1	1	1	Dual 64-byte receive buffer, selected by bUEP_R_TOG; dual 64 Byte send buffer, selected by bUEP_T_TOG. All 256 bytes are arranged as follows: UEPn_DMA+0 address: endpoint reception when bUEP_R_TOG=0; UEPn_DMA+64 address: endpoint reception when bUEP_R_TOG=1; UEPn_DMA+128 address: endpoint sent when bUEP_T_TOG=0; UEPn_DMA+192 address: endpoint sent when bUEP_T_TOG=1

USB Endpoint n Buffer Start Address (UEPn_DMA) (n=0/1/2/3):

Bit	name	access	description	Reset value
[7:0]	UEPn_DMA_H	RW	Endpoint n buffer start address high byte, only the lower 2 bits are valid, the upper 6 bits Fixed to 0	0xh
[7:0]	UEPn_DMA_L	RW	endpoint n buffer start address low byte	Xxh

Note: The length of the buffer receiving data >= min (maximum packet length possible to receive + 2 bytes, 64 bytes)

17, touch button Touch-Key

17.1 Introduction to Touch-Key

The CH552 chip provides a capacitance detection module and associated timers with 6 input channels and supports a capacitance range of 5pF~ 150pF. The self-capacitance mode can support up to 6 touch buttons, and the mutual capacitance mode can support up to 15 touch buttons.

17.2 Touch-Key Register

Table 17.2.1 Touch-Key Related Register List

name	address	description	Reset value
TKEY_CTRL	C3h	Touch-Key Control Register	X0h
TKEY_DATH	C5h	Touch-Key data high byte (read only)	00h
TKEY_DATL	C4h	Touch-Key data low byte (read only)	Xxh
TKEY_DAT	C4h	TKEY_DATL and TKEY_DATH form a 16-bit SFR	00xxh

Touch-Key Control Register (TKEY_CTRL):

Bit	name	access	description	Reset value

7	bTKC_IF	RO	Timed interrupt flag. If bTKD_CHG=0 then at the current timing week Automatically set a request interrupt at the end of the period, when the preparation phase ends Cleared to zero or cleared by writing TKEY_CTRL. in case bTKD_CHG=1 is automatically cleared, no interrupt is requested, skip the current week Period, then re-prepare and test in the next cycle, and next Automatically set request interrupt at the end of each cycle	x
[6:5]	Reserved	RO	reservation	00b
4	bTKC_2MS	RW	The period of the capacitor detection timer is selected: 0-1mS; 1-2mS. The first 87uS of each cycle is the preparation phase and the remaining time the detection phase. The above time is based on the time when Fosc=24MHz	0
3	Reserved	RO	reservation	0
2	bTKC_CHAN2	RW	touch button capacitance detection input selects high position	0
1	bTKC_CHAN1	RW	touch button capacitance detection input selects median	0
0	bTKC_CHAN0	RW	touch button capacitance detection input selects low position	0

The touch key capacitance detection input channel is selected by bTKC_CHAN2~bTKC_CHAN0.

bTKC_CHAN2	bTKC_CHAN1	bTKC_CHAN0	Select touch button capacitance detection input channel
0	0	0	Turn off the power of the capacitance detection module. Only used as an independent timer interrupt with a period of 1mS or 2mS
0	0	1	TIN0 (P1.0)
0	1	0	TIN1 (P1.1)
0	1	1	TIN2 (P1.4)
1	0	0	TIN3 (P1.5)
1	0	1	TIN4 (P1.6)
1	1	0	TIN5 (P1.7)
1	1	1	Turn on the power of the capacitance detection module but do not connect any channels.

Touch-Key Data Register (TKEY_DAT):

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Bit	name	access	description	Reset value
7	bTKD_CHG TKEY_DATH[7]	RO	The Touch-Key controls the change flag. This bit is 1 indicating that TKEY_CTRL is The capacitor detection phase is rewritten, which may cause the TKEY_DAT data to be invalid. And bTKC_IF will not be set at the end of the current cycle. This bit is fixed at each The time period is automatically cleared at the end of the preparation phase, and the data needs to be masked.	0
6	Reserved	RO	reservation	0
[5:0]	TKEY_DATH	RO	Touch-Key data high byte. At the preparation stage of each timing cycle Automatically clear when beam is bundled; automatically counts during capacitance detection phase; in preparation phase Keep the data unchanged so that the timer interrupts the program to read	00h
[7:0]	TKEY_DATL	RO	Touch-Key data low byte. At the preparation stage of each timing cycle Automatically clear when beam is bundled; automatically counts during capacitance detection phase; in preparation phase Keep the data unchanged so that the timer interrupts the program to read	Xxh

17.3 Touch-Key Function

Capacitance detection steps:

(1) Set bTKC_2MS and bTKC_CHAN2 to bTKC_CHAN0 in the TKEY_CTRL register to select the period and input channel. Be
The selected input channel, its GPIO pin must be set to high-impedance input mode, or open-drain output mode and is in the input
A state of 1 (corresponding to a high-impedance input), Pn_DIR_PU[x]=0.

(2) Clear bTKC_IF and enable interrupt IE_TKEY to wait for the timer interrupt, or enter the interrupt program by actively polling bTKC_IF.

(3) After the current channel capacitance detection is completed, the bTKC_IF request interrupt will be automatically set and the preparation phase of the next cycle will be entered.
And keep the TKEY_DAT data unchanged about 87uS.

(4), enter the interrupt program, first read the current channel capacitance data from TKEY_DAT, and shield the highest bit bTKD_CHG,
The data is a relative value, which is inversely proportional to the capacitance, and the data when the touch button is pressed is smaller than the data when the touch button is not pressed.

(5) Set bTKC_2MS and bTKC_CHAN2 to bTKC_CHAN0 in the TKEY_CTRL register to select the next input channel. The
The write operation will automatically clear bTKC_IF and end the interrupt request.

(6), the TKEY_DAT data read by the step (4) is compared with the data when the previously saved channel has no button, and it is judged whether the capacitance changes.

And if there is a button pressed.
(7), interrupt return, when the capacitance of the next channel is detected, it will turn to step (3).

18, parameters

18.1 Absolute Maximum (Critical or exceeding the absolute maximum may cause the chip to work abnormally or even be damaged)

name	Parameter Description	Minimum value	Maximum	unit
TA	The system's main frequency Fsys is less than 28MHz.	-40	85	°C
TA32M	The system's main frequency Fsys is greater than 28MHz.	-20	70	°C
TS	Ambient temperature during storage	-55	125	°C
VCC	Power supply voltage (VCC is connected to the power supply, GND is grounded)	-0.4	5.8	V
VIO	Voltage on other input or output pins except P3.6/P3.7	-0.4	VCC+0.4	V
VIOU	P3.6/P3.7 Voltage on the input or output pin	-0.4	V33+0.4	V

18.2 Electrical parameters 5V (test conditions: TA=25°C, VCC=5V, Fsys=6MHz)

name	Parameter Description	Minimum value	Typical value	Maximum	unit
VCC5	VCC pin supply voltage V33 external capacitor only	3.7	5	5.5	V
V33	Internal USB power regulator output voltage	3.14	3.27	3.4	V

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ICC24M5	Fsys=24MHz total supply current during operation	8	11		mA
ICC6M5	Fsys=6MHz total supply current during operation	4	6		mA
ICC750K5	Fsys=750KHz total supply current during operation	2	3		mA
ISLP5	Total supply current after sleep		0.1	0.2	mA
ISLP5L	VCC=V33=5V, and the external crystal clock is selected. And bLDO3V3_OFF=1 turns off the LDO, Total supply current after complete sleep		0.008	0.02	mA
IADC5	ADC analog to digital converter module operating current		200	800	uA
ICMP5	Voltage comparator module operating current		100	500	uA
ITKEY5	Touch button capacitance detection module operating current		150	250	uA
VIL5	Low level input voltage	-0.4		1.2	V
VIH5	High level input voltage	2.4		VCC+0.4	V
VOL5	Low level output voltage (12mA sink current)			0.4	V
VOH5	High level output voltage (8mA output current)	VCC-0.4			V
VOH5U	P3.6/P3.7 High level output voltage (8mA output current)	V33-0.4			V
IIN	Input current without pull-up input	-5	0	5	uA
IDN5	Input current with pull-down resistor input	-35	-70	-140	uA
IUP5	Input current with pull-up resistor input	35	70	140	uA
IUP5X	Input current with pull-up input from low to high flip	250	400	600	uA
Vpot	Threshold voltage of power-on reset	2.1	2.3	2.5	V

18.3 Electrical parameters 3.3V (test conditions: TA=25°C, VCC=V33=3.3V, Fsys=6MHz)

name		Parameter Description	Minimum value	Typical value	Maximum	unit
VCC3	VCC pin voltage	V33 is shorted to VCC and USB is turned on	3.0	3.3	3.6	V
		V33 is shorted to VCC, turn off USB	2.5	3.3	3.6	V
ICC16M3		Fsys=16MHz total supply current during operation	4	6		mA
ICC6M3		Fsys=6MHz total supply current during operation	2	4		mA
ICC750K3		Fsys=750KHz total supply current during operation	1	2		mA
ISLP3		Total supply current after sleep		0.07	0.15	mA
ISLP3L		bLDO3V3_OFF=1 turns off the LDO, Total supply current after complete sleep		0.004	0.01	mA
IADC3		ADC analog to digital converter module operating current		150	500	uA
ICMP3		Voltage comparator module operating current		70	300	uA
ITKEY3		Touch button capacitance detection module operating current		130	200	uA

VIL3	Low level input voltage	-0.4		0.8	V
VIH3	High level input voltage	1.9		VCC+0.4	V
VOL3	Low level output voltage (8mA sink current)			0.4	V
VOH3	High level output voltage (5mA output current)	VCC-0.4			V
VOH3U	P3.6/P3.7 High level output voltage (8mA output current)	V33-0.4			V
IIN	Input current without pull-up input	-5	0	5	uA
IDN3	Input current with pull-down resistor input	-15	-30	-60	uA
IUP3	Input current with pull-up resistor input	15	30	60	uA
IUP3X	Input current with pull-up input from low to high flip	100	170	250	uA
Vpot	Threshold voltage of power-on reset	2.1	2.3	2.5	V

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18.4 Timing parameters (test conditions: TA=25°C, VCC=5V or VCC=V33=3.3V, Fsys=6MHz)

name	Parameter Description	Minimum value	Typical value	Maximum	unit
Fxt	External crystal frequency or XI input clock frequency	6	twenty four	25	MHz
Fosc	Calibrated internal clock frequency at V33=3V to 3.6V	23.64	twenty four	24.36	MHz
	Calibrated internal clock frequency when Fosc27 V33=2.7V~3V	23.28	twenty four	24.72	MHz
Fosc25	Calibrated internal clock frequency at V33=2.5V	twenty one	twenty four	27	MHz
Fpll	Internally multiplied PLL frequency	twenty four	96	100	MHz
Fusb4x	USB sampling clock frequency when using USB device function	47.04	48	48.96	MHz
Fsys	System clock frequency (VCC>=4.9V)	0.1	6	32	MHz
	System clock frequency (4.9V>VCC>=4.0V)	0.1	6	twenty four	MHz
	System clock frequency (4.0V>VCC>=2.8V)	0.1	6	16	MHz
	System clock frequency (VCC<2.8V)	0.1	6	12	MHz
Tpor	Power-on reset delay	9	11	15	mS
Trst	Enter the width of the valid reset signal from the RST external	70			nS
Trdl	Warm reset delay	30	45	60	uS
Twdc	Calculation formula for watchdog overflow period/timing period	65536 * (0x100 - WDOG_COUNT) / Fsys			
Tusp	Detect USB auto suspend time	4	5	6	mS
Twak	Wake-up completion time after chip sleep	1	2	10	uS

19, modify the record

version	date	Description
V1.0	2016.12.20	Original Issue