Lowlights to roll up

JasperGold **FPV** @ **Hisilicon** (Tim):  The analyze issue” the report error causing about -f option in the filelist” was appeared again in another case. Users complained that spend them a lot of time to find the cause of this kind of problem, they hope we can fix it as soon as possible. JG-76678, escalate to S0

JasperGold **CDC** @ **TI** **Bangalore** (Bijit): TI CMCU has expressed concern about bandwidth shortage for R&D/AE/PE. They want resource augmentation in R&D to deliver features faster and handle deployment issues at the same time. Also want AEs to take over day to day support issues so that my bandwidth is available to concentrate on SoC bring up activity. Internally discussing with R&D, AE team and management on mitigation plan.

JasperGold **SEC** @ **Intel** (Vaibhav): False positive uncovered by customer.  Previous version showed equivalence while latest version shows correct non-equivalence. Account team very concerned about the false positive but more about the lack of communication around a known tool bug. Asa and Karam to follow up...

Highlights to roll up

JasperGold **FPV** @ **Samsung** (Yumi): Foundry group confirmed that they will use FSO in their next project. Trying to understand from account team next steps on FSO with System LSI

JasperGold **FPV** @ **CSCC** **Changsha:** (Tim) user is design ARM-based CPU core. In the new project DMS, they decide to use JasperGold (both FPV and SEC) for unit verification for most of the design. I have delivered training and having design review with the team to come out a long list of units. User is also interested in CSR and CONN applications, also DBH. The good thing is that it will become JapserGold dedicated user if we can help user to be successful in this project. The bad thing is that it will consume a lot of our resource. **Synopsys** is promoting Hector there.

JasperGold **FPV** @ **WD** **TW:** (Tim) the evaluation went very well. “OneSpin left some liveness properties cannot converged, while  Jasper can converge or catch CEX for all the properties within one day. JG found a lot of false negative CEX due to incorrect assumption while OneSpin cannot find them”. For CONN Application, “JG provide more complete configuration options than OneSpin for users to define connections”. For COV application, “JG found much more deadcode items than OneSpin.”

Lowlights

JasperGold **CDC** @ **Saankhya** **Labs** **Bangalore** (Bijit): Had a review meeting with the customer on their IP level CDC setup. They have cleaned up 4 IPs and want to use them at top level. Suggested running hierarchical CDC with 2018.03 build. They faced long runtime issue with 2018.03. The clock domain find step was completing in one hour time with 2017.12 but hangs with 2018.03. SCR JG-79483 filed. Advised user to continue with 2017.12 and reuse block level port ratings to identify CDC at full chip level. Fortunately, they only have static registers crossing clock domains at the top level.

JasperGold **SEC** @ **New** **York** (Yaron): Prove performance for "FPV" properties in SEC setup culprit are the INIT mappings. Seems that we dont have out of the box solution for this issue and will probably need silver level support. Could not get all stake holders to discuss the simplification process performance boost that Antonio reported in SEC. delayed to next week

JasperGold **SEC** @ **Nvidia** (Yaron): Nvidia accpetence tests with 2018.03p002 revealed many issues. some of them were already solved by R&D, some are still pending. PGM bug prevents running bug hunting strategy on 2018.06. R&D are working to reproduce internally

JasperGold **SuperLint** @ **Arm** **Austin** (Kanwar): Worked with R&D to help resolve a release blocker Superlint restore crash reported by the DFT team. It took multiple iterations to nail down the issue and fix it. Finally it seems to be fixed and shoudl make it to the 2018.06 FCS release

JasperGold **SuperLint** @ **TI** **Bangalore** (Kanwar): With Superlint usage picking up in various CMCU teams, some concerns were raised by SimpleLink team lead on iterations required between Cadence and TI to fix/close issues. We took an action to streamline the process to reduce the iterations

JasperGold **UNR** @ **NY** **Cupertino** (Jose): Ongoing activities to debug Ba\* issue and Ce\* issues.  Ce\* design effort is internal and has no customer visibility at this time.  Ba\* debug activity is an outstanding activity from a few months back but is not gating any NY activities.

Highlights

JasperGold @ **Samsung** **Bangalore** (Kanwar): Visited Samsung with Asa, Amit and Pradeep from the field team. Samsung is growing big time and the expanded System LSI team looking to use wherever possible to improve the quality and productivity of SOC verification. Listed various Jasper apps/technologies they like to engage with - CONN, SEC, SPV being the primary apps of interest. Hope to see much bigger adoption of Jasper technology by Samsung Bangalore team. During the meeting, Rahul from Samsung MSG team came and endorsed Jasper and benefits

he and his team have seen.

JasperGold @ INTERNAL Bangalore (Kanwar): Attended Club in Bangalore. This year's theme was signoff. Very well attended event. Nearly 70 attendees from different customers in Bangalore. NXP keynote talked about UNR, CONN and Superlint (for FSM checks) usage. Good user presentations from nVidia and TI. Asa presented the Jasper roadmap and Vaibhav talked about Signoff. I had discussions with Intel, TI (DV team) and nVidia on the sides of the event. Event ended with a panel discussion on 'Is Signoff a reality or still a dream'

JasperGold **ABVIP** @ **HXT** **China** (Dave): PE-R&D sync to plan delivery schedule, ABVIP testing.  Vaibhav now helping with interface ABVIP.  SYS will create wrapper aligned to INTF ABVIP - s   ignals, parameters, etc.

JasperGold **CDC** @ **TI** **Bangalore** (Bijit): Met with the Analog group in Bangalore. The high runtime was due to FIFO detection. After defining the FIFO sync as custom scheme, the issue got    resolved. However, they have a special FIFO which has more than one read data bus. We need to enhance our custom scheme template to support it. Combined clock domain for gated clocks issue got resolved with additional set\_case\_analysis constraints. Other queries regarding .lib support, bbox handling and static signals answered.

JasperGold **CDC** @ INTERNAL (Bijit): Worked with Nizar and Fabiano to come up with the CPF plan for Ziyad to present during DAC to TI. It considers only those items marked as H and M in the XLS. The plan also includes the estimates for supporting existing CDC flow on PA design in Always-ON mode.

JasperGold **CONN** @ **Arm** **Cambridge** (Stefan): With moving the MBIST initialize sequence to reset simulation, we were able to converge all but 13 assertions out of 7000. Prashant who's driving the project from Arm side is happy, and wants Stefan to have a look at another example with convergence problems.

JasperGold **COV** @ INTERNAL US (Dave): JG-COV - new coverage app is being turned on for trunk builds by default this week.  Many refinements completed on the GUI.  Will be pushing this out to AEs for feedback, along with some selected users at EA customers Intel and ARM

JasperGold **FPV** @ **Cray** (Dave): Cray Bristol is interested in a JG-FPV evaluation.  There has been previous interest in JG at Bristol and US sites, and was considered during last renewal   , but then dropped at last minute.  Bristol will do an eval, pending AE resource approval.  There has not been much contact with the US (Wisconsin) team we had talked with previously,    due to people on both sides leaving, but account team is trying to re-establish contact.

JasperGold **FPV** @ **IFX** (Stefan): Eval still going very well, next two weeks will be used to work on 2 designs. We were able to cut down the proof time in the ECC to 2h using 10 licenses,    and OneSpin needs around 6h. Phani who is driving the evaluation from IFX side is very happy so far. experts at IFX are kept in the loop and also want to get hands on the tool.

JasperGold **FPV** @ **Samsung** **India** (Yumi): FSO Discovery for Samsung India: Samsung SLSI in Korea requested the discovery slides to forward to SLSI in India. Sent to them yesterday. After    that they (India group) might contact us for webinar or engagement. Asa also visited this group while in India.  While FSO is of interest others apps/flows likely more important in the short term (CONN, SEC)

JasperGold **SEC** @ **Nvidia** (Yaron): Managed to get better performance than competition on a memory loaded SEC model with engine J. It will be added to Autoprove relevant threads. Managed to get reduced memory footprint results with a WA supplied by R&D. This does not solve the memory leak, but make it possible to run the testcases without memory blowing up in a critical manner

JasperGold **SuperLint** @ **TI** **Bangalore** (Kanwar): Visited TI CMCU team in Bangalore to discuss Superlint adoption. Got confirmation about Superlint1.0 being POR for Lint and DFT in all CMCU teams worldwide.

Lights

JasperGold @ **Arm** **Cambridge** (Stefan): Arm sent their list of SCRs they want to be fixed for 2018.09FCS. Long list, need to agree on a subset with Arm

JasperGold @ INTERNAL (Yaron): Found out that 2018.06 versions cannot run engine jobs on RH5 servers. This issue popped up in DPC runs. Alerted Paula that we need to better communicate this issue to customers as the reporting AE could not easily understand why many of his runs failed.

JasperGold **CDC** @ INTERNAL Bangalore (Bijit): Met with the engineer from IPG DDR group. Debugged all the no\_scheme violations and realized that the issue is related to cdc\_level\_sync not being identified as NDFF automatically. Defining it as a user-defined/custom also did not help. Planned to create smaller test cases to reproduce the issue.

JasperGold **COV** @ INTERNAL (Yumi): "default" support on covergroups: While preparing covergroup tech update I got surprised with the behavior of "default" keyword in covergroups. R&D clarified it's not defined in LRM and thus implementation is tool-specific. Confirmed that it was implemented as requested by customers (ARM and Mediatek)

JasperGold **SEC** @ **Broadcom** **San** **Jose** (Fernanda): Kicked off SEC run with Clock Gating logic toggle covers for bound analysis. This is a proof of concept of the signoff method we wish to    propose to Broadcom. Gautham is working on generating RTL for new blocks and will make them available this week.

JasperGold **SPV** @ **IFX** (Stefan): IFX also wants to look at SPV, as a next automotive design will have a larger security part. They also want to compare with what OneSpin has to offer

JasperGold **UNR** @ **NY** **Austin** (Jose): LDC ready to start running UNR flow on latest graphics chip G13P.  Communicated update on latest fixes in UNR flow and their availability in Xcelium GREEN 18.06v001 and Jasper 2018.06FCS. They are ready to pipeclean when we deliver these versions of tools.

JasperGold **vManager** @ **NXP** **Austin** (Jose): Met with Jing (NXP) to discuss Multi-Engine MDV presentation of data in vManager.  It was just a discovery presentation.

JasperGold **vManager** @ **NY** **Austin** (Jose): Kicked off activity to bring in and simulation data into vmanager.  We were able to read in data.  NY’s immediate interest is for us to report properties run in are not being run in simulation.  Investigating how to get this report with simple local testcase.  Once we have simulation results, we will generate this report on real NY metrics