ECE 422 Final Project

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Due 9pm December 10th

Introduction:

We began the project looking at the lecture notes on the miller effect, pole-splitting, and unity gain frequency analysis. Noticing that the miller effect circuit analyzed in the notes was similar to a recent homework problem, we used our homework analysis as a base for the project. Using our base analysis, we remodeled our parameters and created a net-list, which yielded an open loop gain of around 35db for the first stage. For the second stage of the amplifier we incorporated the miller effect compensation capacitor and zero-nullifying resistor. Referencing the calculations in the lecture notes, we were able to calculate a resistance value needed to push the zero towards negative infinity making it LHS. For the second stage of the amplifier we used an inverting topology with a total gain Gm(Ro8 || Ro7). This will give us the maximum output gain for the second stage since the two Ro's are in parallel. This output resistance to the load capacitance will be approximately 8k, assuming the Ro's are approximately 16k from calculations.

Calculations and Results:

Now that we have a basic 2 stage topology, the results from the two stage amplifier with pole splitting compensation is shown in Appendix A. Using our base analysis, we calculated all the transistor width and length values based on the required bias voltages to keep all the transistors in saturation while also maximizing the gm in both amplifier stages and maximizing the output resistances. For the second stage, we modeled the two transistors to get an output gain greater than 65dB. Refer to Appendix B for the simulation graphs and Appendix C for the second stage of the amplifier's capacitance and resistance.

To verify our analysis we used Hspice to sweep and find the input common mode range. We modified our .ac analysis to include a common mode voltage sweep between -1 and 1volts. The result of our simulation gave us a minimum common mode voltage of -0.17v and a maximum common mode voltage of 0.61v.

After simulating the common mode range voltages we calculated by hand the minimum and maximum output voltages using the simulated parameters. To calculate the maximum output voltage we subtracted the over voltage of mosfet m8 from Vdd. The result was a maximum output voltage of 0.765v. To calculate the minimum output voltage we added the over-voltage of mosfet m7 to Vss, resulting in a minimum output voltage of -0.749v.

Appendix A: Table comparing Required with Simulated.

Specification Names	**Required Specifications**	**Simulated Results**
Load capacitance	5pF	5pF
Power supply	Vdd = 0.9V, Vss = -0.9V	Vdd = 0.9V, Vss = -0.9V
Open loop gain	≥ 65dB	= 67.926dB
Phase margin	≥ 60◦	= 90.729◦
Unity gain frequency	≥ 12M Hz	= 66.29M Hz

Appendix B: Graphs of Simulation Results.

Figure B.1

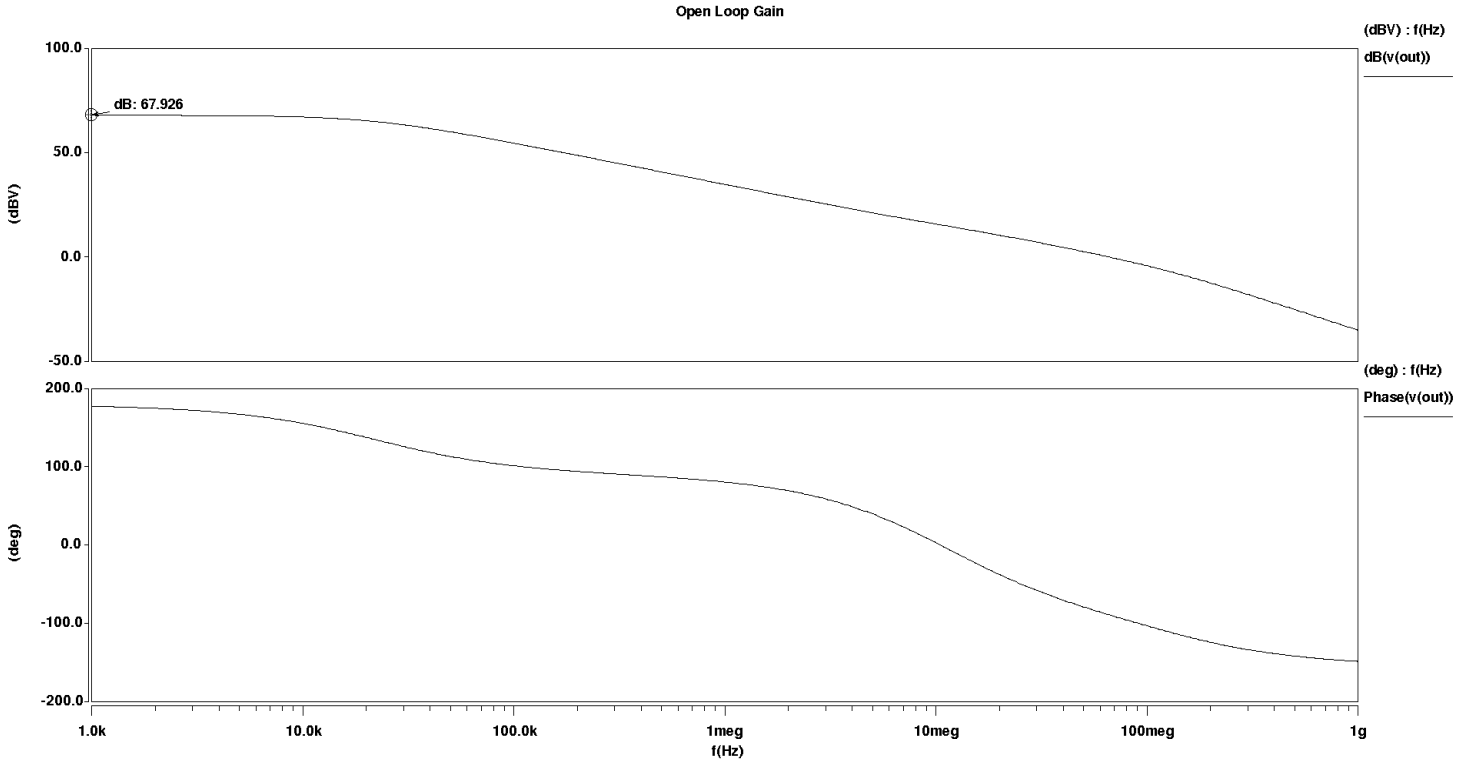


Figure B.2

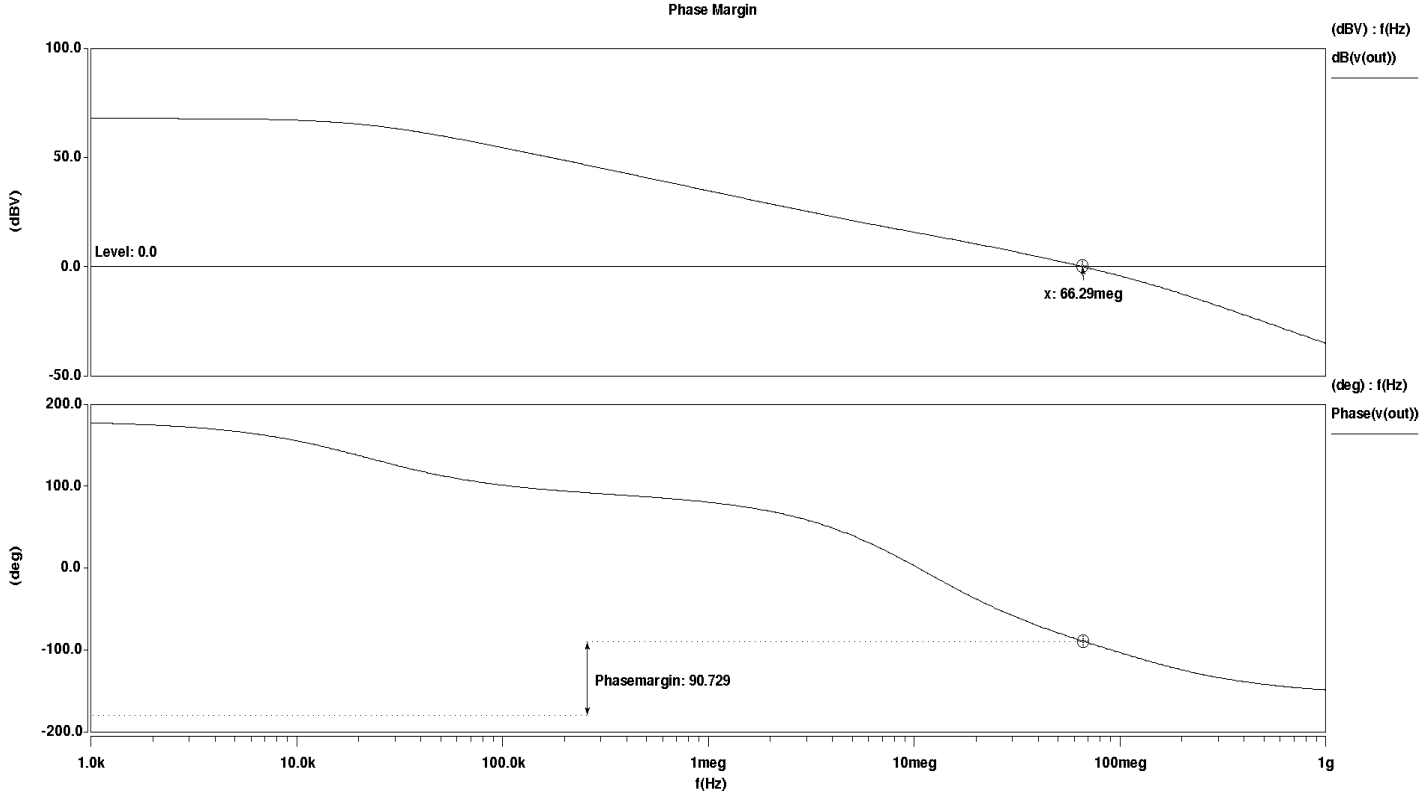
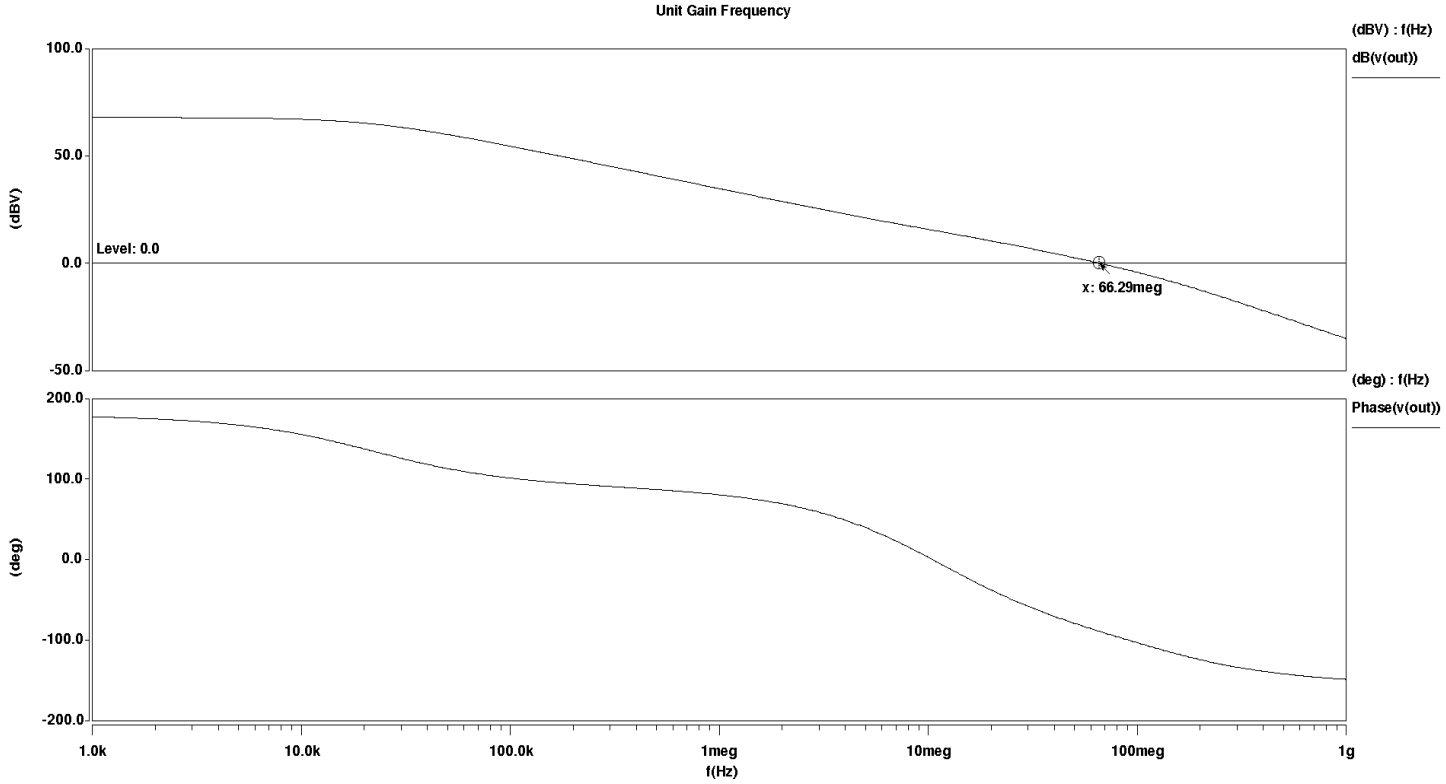


Figure B.3


Unit Gain Frequency
(dBV) : f(Hz)
dB(v(out))
100.0
50.0
0.0
-50.0
(dBV)
Level: 0.0
x: 66.29meg
(deg) : f(Hz)
Phase(v(out))
200.0
100.0
0.0
-100.0
-200.0
(deg)
1.0k
10.0k
100.0k
1meg
10meg
100meg
1g
f(Hz)

Appendix C: Hand Analysis

Figure C.1: General Schematic

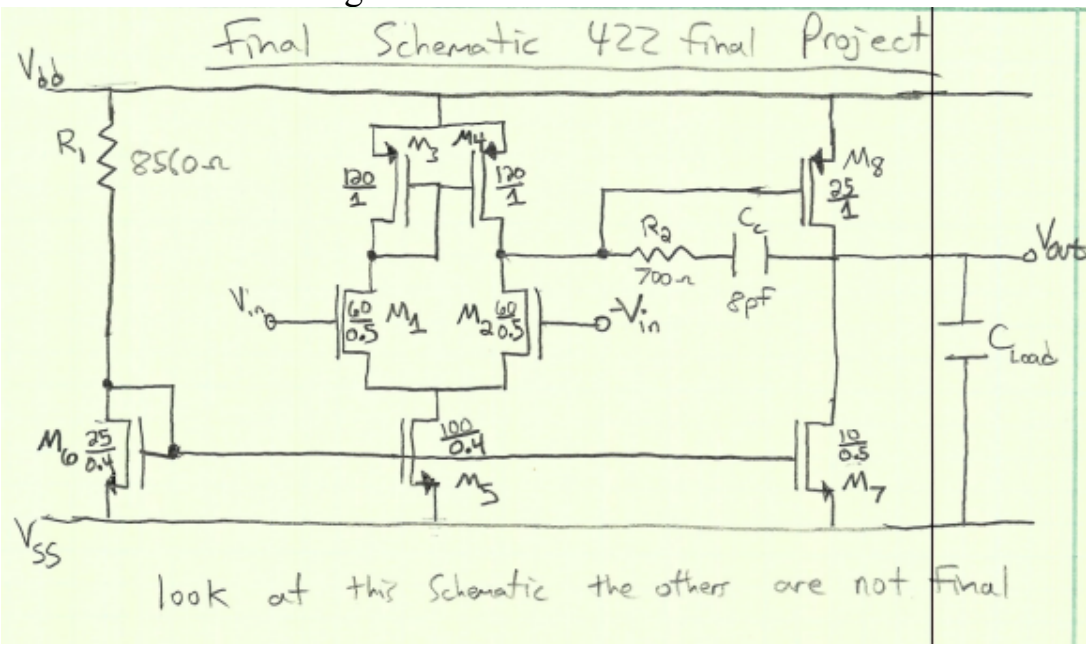


Figure C.2: Output Voltage Range

$$V_{dd} - V_{ov_{M8}} = V_{o_{max}}$$

$$V_{ov_{M8}} = \sqrt{\frac{2I_D}{k_p'\left(\frac{W}{L}\right)}} = \sqrt{\frac{2(53.35\times10^{-6})}{(235\times10^{-6})\left(\frac{25}{1}\right)}} = 0.135\ V$$

$$V_{o_{max}} = 0.9V - 0.135V = 0.765\ V$$

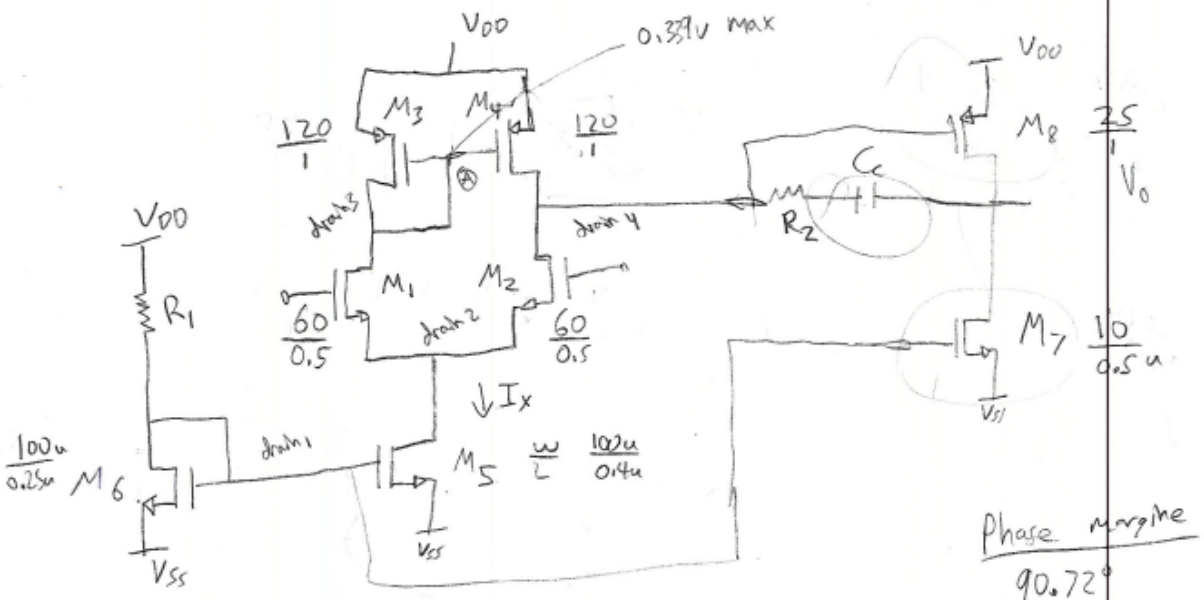
$$V_o - V_{ov_{M7}} = -0.9V$$

$$V_{o_{min}} = V_{ov_{M7}} - 0.9V$$

$$V_{ov_{M7}} = \sqrt{\frac{2I_D}{k_n'\left(\frac{W}{L}\right)}} = \sqrt{\frac{2(53.35\times10^{-6})}{(235\times10^{-6})\left(\frac{10}{0.5}\right)}} = 0.151\ V$$

$$V_{ov_{min}} = -0.749\ V$$

Figure C.3: More output stage calculations.



Phase margine
90.72°

$I_X = 600\mu A$

$r_1 = \frac{1.16614V}{600\mu A} = 8560\Omega$

R_1

$\frac{1}{g_{m4}}$

$\frac{M_6}{M_8}$

Makes lengths larger.

To calculate R_2 I am using the same topology as in the notes. Using the $\frac{1}{g_{m4}}$ to Cancel out one of the Poles.

$g_{m4} = \sqrt{2 k_n' (\frac{W}{L}) I_D}$

$I_D = 300\mu A$

$k_n' = 235 \times 10^{-6} \frac{A}{V^2}$

$(\frac{W}{L}) = 120$ Since $W = 60u$, $L = 0.5u$

$r_{o8} \| r_{o7}$

$r_{o8} \approx r_{o7} \approx \frac{1}{(0.1)(600\mu A)}$

$g_{m4} = \sqrt{2(235\times10^{-6})(120)(300\times10^{-6})}$

$g_{m4} \approx 4.11ms$ $\frac{1}{g_{m4}} \approx 243\Omega$

R_2 needs $> 243\Omega$

Now using $\omega_z = \frac{1}{C_c\{\frac{1}{g_{m2}} - R_z\}}$

chose 8pf for C_c

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Figure C.4: Pole Splinting with R2