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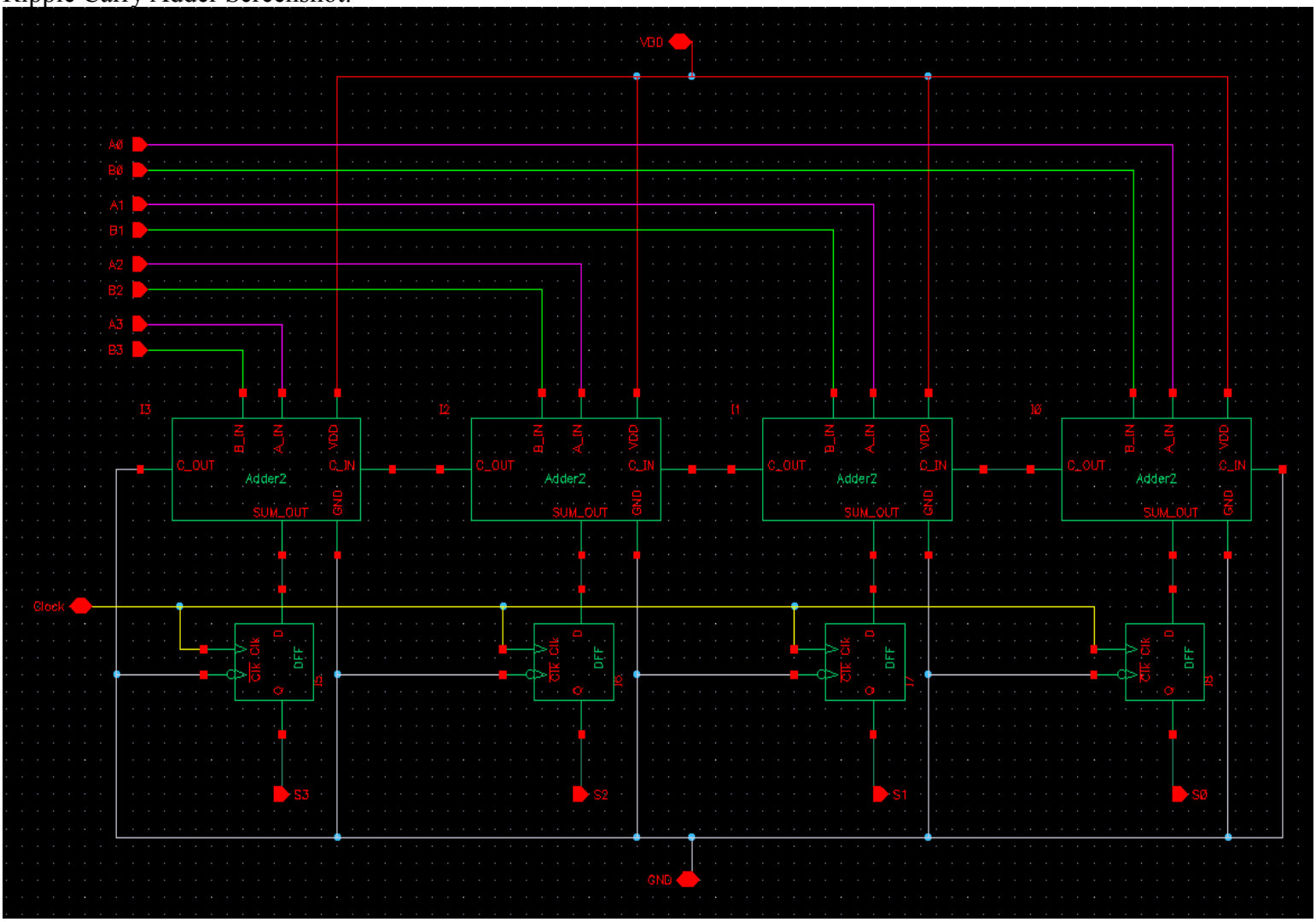
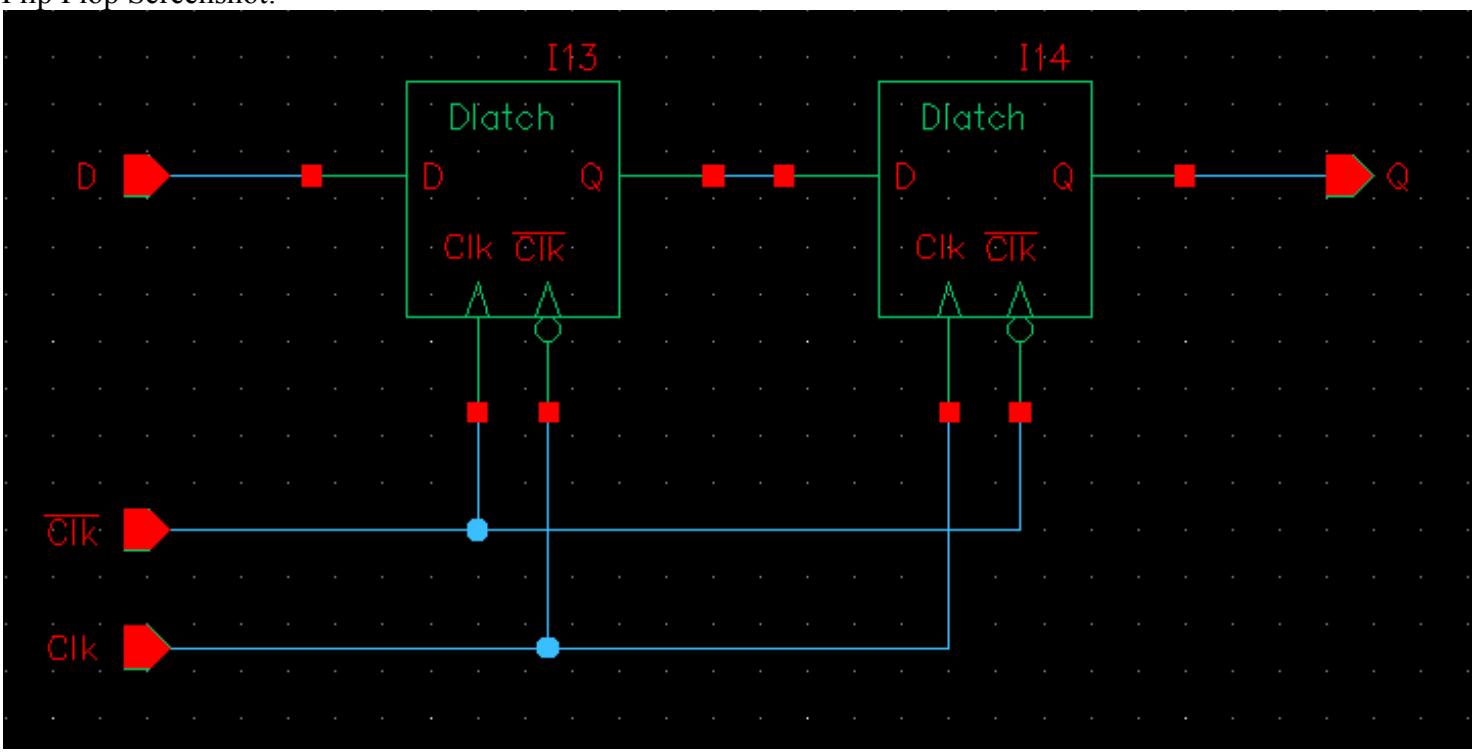
# Lab 6

Calculations:
Assuming worst case delay on all full adders, best clk frequency
Worst case delay assuming last carryout = don't care: 16.83e-10s
Frequency for DFF holding accurate values = 1/16.83e-10s = 5.94MHz

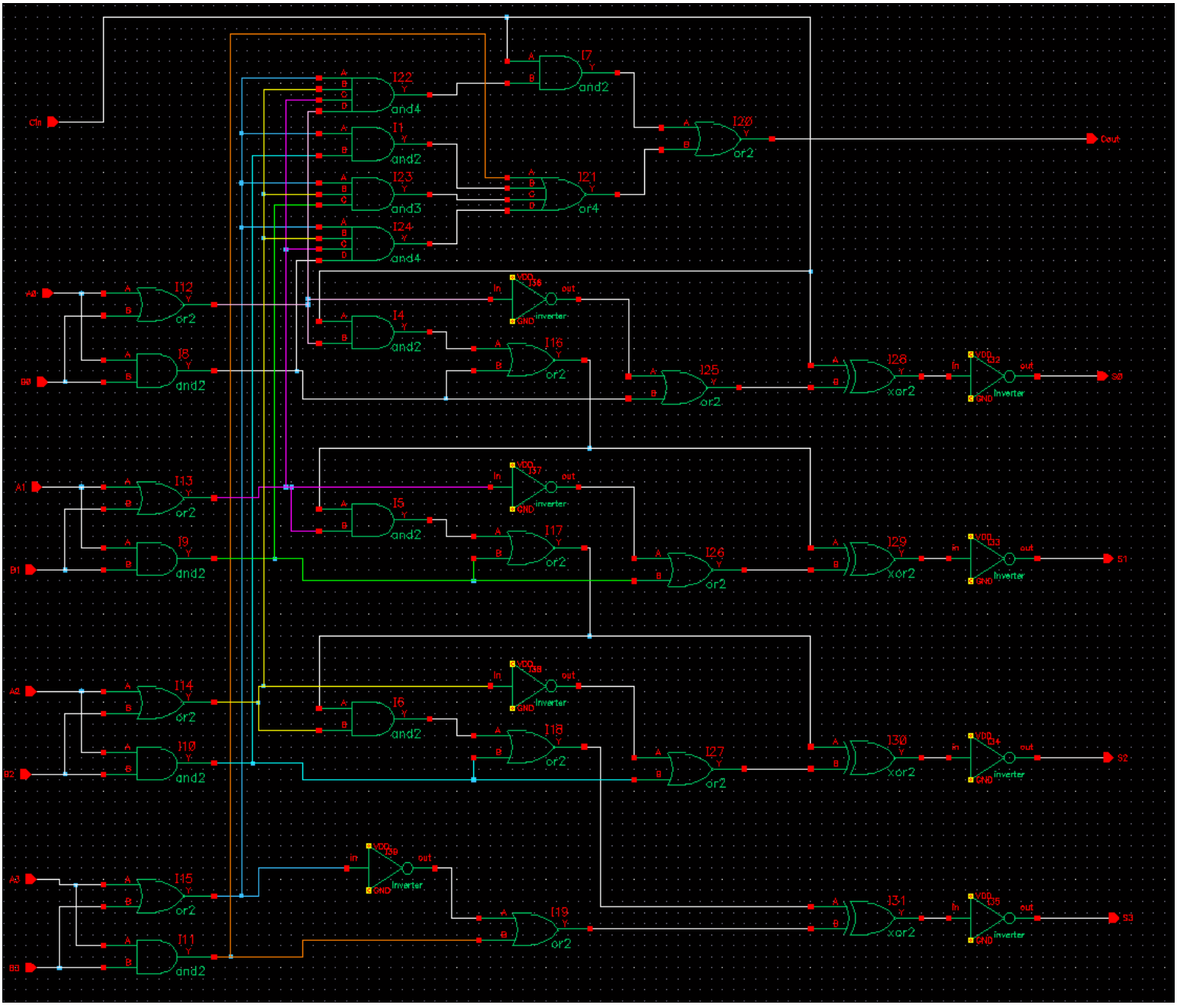
Ripple Carry Adder Screenshot:



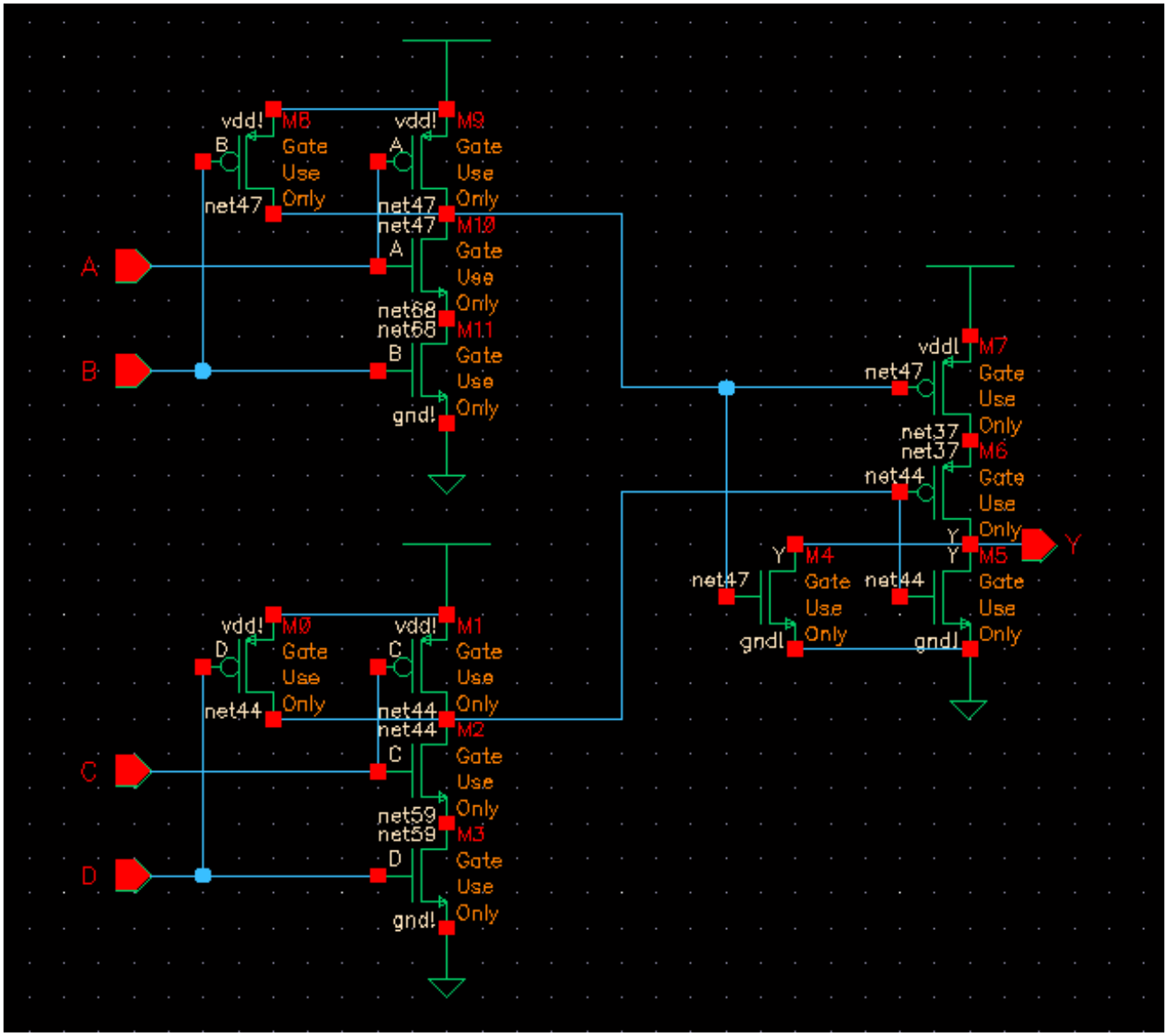
D Flip Flop Screenshot:



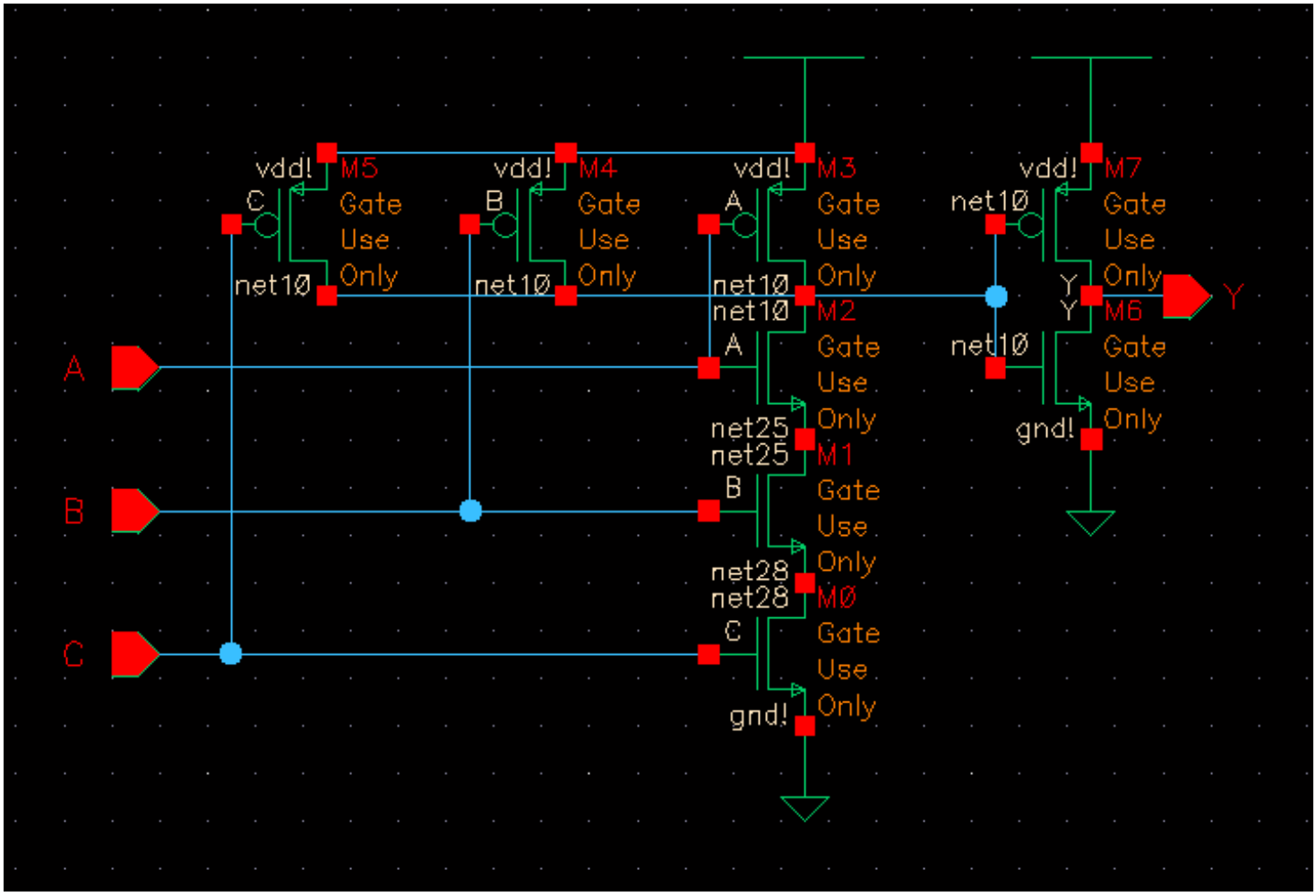
Carry look-ahead full adder:



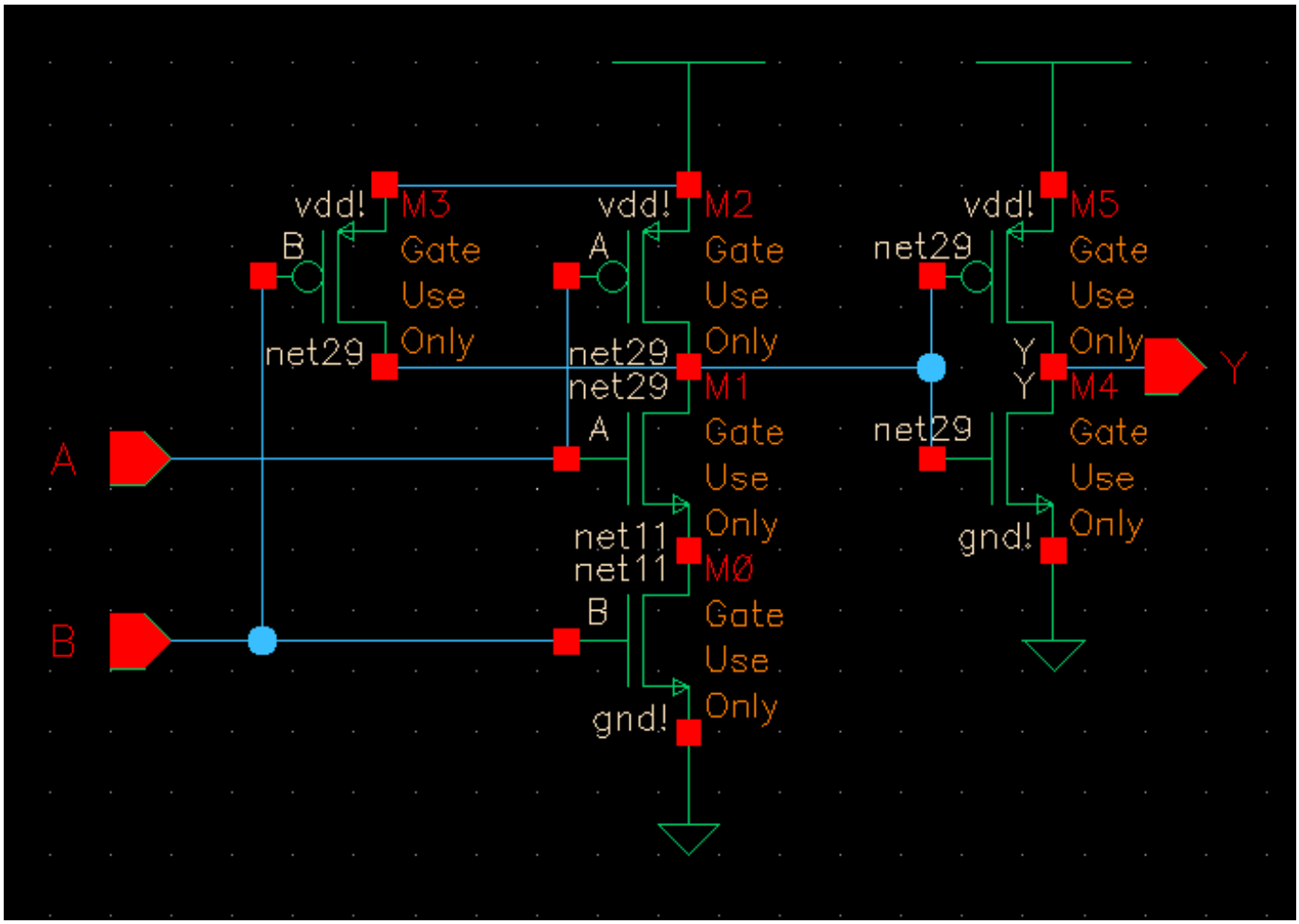
And4:


vdd!
M8
Gate
Use
Only
B
net47
vdd!
M9
A
net47
M10
net68
M11
gnd!
A
B
vddl
M7
net37
M6
net44
M4
M5
Y
net47
net44
gndl
C
D
M0
M1
M2
net59
M3

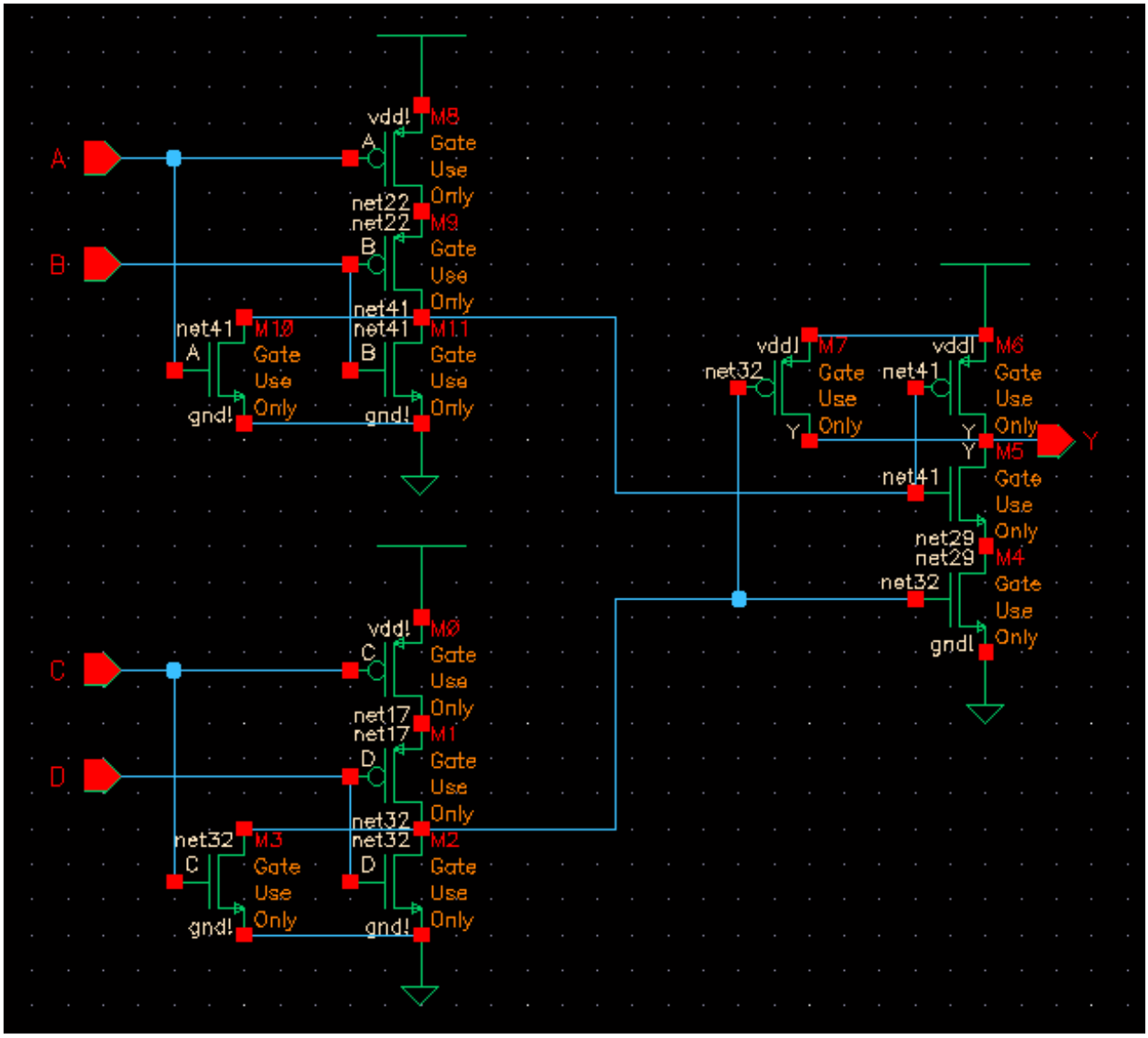
And3:


vdd!
M5
C
Gate
Use
Only
net10
vdd!
M4
B
Gate
Use
Only
net10
vdd!
M3
A
Gate
Use
Only
net10
net10
M2
A
Gate
Use
Only
net25
net25
M1
B
Gate
Use
Only
net28
net28
M0
C
Gate
Use
Only
gnd!
vdd!
M7
net10
Gate
Use
Only
Y
Y
M6
Y
net10
Gate
Use
Only
gnd!
A
B
C

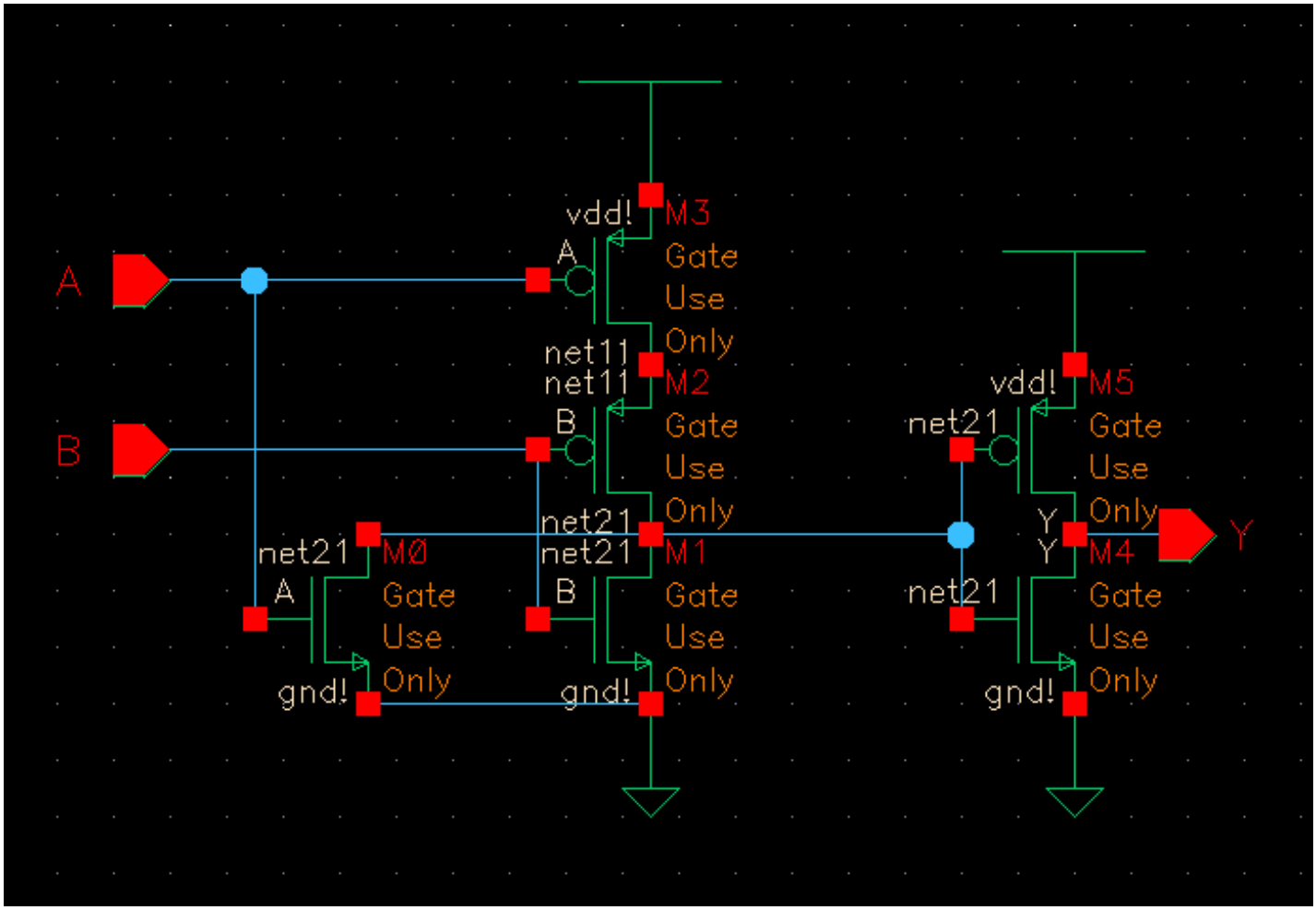
And2:


vdd!
M3
Gate
Use
Only
B
net29
vdd!
M2
Gate
Use
Only
A
net29
net29
M1
Gate
Use
Only
A
net11
net11
MØ
Gate
Use
Only
B
gnd!
vdd!
M5
Gate
Use
Only
net29
Y
Y
M4
Gate
Use
Only
net29
gnd!
A
B
Y

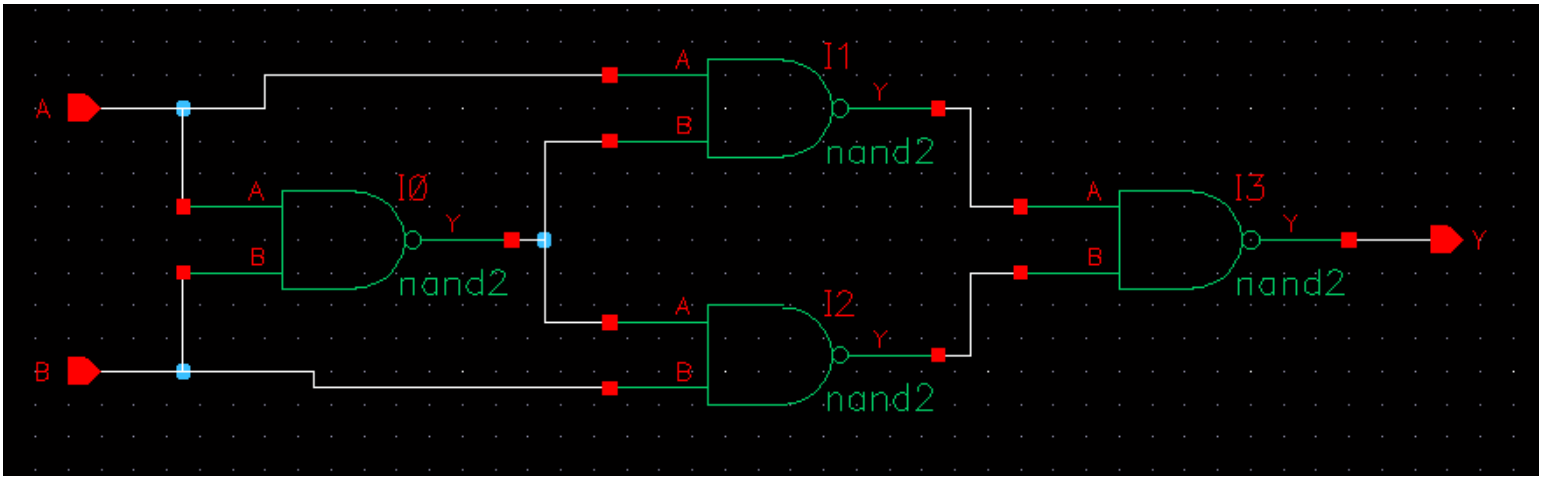
Or4:


A
B
C
D
Y
vdd!
gnd!
net22
net41
net17
net32
net29
M8
M9
M10
M11
M0
M1
M3
M2
M7
M6
M5
M4
Gate
Use
Only

Or2:


A
B
vdd!
M3
A
Gate
Use
Only
net11
net11
M2
B
Gate
Use
Only
net21
net21
M1
B
Gate
Use
Only
gnd!
gnd!
net21
M0
A
Gate
Use
Only
vdd!
M5
net21
Gate
Use
Only
Y
Y
M4
Gate
Use
Only
net21
Y

Xor2:


A
B
A
B
I1
Y
nand2
A
B
I0
Y
nand2
A
B
I2
Y
nand2
A
B
I3
Y
nand2
Y

Nor2:

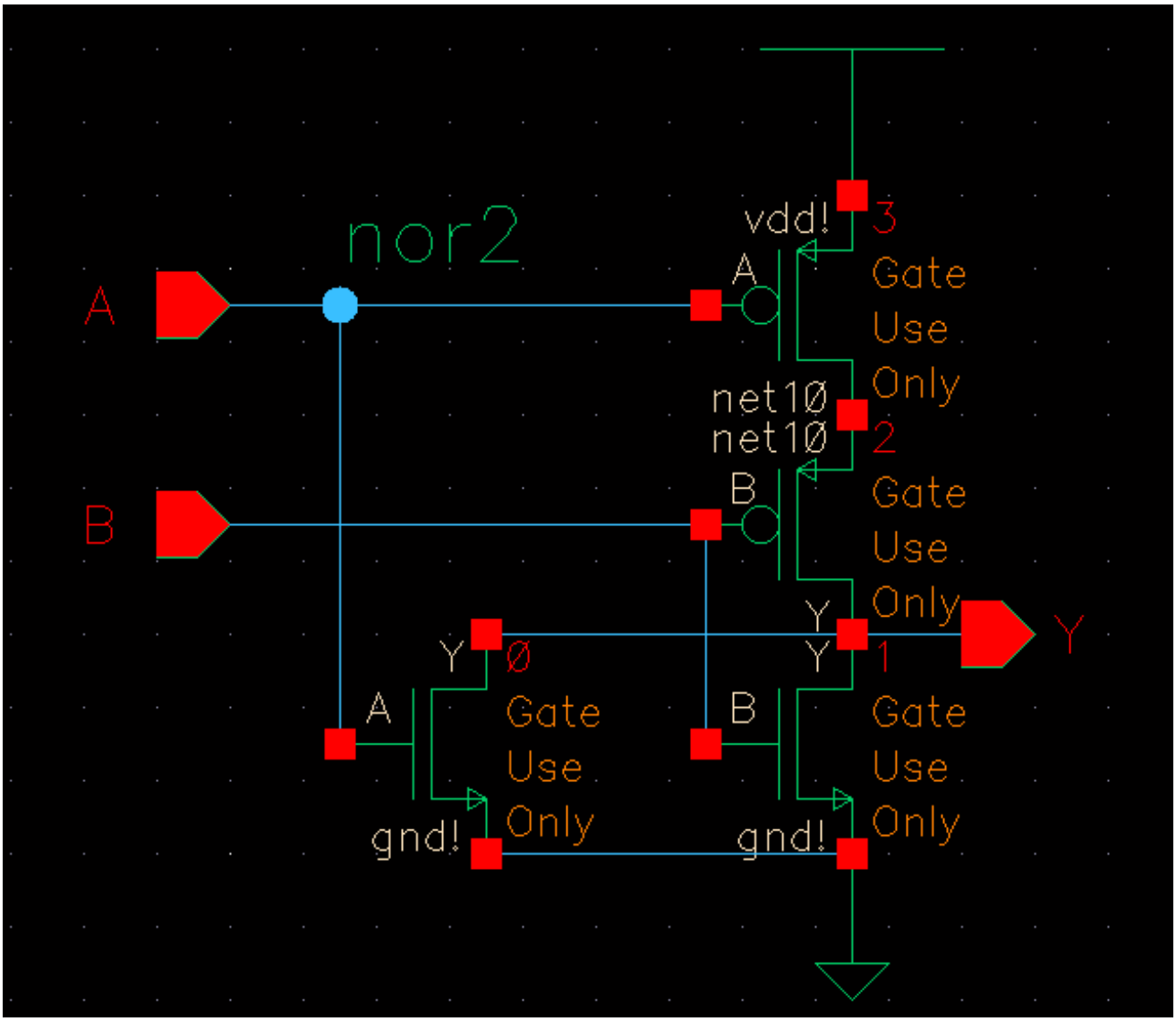



Table of Values:

| | Ripple Carry Adder | Carry Look-ahead Adder |
|---|---|---|
| Clock Frequency @Vdd=2.5V | 594Mhz | 1.34Ghz |

| | | |
|---|---|---|
| Static Power | 1.01E-08W | 1.30E-05W |
| Dynamic Power | 7.70E-09W | 2.59E-06W |