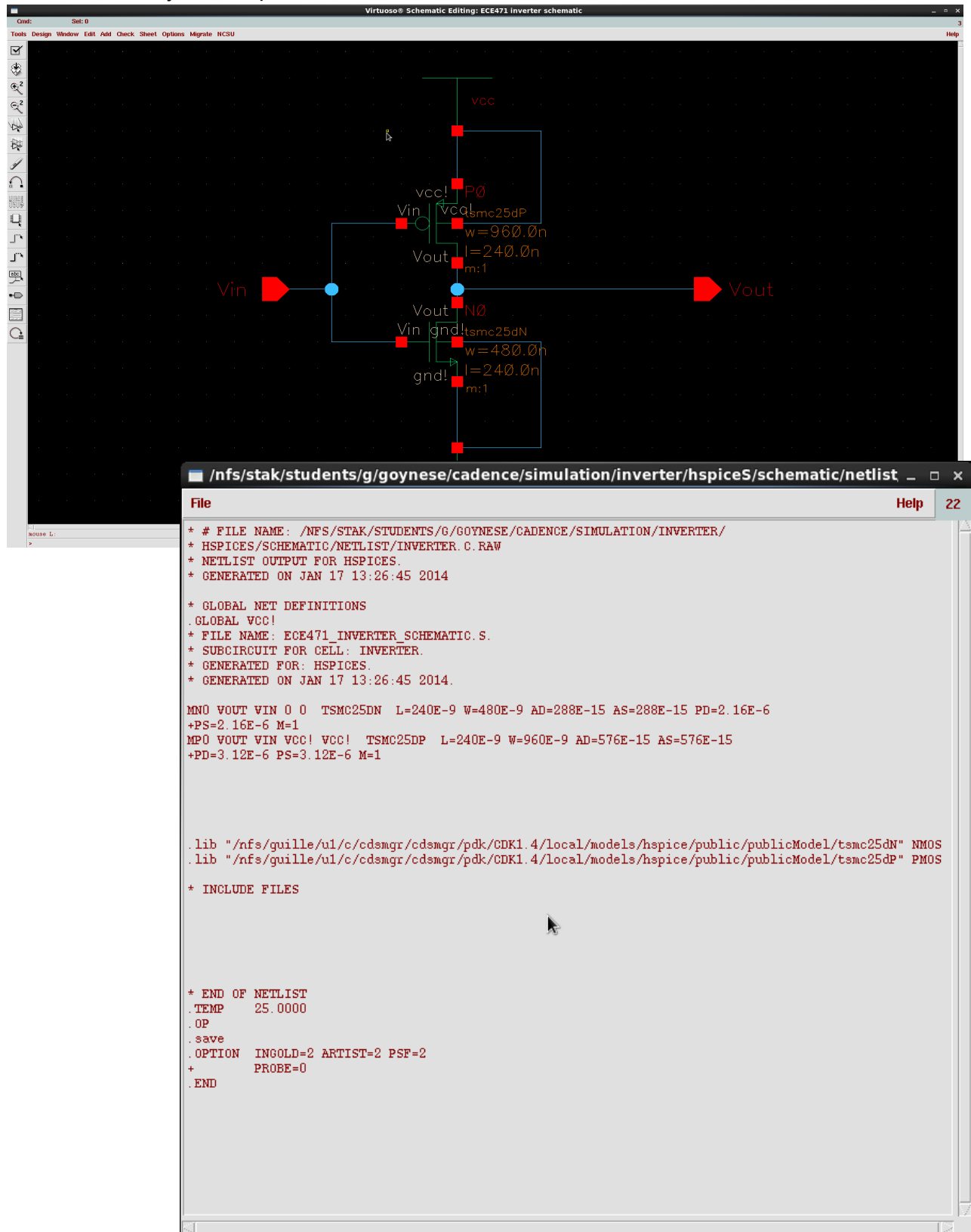


## 1. Screenshots of your completed, error free schematic and HSPICE schematic netlist.



The image displays two screenshots from a Cadence Virtuoso environment. The top screenshot shows a schematic of an inverter circuit. The input signal **Vin** is connected to the gate of a PMOS transistor (**P0**) and the gate of an NMOS transistor (**N0**). The PMOS transistor's source is connected to **VCC** and its drain is connected to the output node **Vout**. The NMOS transistor's source is connected to **gnd!** and its drain is also connected to **Vout**. The PMOS transistor is labeled with parameters: **tsmc25dP**, **w=960.0n**, **l=240.0n**, and **m:1**. The NMOS transistor is labeled with parameters: **tsmc25dN**, **w=480.0n**, **l=240.0n**, and **m:1**. The bottom screenshot shows the HSPICE netlist generated from the schematic, titled **/nfs/stak/students/g/goynese/cadence/simulation/inverter/hspiceS/schematic/netlist**. The netlist contains the following text:

```
* # FILE NAME: /NFS/STAK/STUDENTS/G/GOYNESE/CADENCE/SIMULATION/INVERTER/
* HSPICES/SCHEMATIC/NETLIST/INVERTER.C.RAW
* NETLIST OUTPUT FOR HSPICES.
* GENERATED ON JAN 17 13:26:45 2014

* GLOBAL NET DEFINITIONS
.GLOBAL VCC!
* FILE NAME: ECE471_INVERTER_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: INVERTER.
* GENERATED FOR: HSPICES.
* GENERATED ON JAN 17 13:26:45 2014.

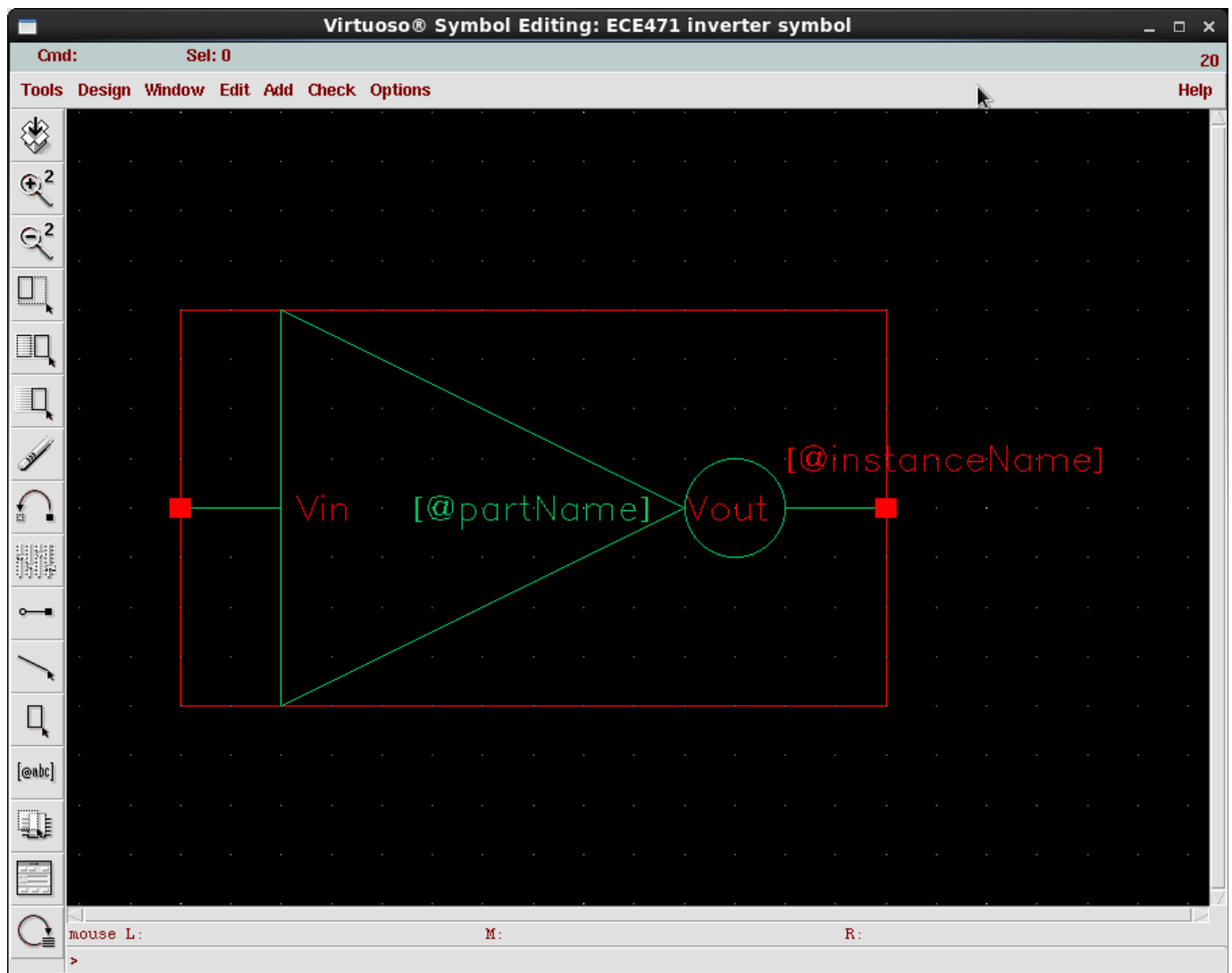
MNO VOUT VIN 0 0 TSMC25DN L=240E-9 W=480E-9 AD=288E-15 AS=288E-15 PD=2.16E-6
+PS=2.16E-6 M=1
MP0 VOUT VIN VCC! VCC! TSMC25DP L=240E-9 W=960E-9 AD=576E-15 AS=576E-15
+PD=3.12E-6 PS=3.12E-6 M=1

.lib "/nfs/guille/u1/c/cdsngr/cdsngr/pdk/CDK1.4/local/models/hspice/public/publicModel/tsmc25dN" NMOS
.lib "/nfs/guille/u1/c/cdsngr/cdsngr/pdk/CDK1.4/local/models/hspice/public/publicModel/tsmc25dP" PMOS

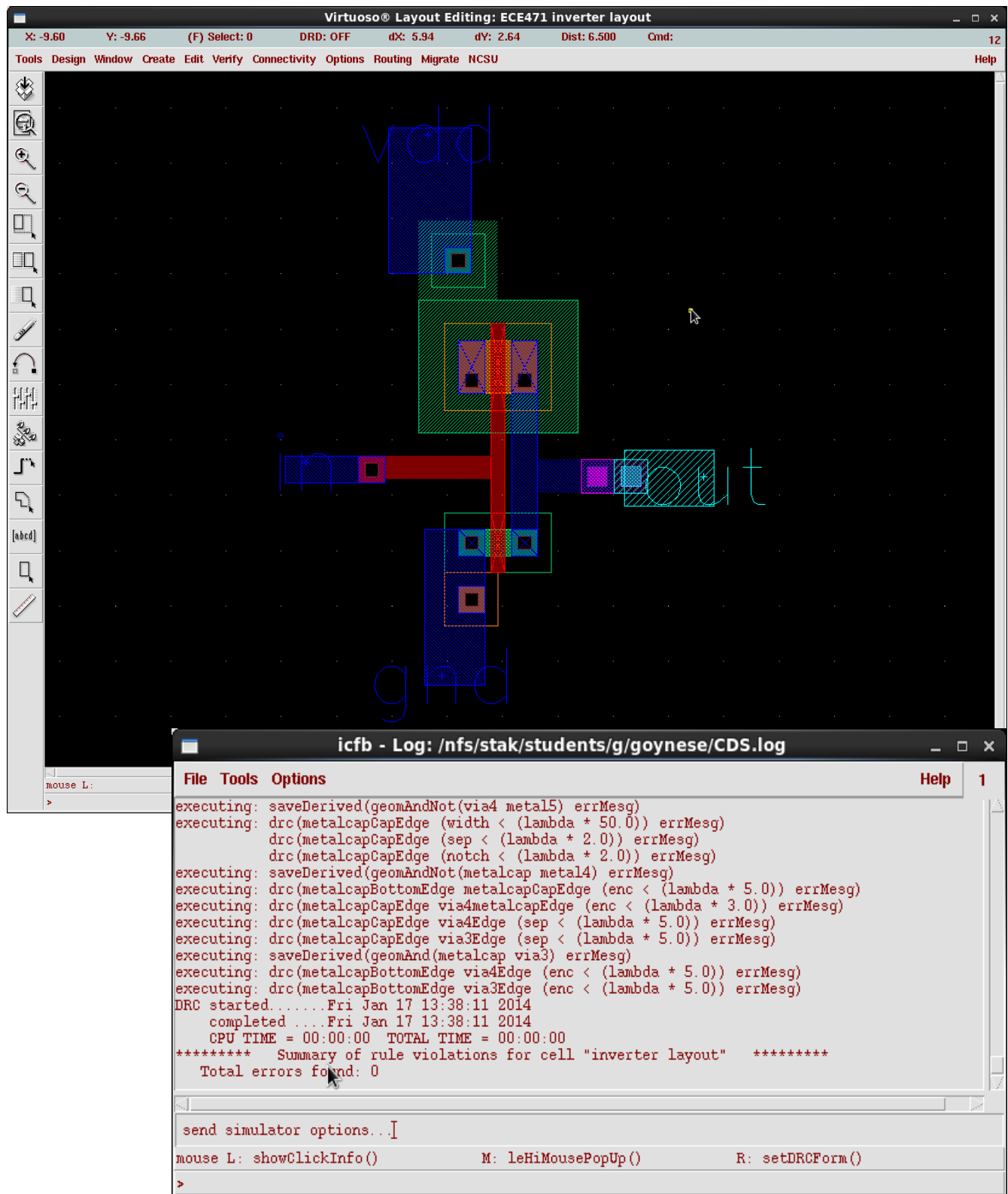
* INCLUDE FILES

* END OF NETLIST
.TEMP 25.0000
.OP
.save
.OPTION INGOLD=2 ARTIST=2 PSF=2
+ PROBE=0
.END
```

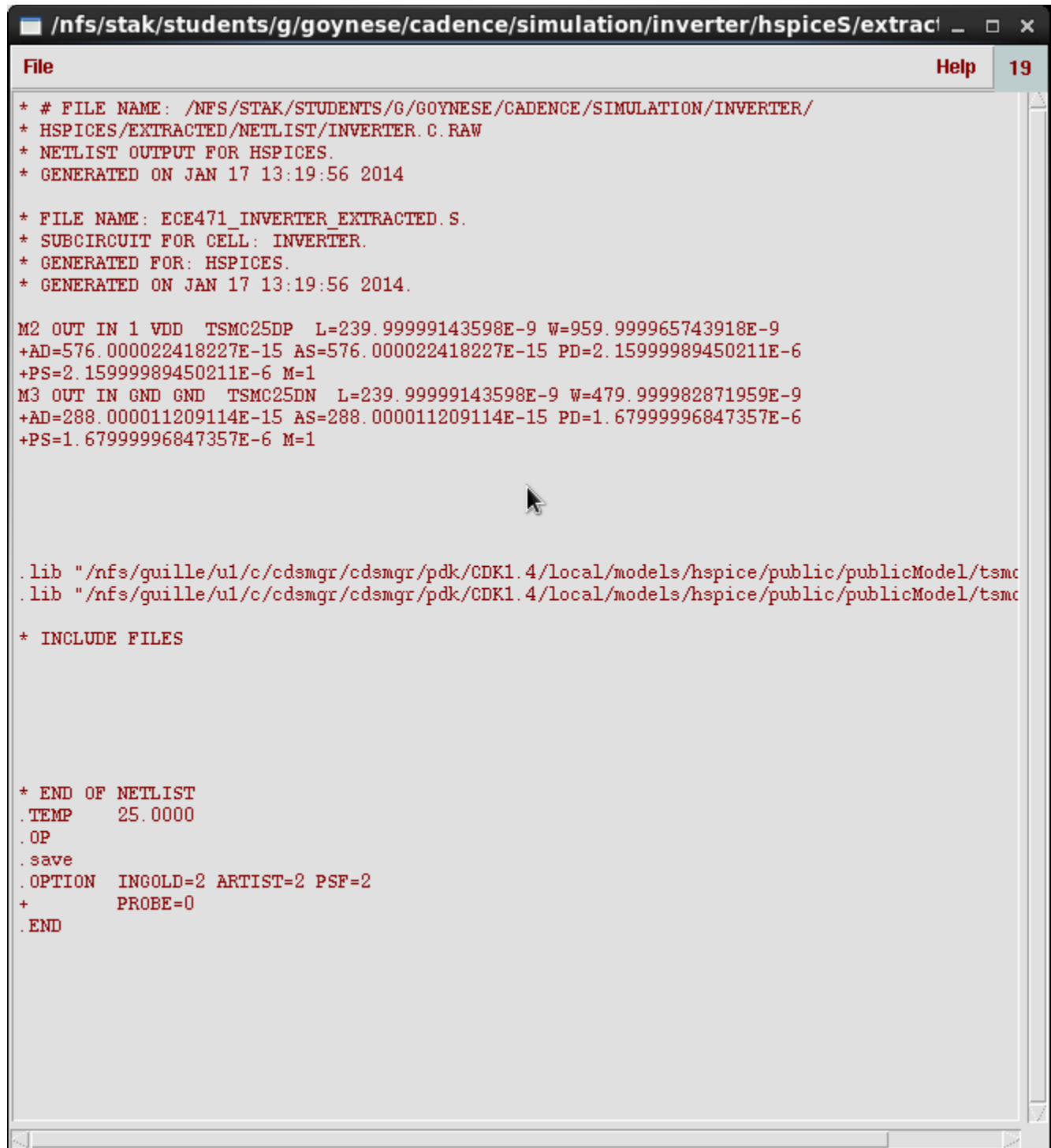
2. A screenshot of your completed symbol.



### 3. Screenshots of your completed, DRC clean layout, and your extracted HSPICE netlist.



## DRC Hspice Screenshot



The screenshot shows a window titled `/nfs/stak/students/g/goynese/cadence/simulation/inverter/hspiceS/extract`. The window has a menu bar with `File` and `Help`, and a page number `19` in the top right corner. The main area displays a netlist for an inverter simulation. The netlist includes comments about the file name, subcircuit, and generation date. It defines two MOSFETs, M2 and M3, with their parameters and connections. It also includes library paths for TSMC models and a list of include files. The netlist ends with `.END`.

```
* # FILE NAME: /NFS/STAK/STUDENTS/G/GOYNESE/CADENCE/SIMULATION/INVERTER/
* HSPICES/EXTRACTED/NETLIST/INVERTER.C.RAW
* NETLIST OUTPUT FOR HSPICES.
* GENERATED ON JAN 17 13:19:56 2014

* FILE NAME: ECE471_INVERTER_EXTRACTED.S.
* SUBCIRCUIT FOR CELL: INVERTER.
* GENERATED FOR: HSPICES.
* GENERATED ON JAN 17 13:19:56 2014.

M2 OUT IN 1 VDD TSMC25DP L=239.99999143598E-9 W=959.999965743918E-9
+AD=576.000022418227E-15 AS=576.000022418227E-15 PD=2.15999989450211E-6
+PS=2.15999989450211E-6 M=1
M3 OUT IN GND GND TSMC25DN L=239.99999143598E-9 W=479.999982871959E-9
+AD=288.000011209114E-15 AS=288.000011209114E-15 PD=1.67999996847357E-6
+PS=1.67999996847357E-6 M=1

.lib "/nfs/guille/ul/c/cdsmgr/cdsmgr/pdk/CDK1.4/local/models/hspice/public/publicModel/tsmc
.lib "/nfs/guille/ul/c/cdsmgr/cdsmgr/pdk/CDK1.4/local/models/hspice/public/publicModel/tsmc

* INCLUDE FILES

* END OF NETLIST
.TEMP 25.0000
.OP
.save
.OPTION INGOLD=2 ARTIST=2 PSF=2
+ PROBE=0
.END
```

4. An explanation of any problems you may have had.

First we had problems running Cadence using the tcsl, we had to make sure to use the Cshell csl, just some menus didn't show up. I remember another problem I had was I used the wrong metal layer for parts of my design, so I had to redo these. When drawing the traces connecting the gates together I received a DRC error. I didn't know what was wrong, but Neil told me what I did wrong. Lab 2 otherwise went smoothly, I just followed the directions and everything worked out. In the process I learned how to complete a design in Cadence.

5. Why is it important to simulate your circuit both after schematic and post-layout? (after parasitic extraction)

Before layout when we simulate our design we are essentially just simulating the circuit, without the included parasitic capacitance's, and other parasitics. After layout and we connect everything with large area traces parasitics are added, therefore we need to re-simulate our design taking into account these added effects.