ECE471– Energy Efficient VLSI Design

Project 6 – 4-bit Adders

Due Date – 11:30pm on Friday, February 29^{th} 2013

Introduction

Now that you have made a functional full adder, we are going to create and compare two different 4-bit adder architectures. First you will make a ripple carry adder and simulate its power and worst-case delay. Then you will make a carry-lookahead adder, and simulate for the same numbers.

The 4-bit ripple-carry adder schematic and simulation

- Using your full-adder create a 4-bit ripple-carry adder (schematic only) with pipelined inputs and outputs. The ripple-carry architecture is shown in figure 1. you may need to add inverters at the outputs of the adder you designed for previous lab. you can use any type of D-FF or Registers. one option is Figure 7-26 on page 347 of text book or simply look for D-FF on Wikipedia!

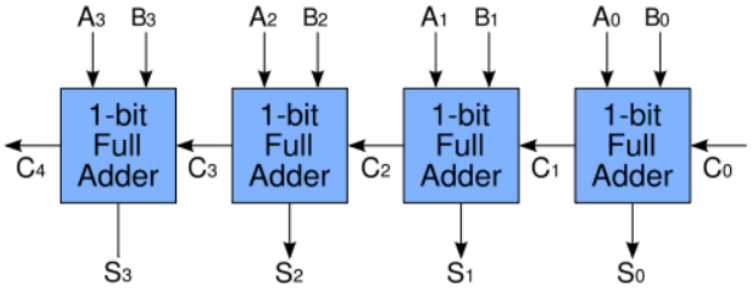

Figure 1: 4-bit ripple carry adder.

- Determine the clock frequency that this adder can run at (at nominal V_{DD}), as well as the dynamic and static power. Keep in mind that it is limited by the worst-case delay.

The 4-bit carry-lookahead adder schematic and simulation

- Now we want to employ the carry-lookahead architecture similar to figure 2. For this you will have to create a schematic for a new CLA full-adder block which has functional behavior described by:

$$\begin{aligned} S &= A \oplus B \oplus C_{in} \\ C_{out} &= (A \cdot B) + (C_{in} \cdot (A \oplus B)) \\ G_i &= A_i \cdot B_i \\ P_i &= A_i \oplus B_i \end{aligned}$$

- To do this, you will need to create your own and, or, and xor cells (schematic only).

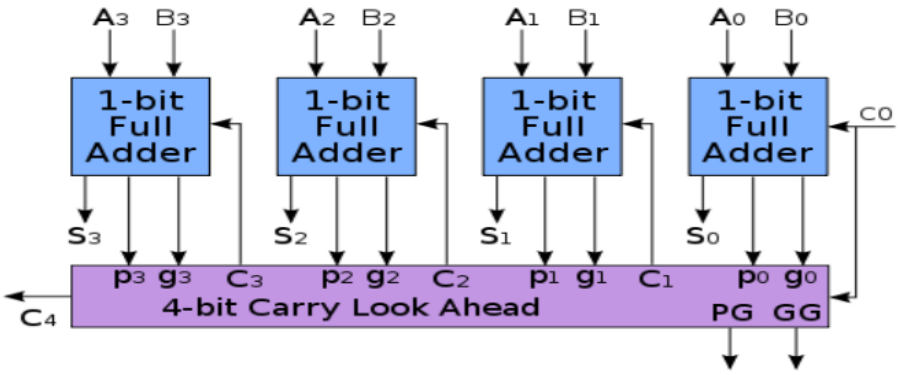

Figure 2: A 4-bit adder with Carry Look Ahead (CLA)

- Next you will need to create a separate block for the Carry Look Ahead unit. Here are the equations describing a 4-bit CLA unit:

$$\begin{aligned} C_1 &= G_0 + P_0 \cdot C_0 \\ C_2 &= G_1 + P_1 \cdot C_1 \\ C_3 &= G_2 + P_2 \cdot C_2 \\ C_4 &= G_3 + P_3 \cdot C_3 \end{aligned}$$

  Now substitute C_1 into C_2, C_2 into C_3, etc. we get:

$$\begin{aligned} C_1 &= G_0 + P_0 \cdot C_0 \\ C_2 &= G_1 + P_1 \cdot (G_0 + P_0 \cdot C_0) \\ C_3 &= G_2 + P_2 \cdot (G_1 + P_1 \cdot (G_0 + P_0 \cdot C_0)) \\ C_4 &= G_3 + P_3 \cdot (G_2 + P_2 \cdot (G_1 + P_1 \cdot (G_0 + P_0 \cdot C_0))) \end{aligned}$$

- Once you have finished, determine the frequency (at nominal V_{DD}) that the CLA adder can run at as well as the static and dynamic power. Create a table showing the results for both the ripple-carry and CLA adders.

What to turn in

Please turn in a pdf/tar file to TEACH by 11:30pm on Friday, February 29^{th} with the following things:

- Screenshots of your completed, error free schematics (include every new block that you made).
- A table of values you simulated from the two adders.