ECE471– Energy Efficient VLSI Design

Project 3 – Measuring Delay of Different Inverter Configurations

Due Date – 11:30pm on Friday, January 31^{st} 2014

Introduction

By this lab you should have a general understanding of the basics of HSPICE, as well as how to create a schematic and layout in Cadence. This week we are going to combine these two skills. First, you will simulate the inverter schematic and post-layout netlists from last week and compare the differences in dynamic power, propagation delays, and energy. Then we will create a new circuit that combines two inverters, adding wire skew between them in both the schematic and the layout which will give us an idea about how interconnects can affect the total delay of a circuit.

Initial HSPICE simulations

Perform the following using your results from the previous lab.

1. Simulate your schematic and post-layout netlists in HSPICE using similar techniques to Lab 1. For the measurement of the delay, start from when the input is at 10% of `vdd` to when the output is at 10% of `vdd` (assuming then input is switching from $0 \rightarrow 1$).
2. Create a table comparing the dynamic power, delay, and energy.

Creation of a new circuit

In this section we will create a circuit that is a simple chain of two inverters. We will create the schematic, then the layout, and return to the schematic to add wire skew that corresponds to the layout.

1. Create a new cell titled "lab3circuit" and open the schematic view.
2. Add the inverters to your schematic the same way that you would add a transistor. The inverter should be located in your ECE471 library that you created last lab (if you don't see it immediately in your `Component Browser` window under the ECE471 library, you might have to look in the "`Uncategorized`" library).
3. Connect the output of the first inverter to the input of the second inverter. Create an input pin, output pin, vdd and ground pins, and connect them accordingly. Save your schematic.
4. Create a new layout view for this cell. remember to select layout as the View Name and Virtouso as Tool. Add the inverters to the layout the same way you added transistors in the previous lab. They will once again be located in your ECE471 library, be sure to select "`layout`" as the view you want to add.
5. Line the two inverter cells up horizontally, and create `vdd` and `gnd` rails similar to figure 1.
6. Now we want to connect the output of the first inverter to the input of the second inverter. We will do this using the M5 layer. Use vias (M1_M2, M2_M3, etc.) to get to M5 on both sides, then connect the two with a 1mm-long and 5um-wide wire of M5 (In order to accomplish this, you might have to move your inverter cells much farther apart). to define size of wire press 'q' on it and change '`Left`','`Right`', '`Top`' and '`Bottom`' fields appropriately. all units in this window are in micron. these values should be multiplier of '`X snap Spacing`' parameter defined in $Options \rightarrow Display$.
7. Finally, create input, output, and vdd/gnd pins for the layout.

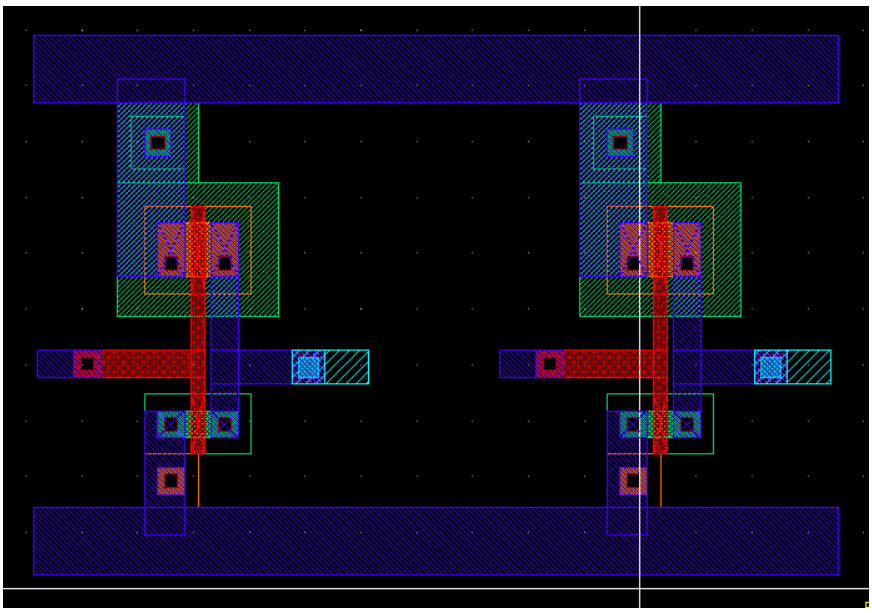

Figure 1: Layout of two inverters.

Adjusting the Schematic to Include Wire Delay

Use these steps to add wire delay to your schematic.

1. We are going to represent wire delay between the two inverters in the schematic using a π model, which is shown on page 171 of the book and can also be found in the lecture notes.
2. The values for R and C in the π model are dependent on the length and width of your M5 wire in the layout.
    - To find the capacitance value, refer to example 4.1 in the book, for this you will need to use the values in the `Field` column and the A15 row of Table 4-2. We are only concerned with area and fringing capacitance.
    - To find the resistance value, use equation 4.4 from the book, and a sheet resistance value of 0.1Ω.
3. Integrate the π model with the correct values into your schematic using the resistor and capacitor models in the $NCSU\ Analog\ Parts \rightarrow R\_L\_C$ library.
4. Take a screenshot of your finished and error-free schematic. Then generate a HSPICE netlist from both your schematic and post-layout extraction like last weeks lab.

Simulations and Circuit Variation

Perform the following simulations.

1. Perform HSPICE simulations on your new netlists and once again compare delay, power, and energy. Keep in mind that now that we have two inverters, we will want the delay target to be at a different output voltage level.
2. Next, model wire delay on your schematic using the π3 model from page 171 (or the lecture notes). Generate a SPICE netlist and simulate this circuit. Create a table showing the delay, power, and energy number for the π3 model, π model, and layout.
3. Now extend the length of the wire between the two inverter stages in the layout to 20mm. Once again implement both the π3 model and π model on the schematic and simulate all three netlists. Take screenshots of all three and generate a table showing your results.

What to turn in

Please turn in a PDF to TEACH by 11:30pm on Friday, January 31^{st} with the following things:

- Screenshots of ALL of your completed, error free schematics and HSPICE schematic netlists.
- A screenshot of BOTH of your completed, DRC clean layouts, and your extracted HSPICE netlists.
- Any hand calculations you needed to do (to find the values for the π-models).
- ALL necessary tables showing your simulation results.
- An explanation of any problems you may have had.