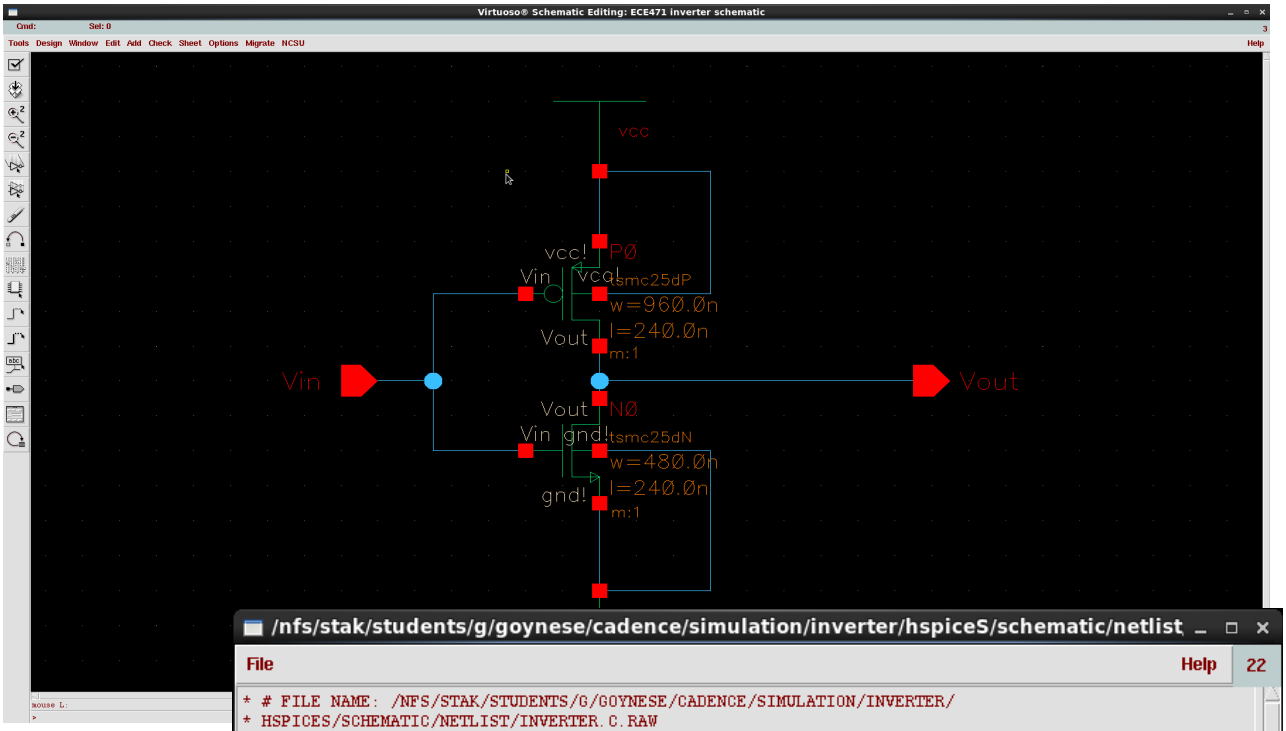
Eddie Goynes
Kris Schneider

ECE 471 Lab 2 Write Up

1. Screenshots of your completed, error free schematic and HSPICE schematic netlist.

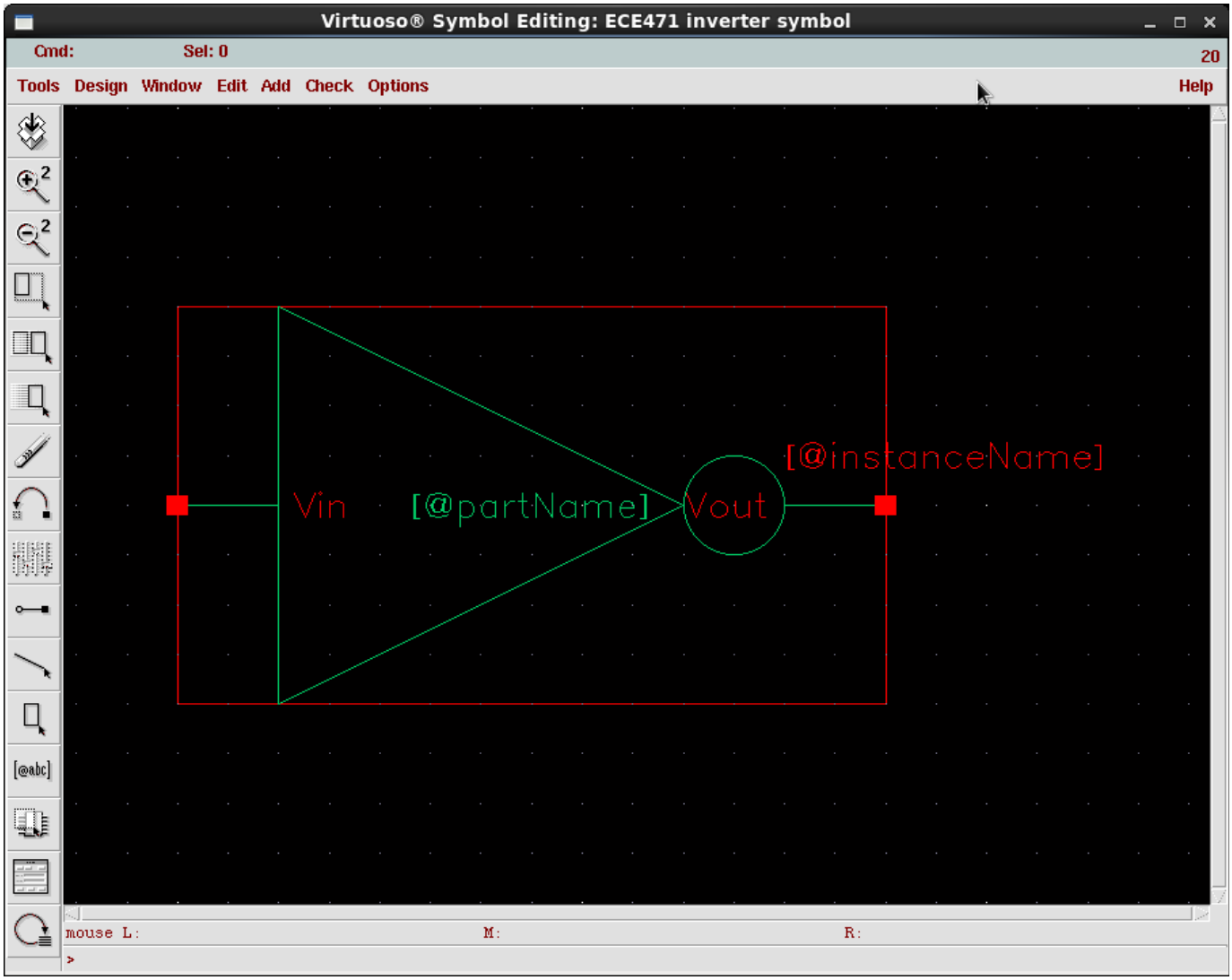


/nfs/stak/students/g/goynese/cadence/simulation/inverter/hspiceS/schematic/netlist

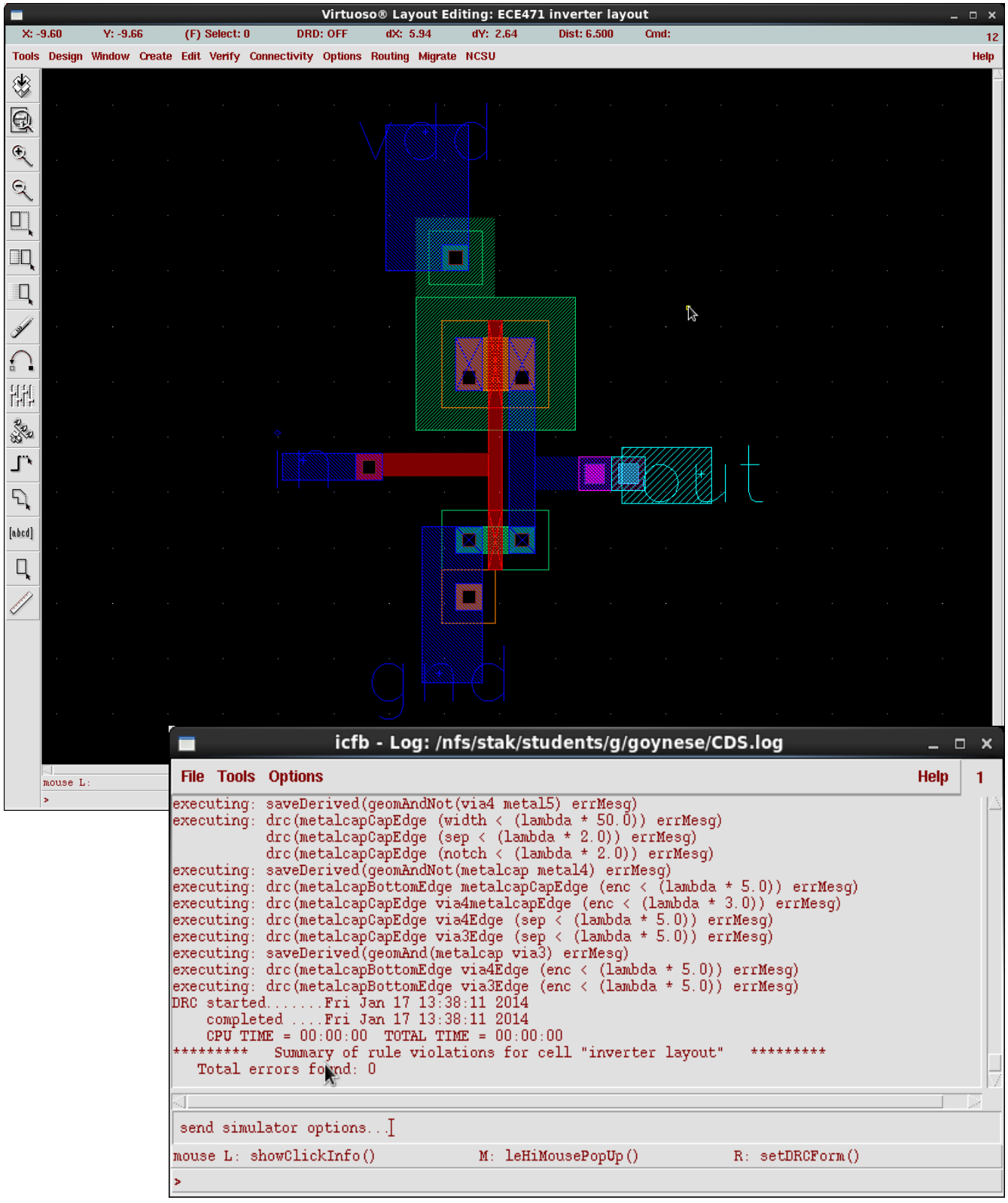
File Help 22

```
* # FILE NAME: /NFS/STAK/STUDENTS/G/GOYNESE/CADENCE/SIMULATION/INVERTER/
* HSPICES/SCHEMATIC/NETLIST/INVERTER.C.RAW
* NETLIST OUTPUT FOR HSPICES.
* GENERATED ON JAN 17 13:26:45 2014

* GLOBAL NET DEFINITIONS
.GLOBAL VCC!
* FILE NAME: ECE471_INVERTER_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: INVERTER.
* GENERATED FOR: HSPICES.
* GENERATED ON JAN 17 13:26:45 2014.

MN0 VOUT VIN 0 0  TSMC25DN  L=240E-9 W=480E-9 AD=288E-15 AS=288E-15 PD=2.16E-6
+PS=2.16E-6 M=1
MP0 VOUT VIN VCC! VCC!  TSMC25DP  L=240E-9 W=960E-9 AD=576E-15 AS=576E-15
+PD=3.12E-6 PS=3.12E-6 M=1




.lib "/nfs/guille/u1/c/cdsmgr/cdsmgr/pdk/CDK1.4/local/models/hspice/public/publicModel/tsmc25dN" NMOS
.lib "/nfs/guille/u1/c/cdsmgr/cdsmgr/pdk/CDK1.4/local/models/hspice/public/publicModel/tsmc25dP" PMOS

* INCLUDE FILES




* END OF NETLIST
.TEMP    25.0000
.OP
.save
.OPTION  INGOLD=2 ARTIST=2 PSF=2
+        PROBE=0
.END
```

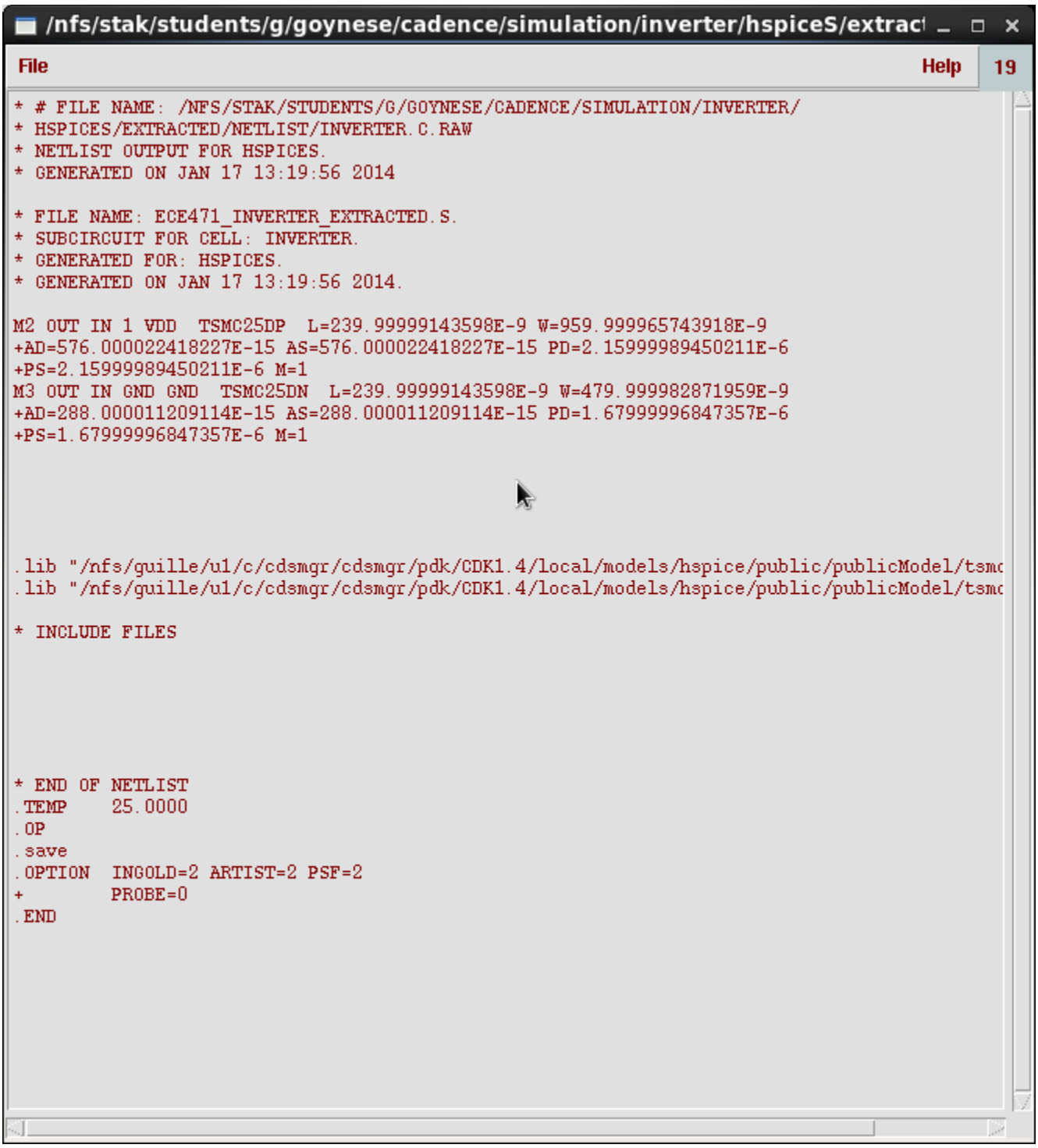
2. A screenshot of your completed symbol.



3. Screenshots of your completed, DRC clean layout, and your extracted HSPICE netlist.



DRC Hpice Screenshot



4. An explanation of any problems you may have had.

First we had problems running Cadence using the tcsl, we had to make sure to use the Cshell csl, just some menus didn't show up. I remember another problem I had was I used the wrong metal layer for parts of my design, so I had to redo these. When drawing the traces connecting the gates together I received a DRC error. I didn't know what was wrong, but Neil told me what I did wrong. Lab 2 otherwise went smoothly, I just followed the directions and everything worked out. In the process I learned how to complete a design in Cadence.

5. Why is it important to simulate your circuit both after schematic and post-layout? (after parasitic extraction)

Before layout when we simulate our design we are essentially just simulating the circuit, without the included parasitic capacitance's, and other parasitics. After layout and we connect everything with large area traces paracitics are added, therefore we need to re-simulate our design taking into account these added effects.