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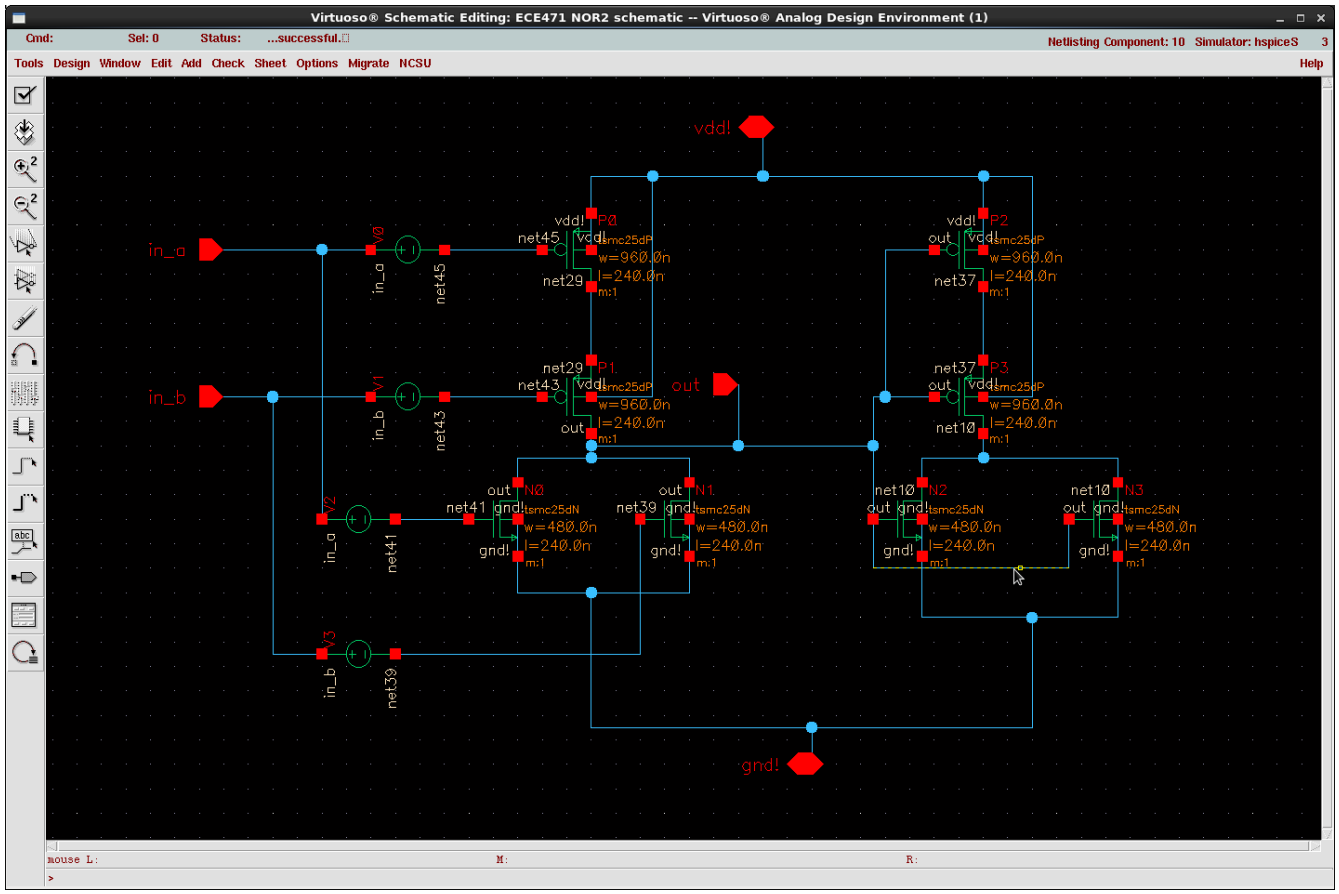
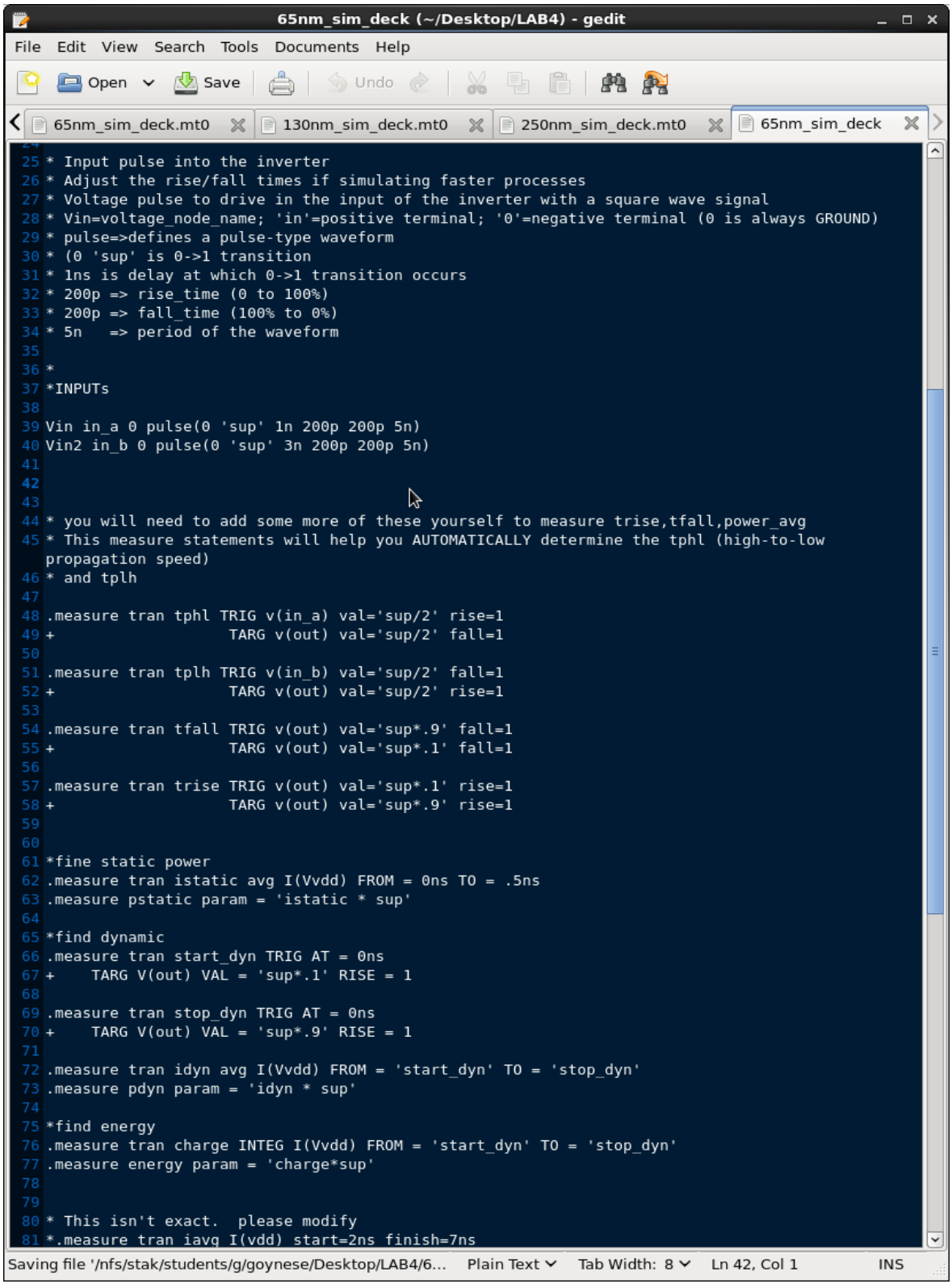
ECE 471 LAB 4 Write UP

1. Here is our Completed Error Free Schematic.



2. One of the nor2 sim_decks are attached. :)
I thought is was easier just to include how we simulated the rise fall, static, esc.



3. The Four completed Tables of data.

Nominal

	tphl	tplh	trise	tfall	Dynamic Pwr	Static Pwr
0.25um	8.42E-11	1.38E-10	2.68E-10	1.13E-10	2.59E-04	1.81E-10
0.13um	3.61E-11	6.94E-11	1.02E-10	7.46E-11	6.66E-05	1.60E-08
65nm	2.59E-11	5.08E-11	8.13E-11	6.16E-11	2.30E-05	1.73E-08
32nm	2.10E-11	2.21E-11	5.85E-11	5.44E-11	1.26E-05	1.02E-08
16nm	2.63E-11	2.78E-11	8.05E-11	6.86E-11	2.06E-06	7.71E-09

Slower Pmos Devices (by 50mV)

	tphl	tplh	trise	tfall	Dynamic Pwr	Static Pwr
0.25um	8.86E-11	1.33E-10	2.64E-10	1.15E-10	2.63E-04	9.60E-11
0.13um	4.47E-11	6.04E-11	1.02E-10	7.47E-11	6.75E-05	6.43E-09
65nm	3.65E-11	4.00E-11	8.03E-11	6.17E-11	2.33E-05	7.12E-09
32nm	3.26E-11	1.05E-11	5.83E-11	5.48E-11	1.27E-05	3.04E-09
16nm	4.10E-11	1.23E-11	7.94E-11	6.89E-11	2.09E-06	2.25E-09

110% Supply Voltage and Faster Nmos & Pmos Devices (by 50mV)

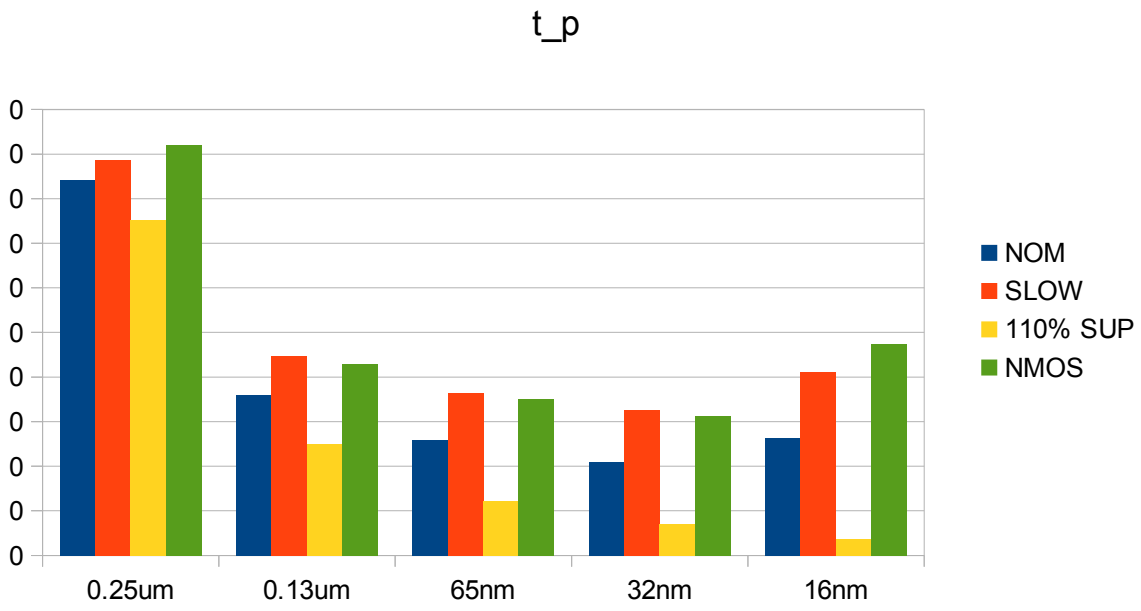
	tphl	tplh	trise	tfall	Dynamic Pwr	Static Pwr
0.25um	7.52E-11	1.38E-10	2.57E-10	1.11E-10	3.35E-04	5.33E-10
0.13um	2.49E-11	7.55E-11	9.84E-11	7.62E-11	8.95E-05	7.66E-08
65nm	1.23E-11	5.80E-11	7.72E-11	6.33E-11	3.24E-05	8.12E-08
32nm	7.04E-12	3.04E-11	5.71E-11	5.50E-11	1.98E-05	5.93E-08
16nm	3.68E-12	3.51E-11	7.50E-11	6.65E-11	3.20E-06	5.08E-08

Nmos & Pmos Lengths Increased by 10%

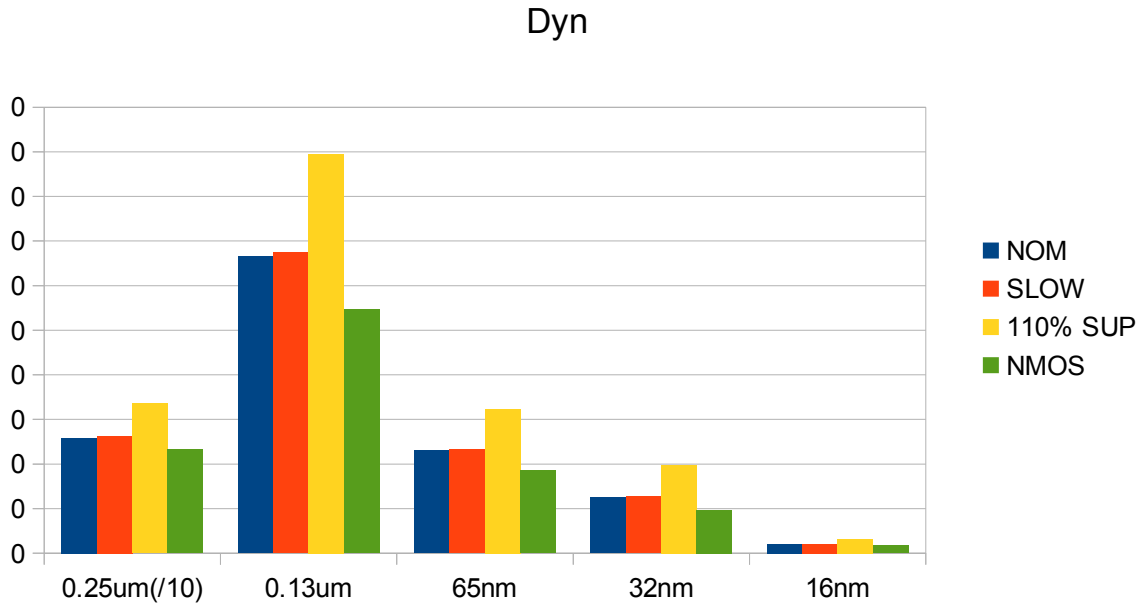
	tphl	tplh	trise	tfall	Dynamic Pwr	Static Pwr
0.25um	9.19E-11	1.56E-10	3.00E-10	1.25E-10	2.32E-04	1.82E-10
0.13um	4.29E-11	8.28E-11	1.20E-10	7.42E-11	5.47E-05	7.36E-09
65nm	3.51E-11	6.39E-11	9.26E-11	5.81E-11	1.86E-05	6.25E-09
32nm	3.12E-11	3.30E-11	5.85E-11	4.96E-11	9.67E-06	1.67E-09
16nm	4.74E-11	5.16E-11	8.07E-11	5.84E-11	1.73E-06	7.11E-10

4. The three plots of results.

The Dynamic power graph seems reasonable. Reduction in the process sizing should reduce the switching on off power of the transistors. The rise fall t_p delay decreasing with reduction in size, and the static power seemed to increase when the size was reduced. We think since Patrick said in class that smaller transistors leak about the same amount of current as larger ones, and it's a property of the materials used rather than the process.



:Note on the Dynamic power graph the 0.25um values were divided by 10 to allow for better definition of the other process sizes.



:Note on the Leak graph the 0.25um values were multiplied by 10 to allow for better definition of the other process sizes.