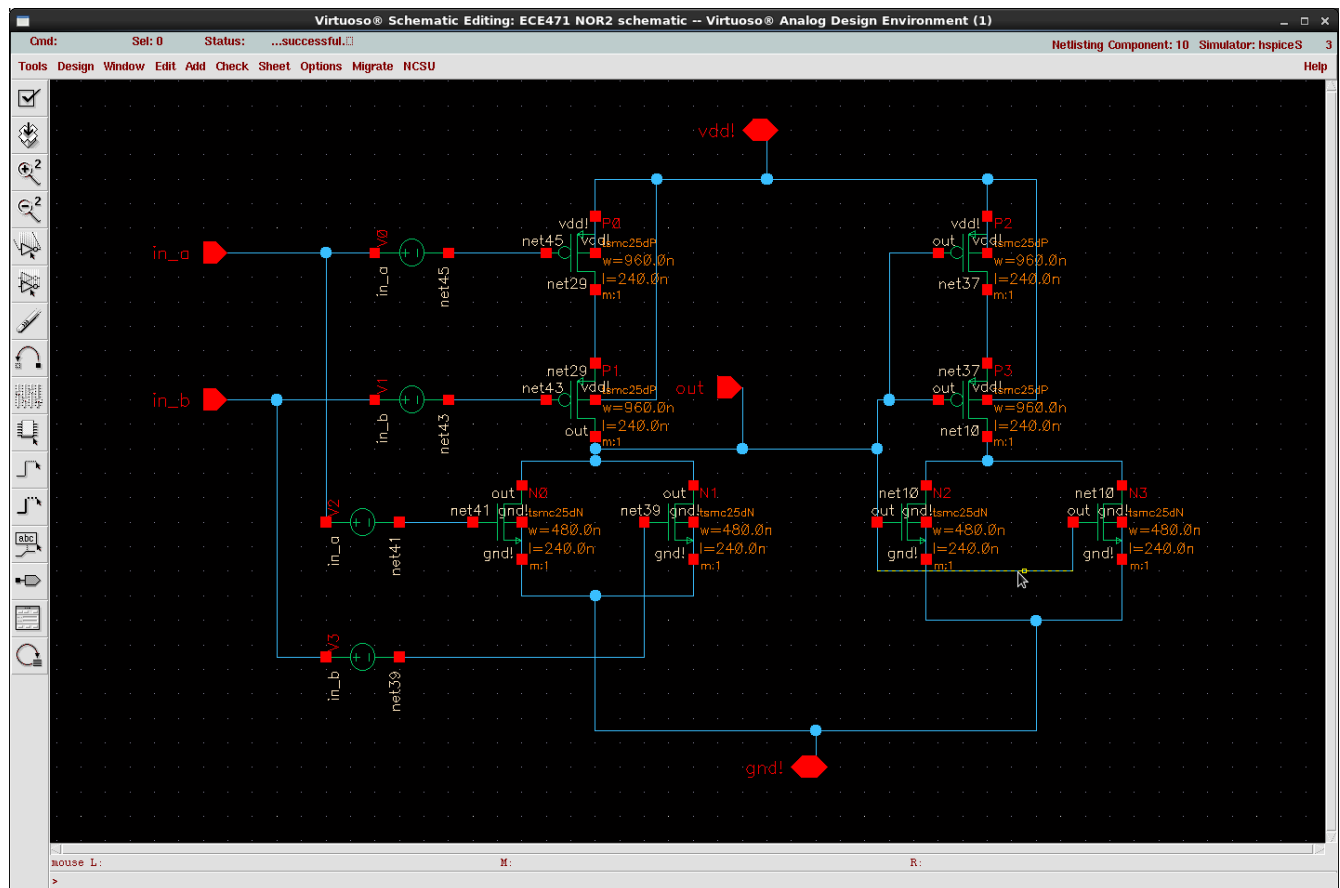
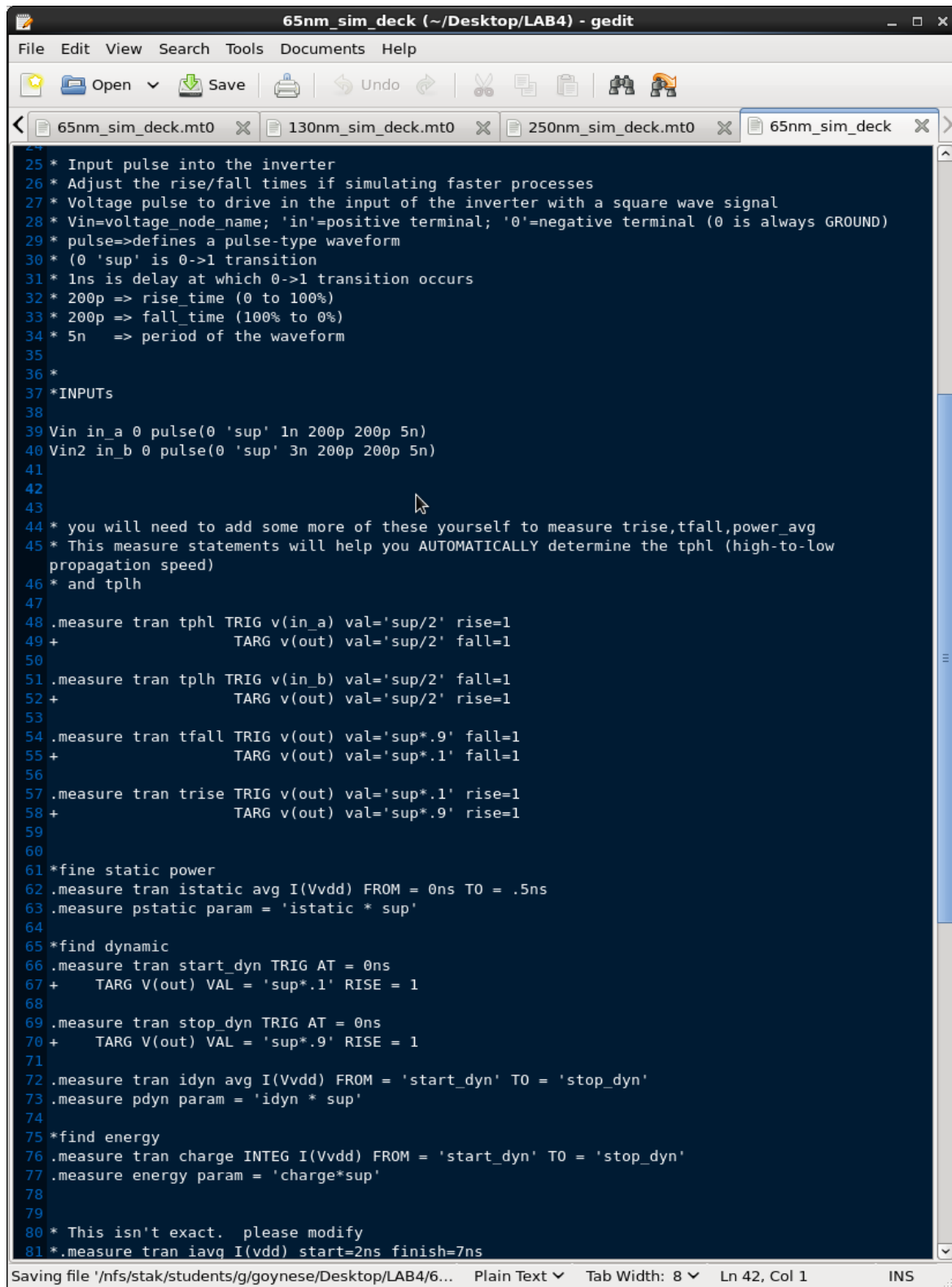


1. Here is our Completed Error Free Schematic.



2. One of the nor2 sim_decks are attached. :)

I thought it was easier just to include how we simulated the rise fall, static, esc.



```
65nm_sim_deck (~/Desktop/LAB4) - gedit
File Edit View Search Tools Documents Help
Open Save Undo
65nm_sim_deck.mt0 130nm_sim_deck.mt0 250nm_sim_deck.mt0 65nm_sim_deck
25 * Input pulse into the inverter
26 * Adjust the rise/fall times if simulating faster processes
27 * Voltage pulse to drive in the input of the inverter with a square wave signal
28 * Vin=voltage_node_name; 'in'=positive terminal; '0'=negative terminal (0 is always GROUND)
29 * pulse=>defines a pulse-type waveform
30 * (0 'sup' is 0->1 transition
31 * 1ns is delay at which 0->1 transition occurs
32 * 200p => rise_time (0 to 100%)
33 * 200p => fall_time (100% to 0%)
34 * 5n => period of the waveform
35
36 *
37 *INPUTs
38
39 Vin in_a 0 pulse(0 'sup' 1n 200p 200p 5n)
40 Vin2 in_b 0 pulse(0 'sup' 3n 200p 200p 5n)
41
42
43
44 * you will need to add some more of these yourself to measure trise,tfall,power_avg
45 * This measure statements will help you AUTOMATICALLY determine the tphl (high-to-low
  propagation speed)
46 * and tplh
47
48 .measure tran tphl TRIG v(in_a) val='sup/2' rise=1
49 + TARG v(out) val='sup/2' fall=1
50
51 .measure tran tplh TRIG v(in_b) val='sup/2' fall=1
52 + TARG v(out) val='sup/2' rise=1
53
54 .measure tran tfall TRIG v(out) val='sup*.9' fall=1
55 + TARG v(out) val='sup*.1' fall=1
56
57 .measure tran trise TRIG v(out) val='sup*.1' rise=1
58 + TARG v(out) val='sup*.9' rise=1
59
60
61 *fine static power
62 .measure tran istatic avg I(Vvdd) FROM = 0ns TO = .5ns
63 .measure pstatic param = 'istatic * sup'
64
65 *find dynamic
66 .measure tran start_dyn TRIG AT = 0ns
67 + TARG V(out) VAL = 'sup*.1' RISE = 1
68
69 .measure tran stop_dyn TRIG AT = 0ns
70 + TARG V(out) VAL = 'sup*.9' RISE = 1
71
72 .measure tran idyn avg I(Vvdd) FROM = 'start_dyn' TO = 'stop_dyn'
73 .measure pdyn param = 'idyn * sup'
74
75 *find energy
76 .measure tran charge INTEG I(Vvdd) FROM = 'start_dyn' TO = 'stop_dyn'
77 .measure energy param = 'charge*sup'
78
79
80 * This isn't exact. please modify
81 *.measure tran iavq I(vdd) start=2ns finish=7ns

Saving file '/nfs/stak/students/g/goynese/Desktop/LAB4/6... Plain Text Tab Width: 8 Ln 42, Col 1 INS
```

3. The Four completed Tables of data.

Nominal						
	tphl	tplh	trise	tfall	Dynamic Pwr	Static Pwr
0.25um	8.42E-11	1.38E-10	2.68E-10	1.13E-10	2.59E-04	1.81E-10
0.13um	3.61E-11	6.94E-11	1.02E-10	7.46E-11	6.66E-05	1.60E-08
65nm	2.59E-11	5.08E-11	8.13E-11	6.16E-11	2.30E-05	1.73E-08
32nm	2.10E-11	2.21E-11	5.85E-11	5.44E-11	1.26E-05	1.02E-08
16nm	2.63E-11	2.78E-11	8.05E-11	6.86E-11	2.06E-06	7.71E-09

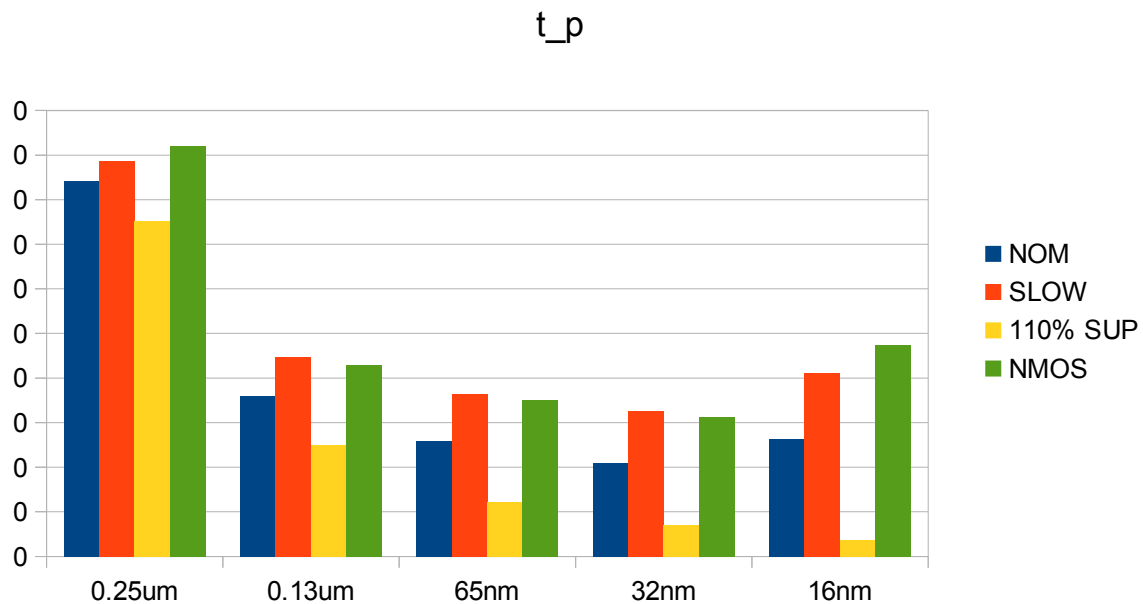
Slower Pmos Devices (by 50mV)						
	tphl	tplh	trise	tfall	Dynamic Pwr	Static Pwr
0.25um	8.86E-11	1.33E-10	2.64E-10	1.15E-10	2.63E-04	9.60E-11
0.13um	4.47E-11	6.04E-11	1.02E-10	7.47E-11	6.75E-05	6.43E-09
65nm	3.65E-11	4.00E-11	8.03E-11	6.17E-11	2.33E-05	7.12E-09
32nm	3.26E-11	1.05E-11	5.83E-11	5.48E-11	1.27E-05	3.04E-09
16nm	4.10E-11	1.23E-11	7.94E-11	6.89E-11	2.09E-06	2.25E-09

110% Supply Voltage and Faster Nmos & Pmos Devices (by 50mV)						
	tphl	tplh	trise	tfall	Dynamic Pwr	Static Pwr
0.25um	7.52E-11	1.38E-10	2.57E-10	1.11E-10	3.35E-04	5.33E-10
0.13um	2.49E-11	7.55E-11	9.84E-11	7.62E-11	8.95E-05	7.66E-08
65nm	1.23E-11	5.80E-11	7.72E-11	6.33E-11	3.24E-05	8.12E-08
32nm	7.04E-12	3.04E-11	5.71E-11	5.50E-11	1.98E-05	5.93E-08
16nm	3.68E-12	3.51E-11	7.50E-11	6.65E-11	3.20E-06	5.08E-08

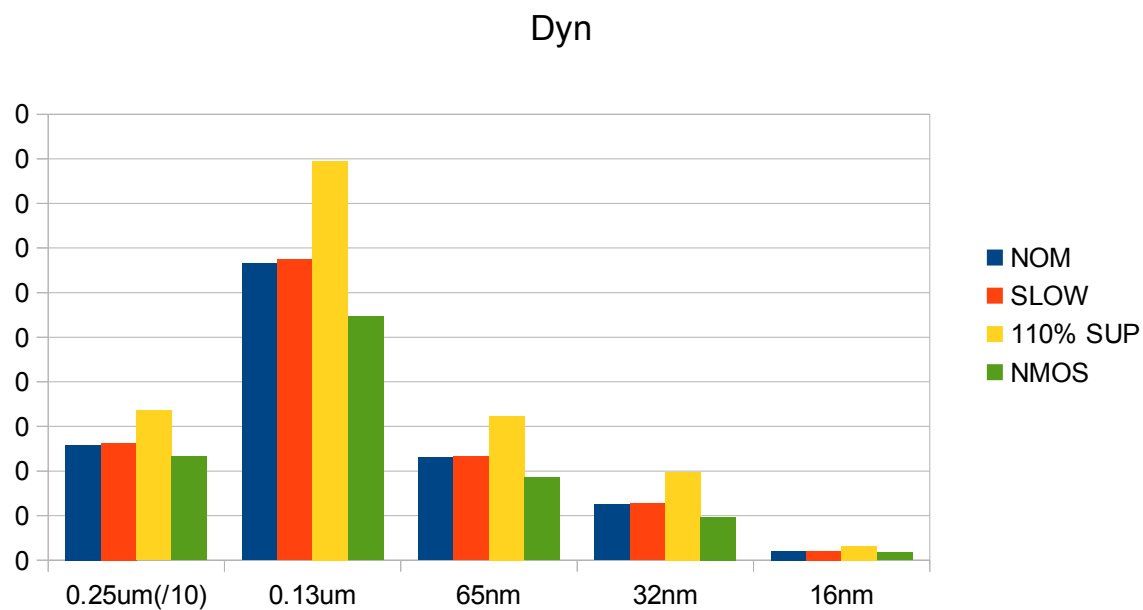
Nmos & Pmos Lengths Increased by 10%						
	tphl	tplh	trise	tfall	Dynamic Pwr	Static Pwr
0.25um	9.19E-11	1.56E-10	3.00E-10	1.25E-10	2.32E-04	1.82E-10
0.13um	4.29E-11	8.28E-11	1.20E-10	7.42E-11	5.47E-05	7.36E-09
65nm	3.51E-11	6.39E-11	9.26E-11	5.81E-11	1.86E-05	6.25E-09
32nm	3.12E-11	3.30E-11	5.85E-11	4.96E-11	9.67E-06	1.67E-09
16nm	4.74E-11	5.16E-11	8.07E-11	5.84E-11	1.73E-06	7.11E-10

4. The three plots of results.

The Dynamic power graph seems reasonable. Reduction in the process sizing should reduce the switching on off power of the transistors. The rise fall t_p delay decreasing with reduction in size, and the static power seemed to increase when the size was reduced. We think since Patrick said in class that smaller transistors leak about the same amount of current as larger ones, and it's a property of the materials used rather than the process.



:Note on the Dynamic power graph the 0.25 μ m values were divided by 10 to allow for better definition of the other process sizes.



:Note on the Leak graph the 0.25um values were multiplied by 10 to allow for better definition of the other process sizes.

