# Names

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**Take Home Midterm #2 and Final-Project#2: POWER CONSUMPTION , PROCESS MISMATCH, and SRAM Design**

**OUT: Feb. 18;**

**IN: Mar. 18 (complete report of Midterm-#2 and Final-Project)**

**DONE IN GROUPS!!!!**

**Optimal Power Consumption vs. Process Sensitivity/Mismatch**

**Problem #1: Energy-Delay Product for Scaled Vdd Technologies with NO Process Mismatch**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tplh | Tphl | Td(avg) | I(static) | Energy(static) | Energy(dynamic) | Energy(TOT)/computation |
| 0.25u(2.5V) |  |  |  |  |  |  |  |
| 2.5V |  |  |  |  |  |  |  |
| 1.0V |  |  |  |  |  |  |  |
| 0.6V |  |  |  |  |  |  |  |
| 0.5V |  |  |  |  |  |  |  |
| 0.3V |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| 65nm(1V) |  |  |  |  |  |  |  |
| 1.0V |  |  |  |  |  |  |  |
| 0.7V |  |  |  |  |  |  |  |
| 0.5V |  |  |  |  |  |  |  |
| 0.4V |  |  |  |  |  |  |  |
| 0.3V |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

1. PLOT: 1) DELAY vs. VDD for each process; 2) ENERGY/COMPUTATION vs. VDD for each process; 3) ENERGY\*DELAY Product vs. VDD for each process (EDP on Y-Axis; VDD and process node on X-Axis)

NOTE: ENERGY(TOT) is the total energy consumed (static AND dynamic) in any one clock period. This is equivalent to ENERGY consumed / computation. YOU NEED TO FIND STATIC ENERGY CORRECTLY, and also what the cycle time is.

**Problem #2: Energy-Delay Products for Scaled Vdd Technologies with WORST-CASE Process Mismatch**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tplh | Tphl | Td(avg) | I(static) | Energy(static) | Energy(dynamic) | Energy(TOT)/computation |
| 0.25u(2.5V) |  |  |  |  |  |  |  |
| 2.5V |  |  |  |  |  |  |  |
| 1.0V |  |  |  |  |  |  |  |
| 0.6V |  |  |  |  |  |  |  |
| 0.5V |  |  |  |  |  |  |  |
| 0.3V |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| 65nm(1V) |  |  |  |  |  |  |  |
| 1.0V |  |  |  |  |  |  |  |
| 0.7V |  |  |  |  |  |  |  |
| 0.5V |  |  |  |  |  |  |  |
| 0.4V |  |  |  |  |  |  |  |
| 0.3V |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

1. PLOT: 1) DELAY vs. process; 2) ENERGY(TOT) vs. process; 3) ENERGY(TOT)\*Delay Product vs. process (EDP on Y-Axis; process node on X-Axis) (SAME AS PROBLEM-#1)

**Problem 3: Qualitative Discussion (short answers)**

1. How does the delay vs. power dissipation scale as Vdd is lowered? At what point can we stop scaling the supply voltage Vdd? Is there a limit? (HINT: Look at the leakage)
2. Vdd scaling is a great way to reduce power consumption, if the increase in delay can be tolerated. However, what happens to the delay vary between: a) no process mismatch case; b) worst case process mismatch case
3. While energy/computation seems to be reducing with reduced VDD, another important metric is energy/computation \* delay (or, energy-delay product). How is Energy-Delay Product scaling? Are we seeing any benefit for low-VDD operation as we continue reducing VDD? Why or why not?

**Problem 4: 2-Page Skim Paper**

**1) Ultralow-voltage, minimum-energy CMOS**

<http://blaauw.eecs.umich.edu/getFile.php?id=247>

**2) Sub-threshold Sensor Network Processor**

http://blaauw.eecs.umich.edu/getFile.php?id=263

**3) Razor-I paper**

http://blaauw.eecs.umich.edu/getFile.php?id=25

Read the three papers above, and **write a 1-page synopsis**, summary of low-voltage, digital logic design. NOTE: I DO READ AND GRADE THESE CAREFULLY, TO DETERMINE UNDERSTANDING OF THIS MATERIAL. PLEASE DO WRITE WELL.

Synopsis

**Problem 4a: Design of a 16 x 16b 6T-SRAM in 0.25um CMOS**

GOAL: Design a 16-entry SRAM with word-size=16b. **NOTE: No layout is required for this design!**

Your design procedure should be similar to the Berkeley final project, except you do NOT need to finish the layout:

<http://bwrc.eecs.berkeley.edu/classes/icdesign/ee141_f08/Project/EE141-Proj1.pdf>

You need to build the following components to demonstrate this 16x16 SRAM:

1. 4:16 decoder for the one-hot word-select lines
2. 6T-SRAM bit cell (use Min-size inverters)
3. Column sensing amplifier (i.e. either opamp or offset-cancelled sense amplifier)
4. Please write-up your design using the 4-page IEEE format paper. There are examples on the class webpage.

NOTE: While you are NOT doing layout, you will need to estimate the parasitic loading of your long wiring loads. Do this by multiplying your total RC wire lengths, and use a PI-model to estimate the parasitic load your decoder and column lines will really see after layout. For example, you can use power-point to estimate this.

**In your final report, please estimate the leakage power, active power, maximum clock frequency, area, and noise margins for the SRAM cell.**

EXTRA CREDIT-1: Scale it to 32nm-CMOS, and show the changes in leakage power, active power, maximum clock frequency, area, and noise margins.

EXTRA CREDIT-2: Add two power gate to your entire 16bx16b SRAM:

a) PMOS power-gating switch, for leakage current reduction

Size this PMOS header to achieve less 10% reduction in total delay (compared with NO PMOS header). NOTE: No retention.

b) NMOS power-gate ‘drowsy’ switch

Saves leakage current by dropping the ‘virtual VDD’ node, while exhibiting retention.