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HW# 2
ECE 474

PART 4

1. Find the total area used by the alu. (report_area command)

   Using report_area it says that my designs total area is 3190.39230 um^2.

2. How many different types of cells (gates) were utilized : (report_hierarchy command)

AND2X1	saed90nm_typ
AND3X1	saed90nm_typ
AO22X1	saed90nm_typ
AO221X1	saed90nm_typ
INVX0	saed90nm_typ
MUX21X1	saed90nm_typ
MUX41X1	saed90nm_typ
NAND2X0	saed90nm_typ
NAND3X0	saed90nm_typ
NAND4X0	saed90nm_typ
NOR2X0	saed90nm_typ
OR2X1	saed90nm_typ
OR4X1	saed90nm_typ
XNOR2X1	saed90nm_typ
XOR2X1	saed90nm_typ
alu_DW01_addsub_0	
FADDX1	saed90nm_typ
XOR2X1	saed90nm_typ
XOR3X1	saed90nm_ty

3. Number of cells (gates). This will require using the report_area command as well as looking at the cell library databook. It is located at: /nfs/guille/a1/cadlibs/synop_lib/SAED_EDK90nm/Digital_Standard_Cell_Library/doc/databook. Its is called SAED Digital Standard Cell Library_Rev1_4_20. Its is a pdf file but has no .pdf on it. Search for the cell "NAND2X0" and record the area. (pg 34) Divide the total area reported by design_vision by this number to get the gate equivalent count.

   It says that the number of cells is 229. By looking at the Design Vision output.

4. The synthesis tool will most likely introduce a hierarchical block to your design because it recognized something in your design. What is the block and what does it do?

   In my design it looks like it recognized that part of my design was an add and subtract, so it added an alu_SW01_addSub_0 block, which acts as the adder er and sub tractor.

5. What style of implementation was chosen for this element? Hint: see report_hierarchy output

   It looks like a combinational logic implementation. It also created an alu addsub element. Which all was created in 90nm type.

```
alu
   AND2X1              saed90nm_typ
   AND3X1              saed90nm_typ
   AO22X1              saed90nm_typ
   AO221X1             saed90nm_typ
   INVX0               saed90nm_typ
   MUX21X1             saed90nm_typ
   MUX41X1             saed90nm_typ
   NAND2X0             saed90nm_typ
   NAND3X0             saed90nm_typ
   NAND4X0             saed90nm_typ
   NOR2X0              saed90nm_typ
   OR2X1               saed90nm_typ
   OR4X1               saed90nm_typ
   XNOR2X1             saed90nm_typ
   XOR2X1              saed90nm_typ
   alu_DW01_addsub_0
      FADDX1           saed90nm_typ
      XOR2X1           saed90nm_typ
      XOR3X1           saed90nm_typ
```

6. What was the maximum delay path through the alu and what were the beginning and endpoints for the max delay path?: (report_timing command)

   Using the report timing command design vision says that it takes 4.76ns for the max delay path.

   The main problem I had with hw2 was not haveing the .synopsys_dc.setup file. It had it named synopsys_sc.setup without the dot in front of it for some reason. Also I had to think about how to pass x to the Zero_out without using if statements.