## UBR Block Diagram

Note Title 5/4/2013 Shifted-speed counter divider-even counter\_sm restart restart Sensor -32 resct\_n reset\_n - reset\_n reset\_n count clk ->clk > clk restart-mem olh->clk shitt-register-sm restart mem fifo Lata-in data-out mem\_to\_fito\_sm fifo-empty shift-sir ROM - data fifo\_wr restart load-sv vestart ROM\_re reset - n reset-n reset y reset - n Rom-ce CIK\_MCM) fiford Dclk-mem clk - olk-mem Rom-addr CIR -> elk data-mem-to-tito fito-rd shift-register out reset n - reset - n CIK ->CIK