Snorkling clock

Variant: EUROPE

Block diagram:

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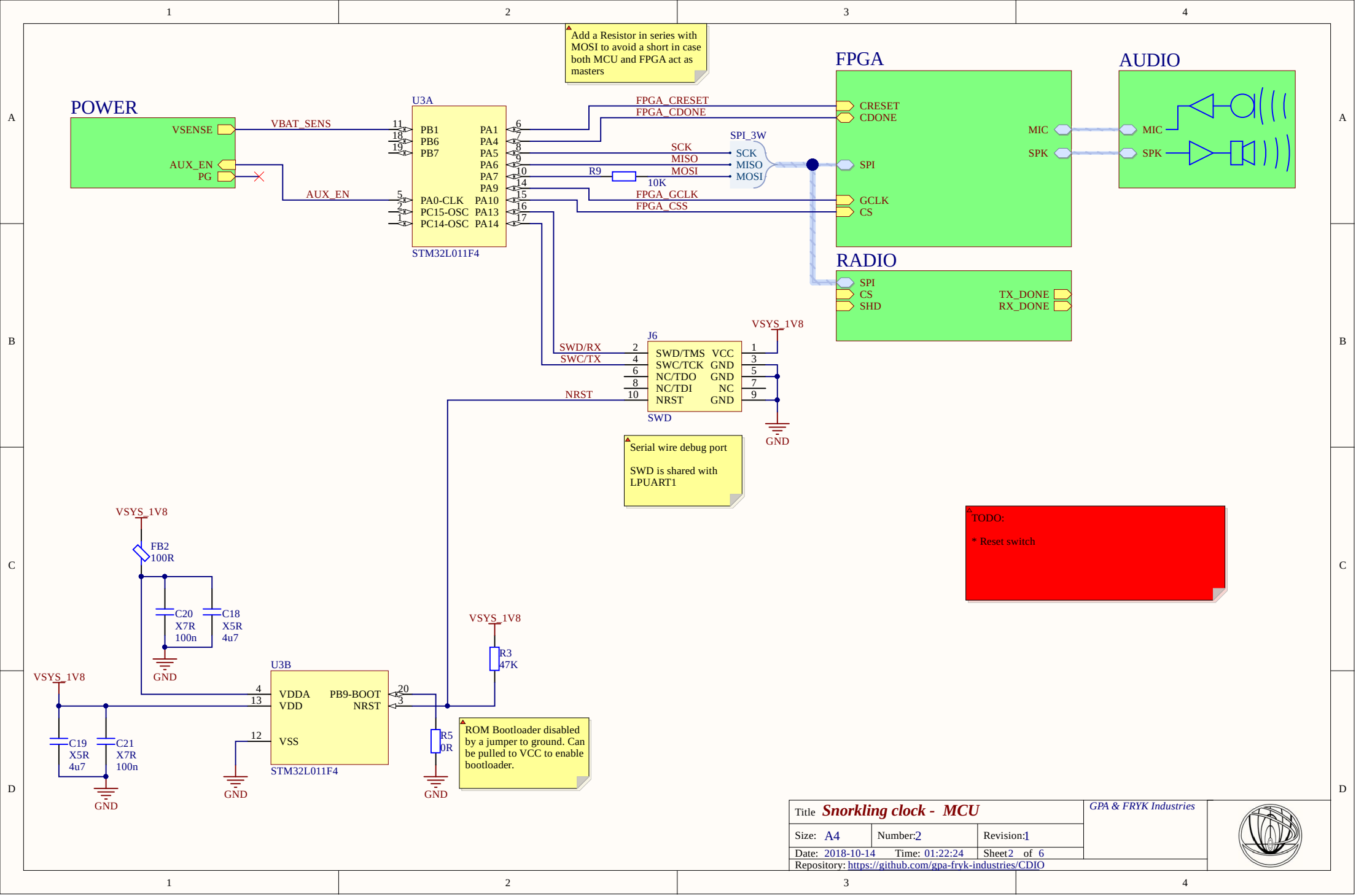
Introduction

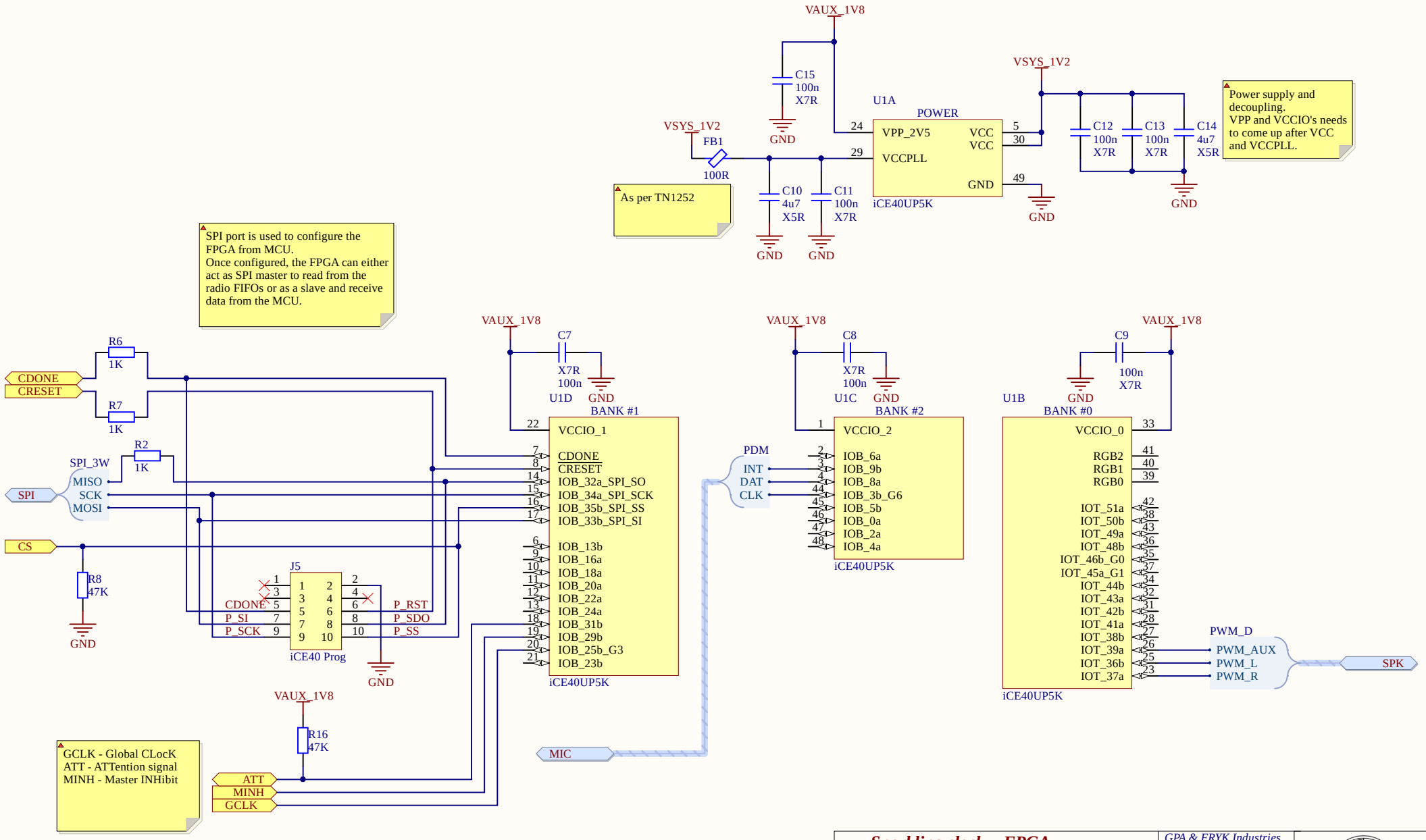
Text

Specifications

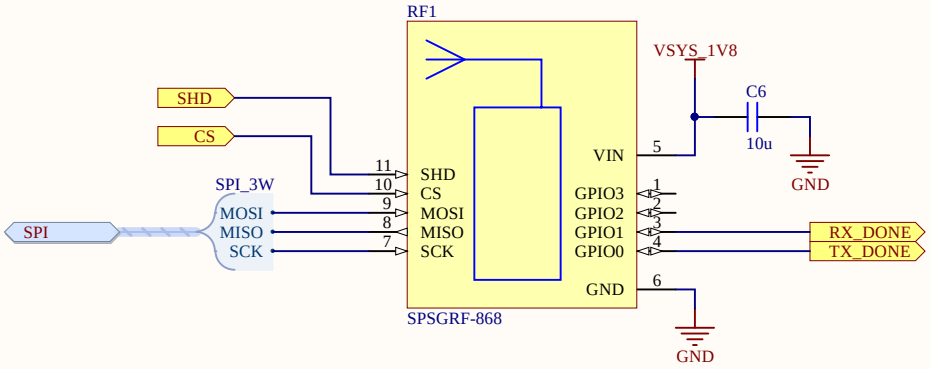
Text

Title	***Snorkling clock - Cover***		*GPA & FRYK Industries*
Size: A4	Number:1	Revision:1	
Date: 2018-10-14	Time: 01:22:24	Sheet 1 of 6	
Repository: https://github.com/gpa-fryk-industries/CDIO			

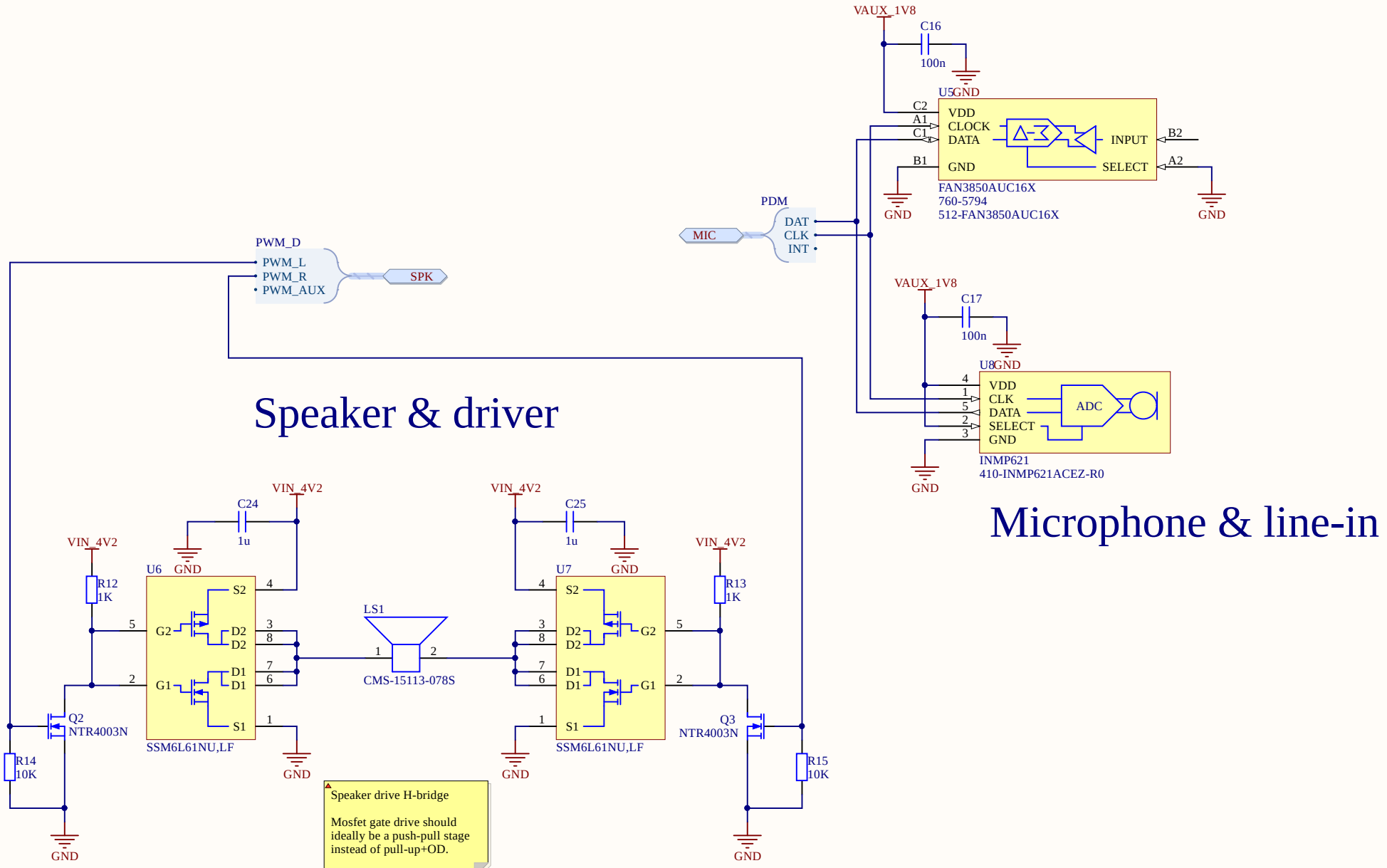

Add a Resistor in series with MOSI to avoid a short in case both MCU and FPGA act as masters
POWER
VSENSE
AUX_EN
PG
VBAT_SENS
AUX_EN
U3A
PB1
PB6
PB7
PA0-CLK
PC15-OSC
PC14-OSC
PA1
PA4
PA5
PA6
PA7
PA9
PA10
PA13
PA14
STM32L011F4
FPGA_CRESET
FPGA_CDONE
SCK
MISO
MOSI
R9
10K
SPI_3W
SCK
MISO
MOSI
FPGA_GCLK
FPGA_CSS
FPGA
CRESET
CDONE
SPI
GCLK
CS
MIC
SPK
AUDIO
MIC
SPK
RADIO
SPI
CS
SHD
TX_DONE
RX_DONE
VSYS_1V8
J6
SWD/RX
SWC/TX
NRST
SWD/TMS
SWC/TCK
NC/TDO
NC/TDI
NRST
VCC
GND
GND
GND
NC
GND
SWD
GND
Serial wire debug port
SWD is shared with LPUART1
TODO:
* Reset switch
VSYS_1V8
FB2
100R
C20
X7R
100n
C18
X5R
4u7
GND
VSYS_1V8
U3B
VDDA
VDD
VSS
PB9-BOOT
NRST
STM32L011F4
R3
47K
R5
0R
GND
GND
VSYS_1V8
C19
X5R
4u7
C21
X7R
100n
GND
ROM Bootloader disabled by a jumper to ground. Can be pulled to VCC to enable bootloader.
Title Snorkling clock - MCU
GPA & FRYK Industries
Size: A4
Number:2
Revision:1
Date: 2018-10-14
Time: 01:22:24
Sheet 2 of 6
Repository: https://github.com/gpa-fryk-industries/CDIO



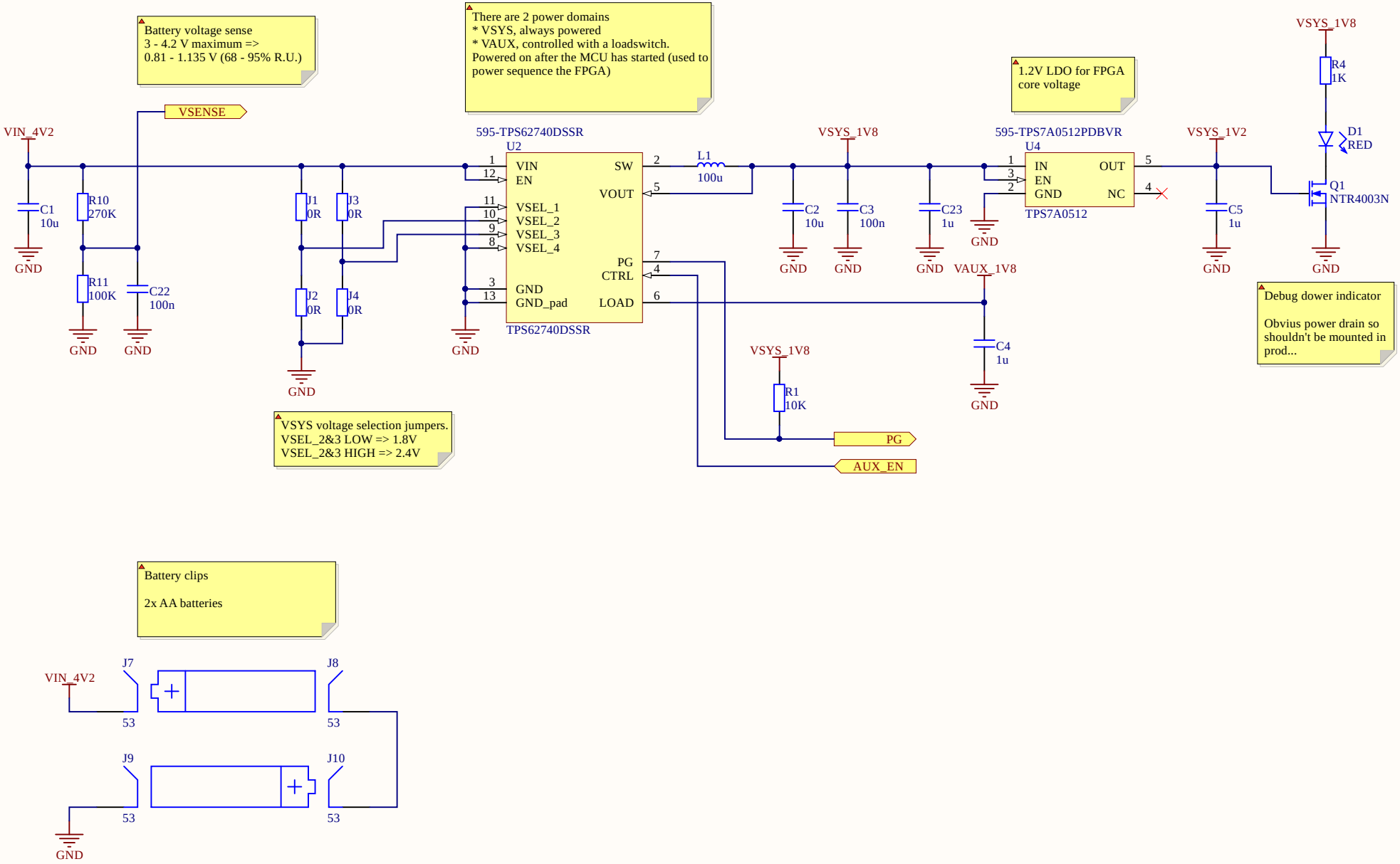
Title	***Snorkling clock - FPGA***	*GPA & FRYK Industries*
Size: A4	Number:3	Revision:1
Date: 2018-10-14	Time: 01:22:24	Sheet3 of 6
Repository: https://github.com/gpa-fryk-industries/CDIO		



Title	***Snorkling clock - Radio module***		*GPA & FRYK Industries*
Size: A4	Number:4	Revision:1	
Date: 2018-10-14	Time: 01:22:24	Sheet 4 of 6	
Repository: https://github.com/gpa-fryk-industries/CDIO			



Title	***Snorkling clock - Audio frontend***		*GPA & FRYK Industries*
Size: A4	Number:5	Revision:1	
Date: 2018-10-14	Time: 01:22:24	Sheet 5 of 6	
Repository: https://github.com/gpa-fryk-industries/CDIO			



Title	***Snorkling clock - Power supply***		*GPA & FRYK Industries*
Size: A4	Number:6	Revision:1	
Date: 2018-10-14	Time: 01:22:24	Sheet6 of 6	
Repository: https://github.com/gpa-fryk-industries/CDIO			