Snorkling clock

Variant: EUROPE

Block diagram:

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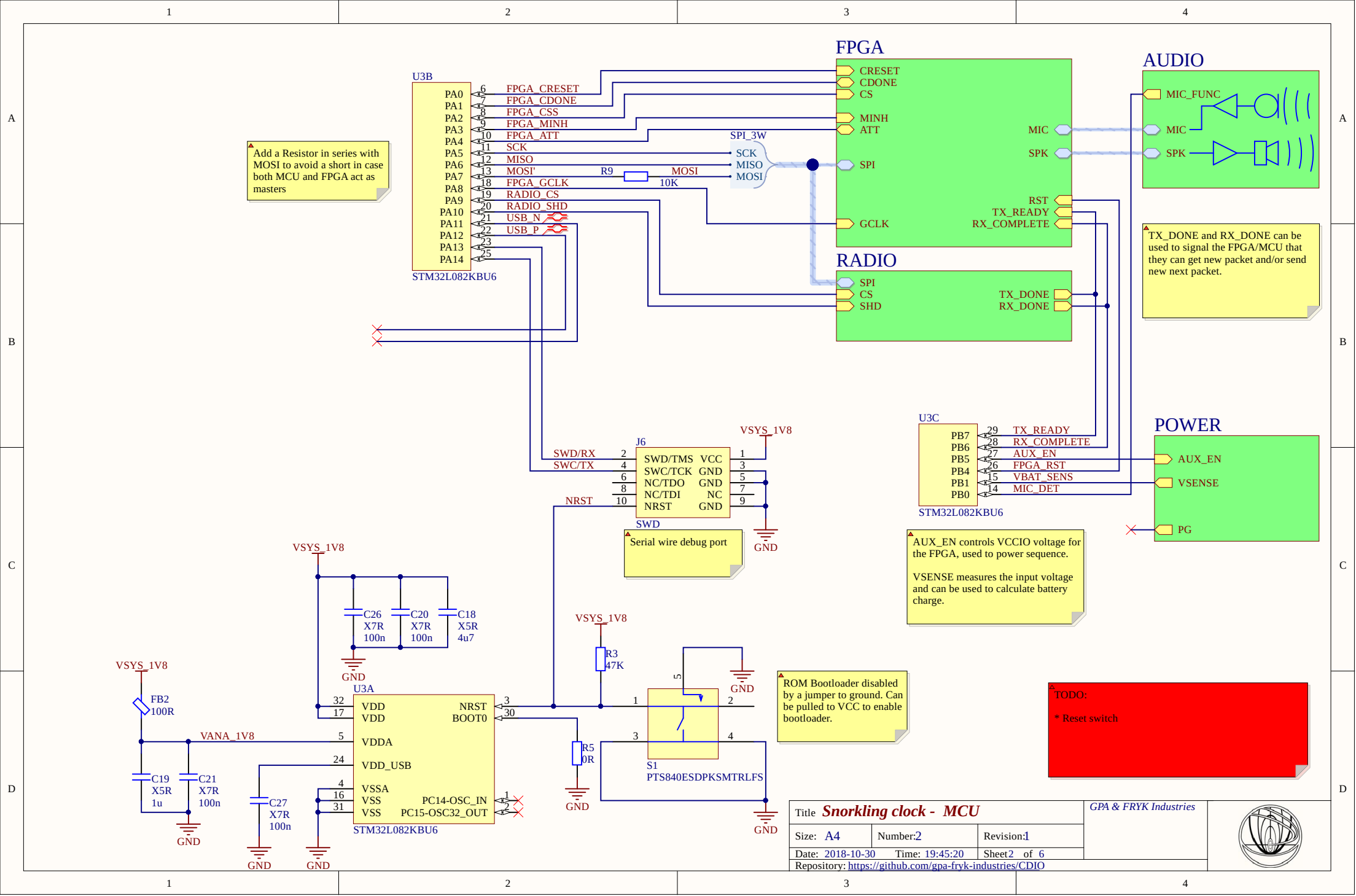
Introduction

Text

Specifications

Text

Title *Snorkling clock - Cover*			*GPA & FRYK Industries*
Size: A4	Number:1	Revision:1	
Date: 2018-10-30 Time: 19:45:20		Sheet 1 of 6	
Repository: https://github.com/gpa-fryk-industries/CDIO			


FPGA
AUDIO
RADIO
POWER
U3B
STM32L082KBU6
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11 PA12 PA13 PA14
FPGA_CRESET
FPGA_CDONE
FPGA_CSS
FPGA_MINH
FPGA_ATT
SCK
MISO
MOSI'
FPGA_GCLK
RADIO_CS
RADIO_SHD
USB_N
USB_P
SPI_3W
SCK
MISO
MOSI
R9
10K
CRESET
CDONE
CS
MINH
ATT
SPI
GCLK
MIC
SPK
RST
TX_READY
RX_COMPLETE
MIC_FUNC
MIC
SPK
SPI
CS
SHD
TX_DONE
RX_DONE
Add a Resistor in series with MOSI to avoid a short in case both MCU and FPGA act as masters
TX_DONE and RX_DONE can be used to signal the FPGA/MCU that they can get new packet and/or send new next packet.
U3C
STM32L082KBU6
PB7 PB6 PB5 PB4 PB1 PB0
TX_READY
RX_COMPLETE
AUX_EN
FPGA_RST
VBAT_SENS
MIC_DET
AUX_EN
VSENSE
PG
AUX_EN controls VCCIO voltage for the FPGA, used to power sequence.
VSENSE measures the input voltage and can be used to calculate battery charge.
J6
SWD
SWD/TMS SWC/TCK NC/TDO NC/TDI NRST
VCC GND GND GND NC GND
SWD/RX
SWC/TX
NRST
VSYS_1V8
GND
Serial wire debug port
U3A
STM32L082KBU6
VDD VDD VDDA VDD_USB VSSA VSS VSS
NRST BOOT0 PC14-OSC_IN PC15-OSC32_OUT
VSYS_1V8
VANA_1V8
FB2
100R
C26 X7R 100n
C20 X7R 100n
C18 X5R 4u7
C19 X5R 1u
C21 X7R 100n
C27 X7R 100n
R3
47K
R5
0R
S1
PTS840ESDPKSMTRLFS
ROM Bootloader disabled by a jumper to ground. Can be pulled to VCC to enable bootloader.
TODO:
* Reset switch
Title Snorkling clock - MCU
GPA & FRYK Industries
Size: A4
Number:2
Revision:1
Date: 2018-10-30
Time: 19:45:20
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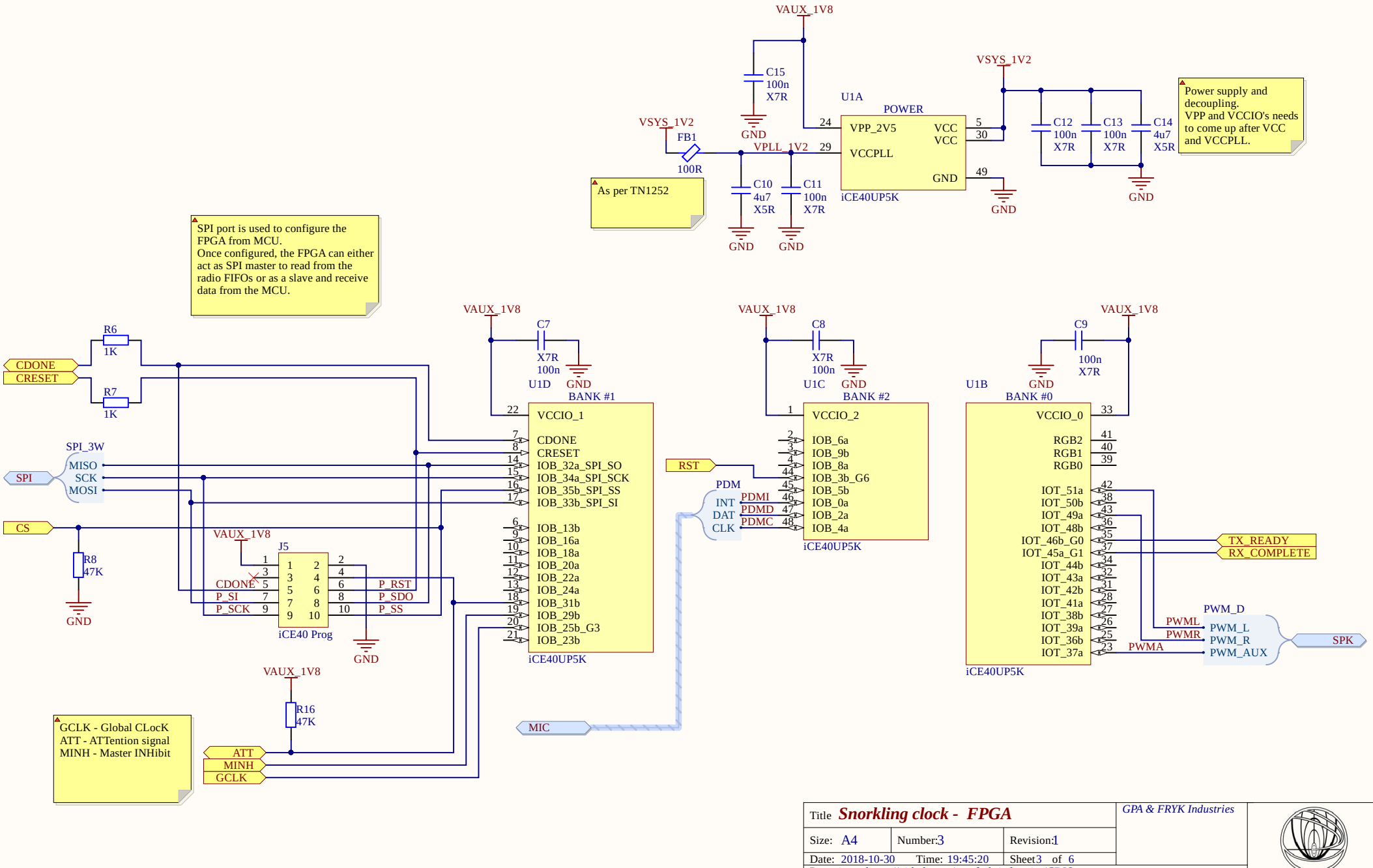
Repository: https://github.com/gpa-fryk-industries/CDIO



Title	***Snorkling clock - FPGA***		*GPA & FRYK Industries*
Size: A4	Number:3	Revision:1	
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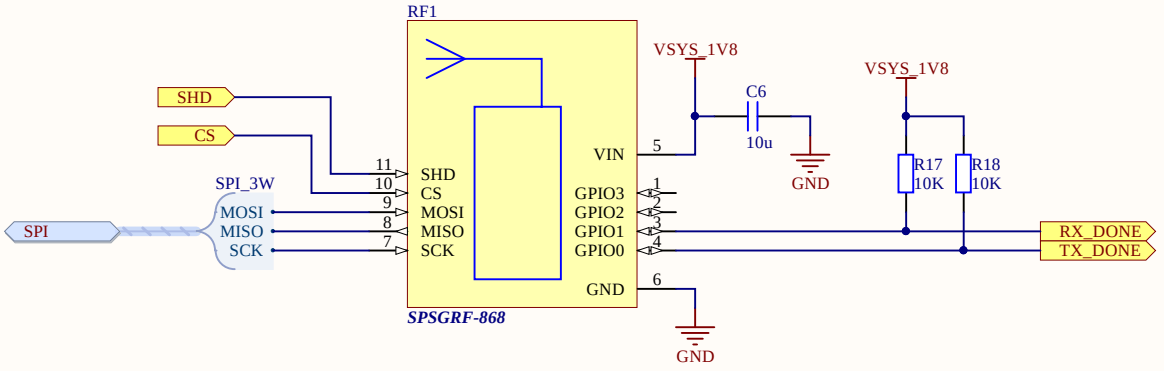
Repository: https://github.com/gpa-fryk-industries/CDIO			



Title	***Snorkling clock - Radio module***		*GPA & FRYK Industries*
Size: A4	Number:4	Revision:1	
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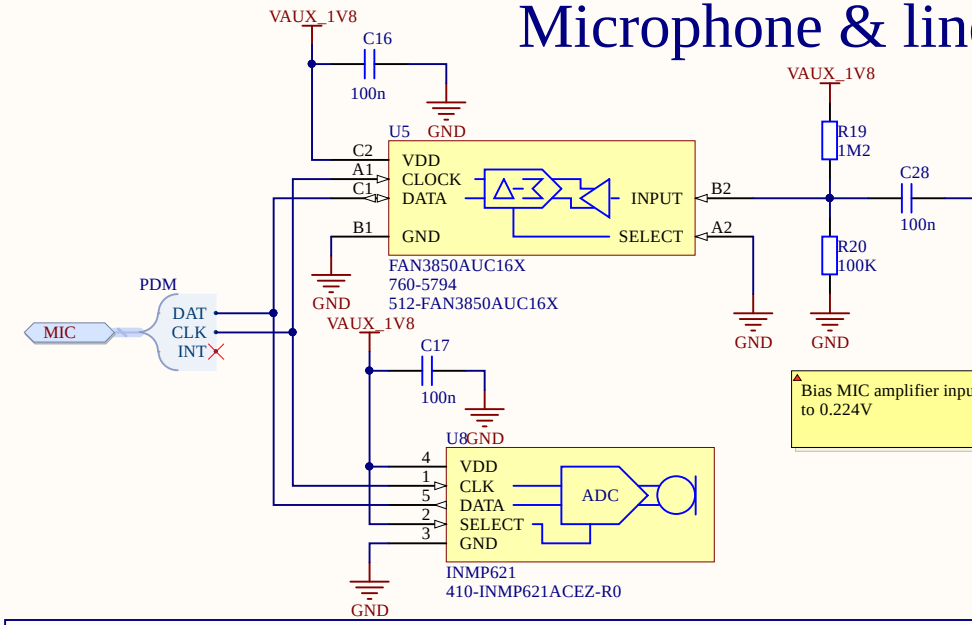
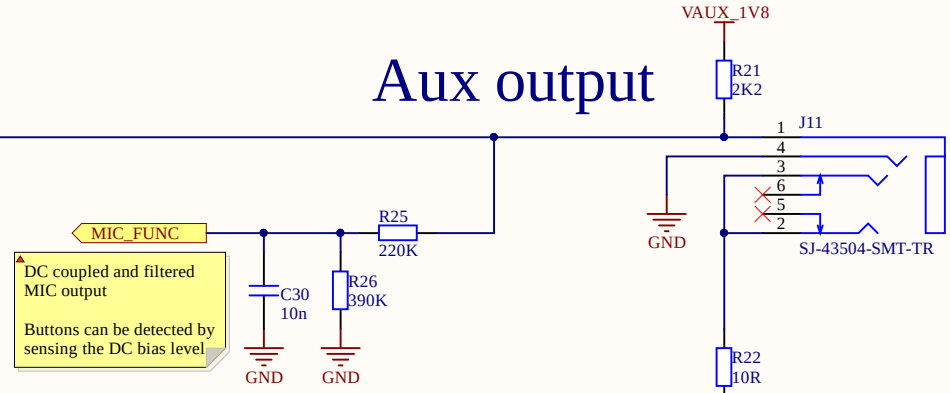
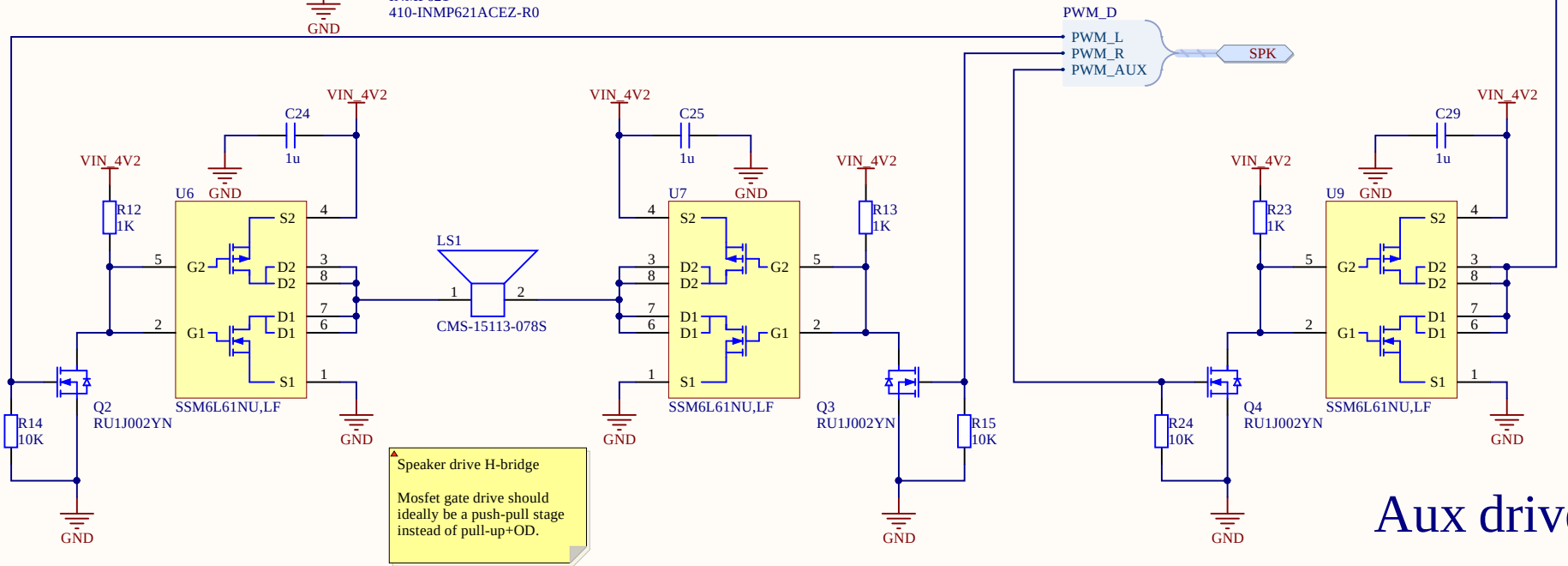
Repository: https://github.com/gpa-fryk-industries/CDIO			

Microphone & line-in



Aux output





Aux driver

Speaker & driver

Title	***Snorkling clock - Audio frontend***		*GPA & FRYK Industries*
Size: A4	Number:5	Revision:1	
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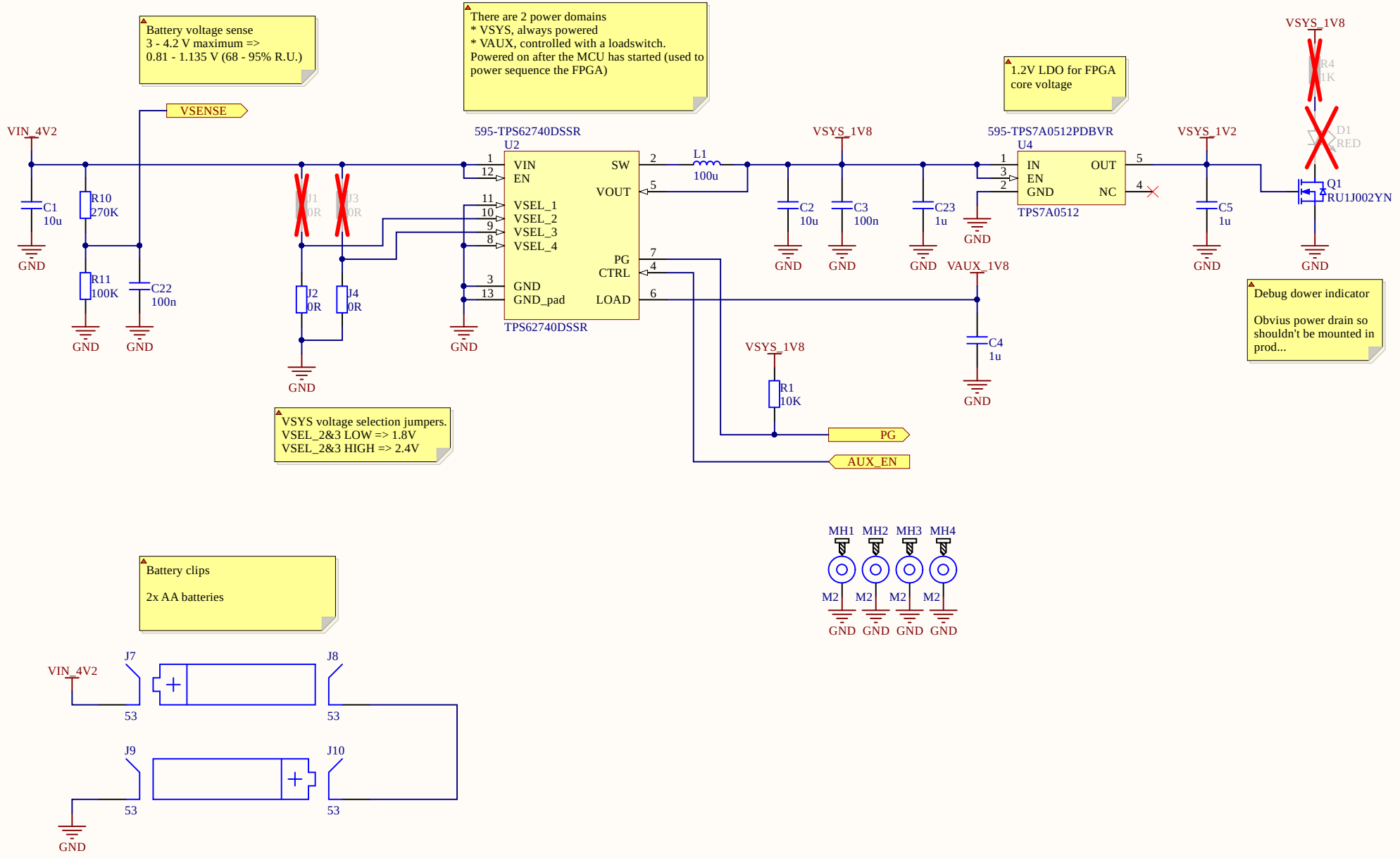
Repository: https://github.com/gpa-fryk-industries/CDIO			



Title	***Snorkling clock - Power supply***		*GPA & FRYK Industries*
Size: A4	Number:6	Revision:1	
Date: 2018-10-30	Time: 19:45:21	Sheet 6 of 6	
Repository: https://github.com/gpa-fryk-industries/CDIO			