



Block diagram:

# Snorkling clock

Variant: EUROPE

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## Introduction

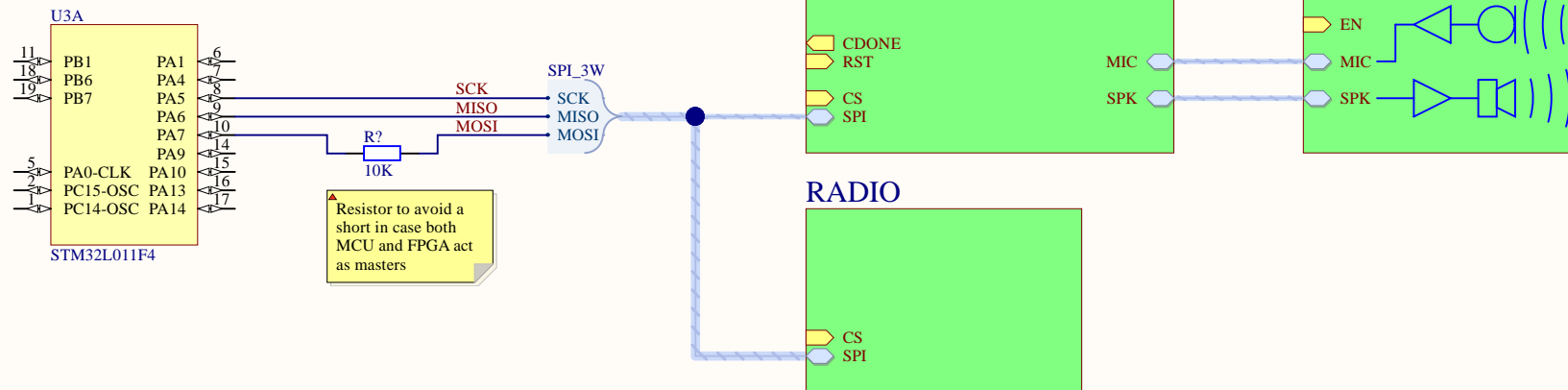
Text

## Specifications

Text

A

A

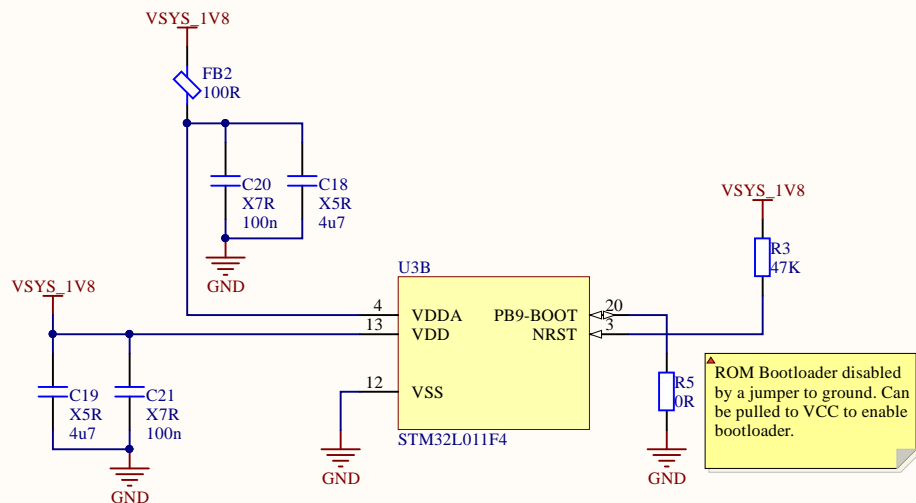


B

B

C

C



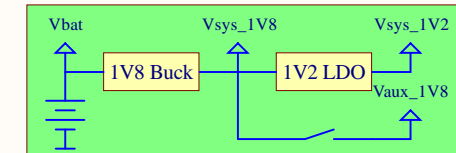
TODO:

- \* Check decoupling according to manufacturer
- \* MCO to fpga
- \* Reset switch

D

D

## POWER



Title **Snorkling clock - MCU**

GPA & FRYK Industries

Size: **A4**

Number: **2**

Revision: **1**

Date: **2018-10-09**

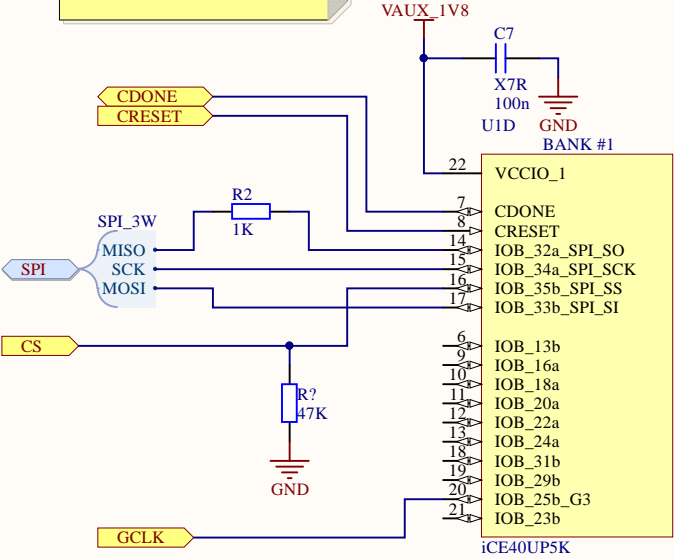
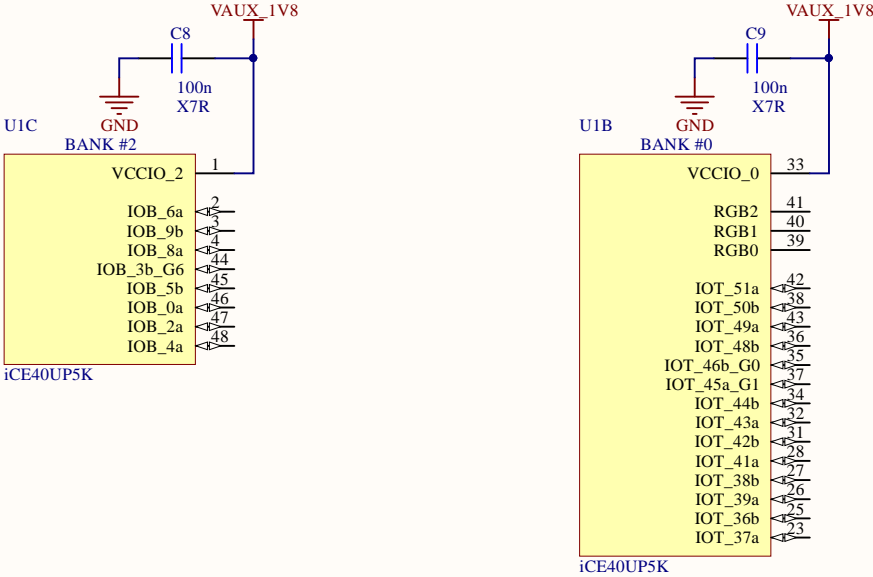
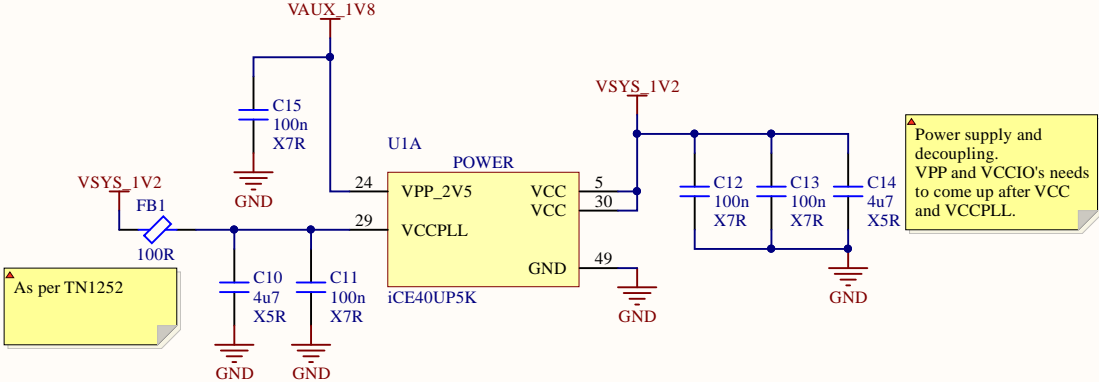
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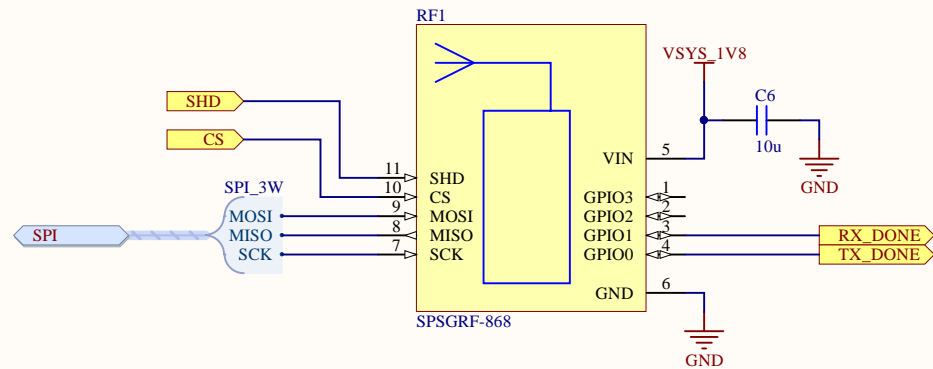
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Repository: <https://github.com/gpa-fryk-industries/CDIO>



▲ SPI port is used to configure the FPGA from MCU. Once configured, the FPGA can either act as SPI master to read from the radio FIFOs or as a slave and receive data from the MCU.





Title ***Snorkling clock - Radio module***

GPA & FRYK Industries

Size: **A4**

Number: **4**

Revision: **1**

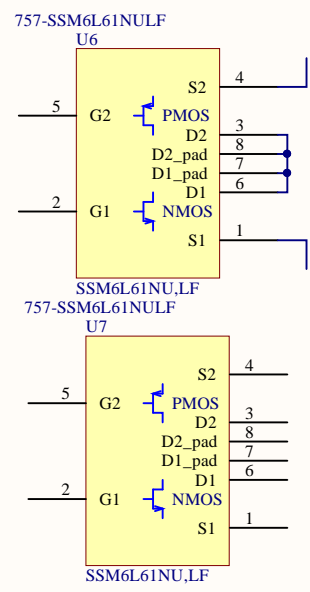
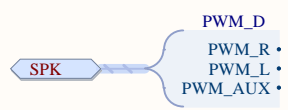
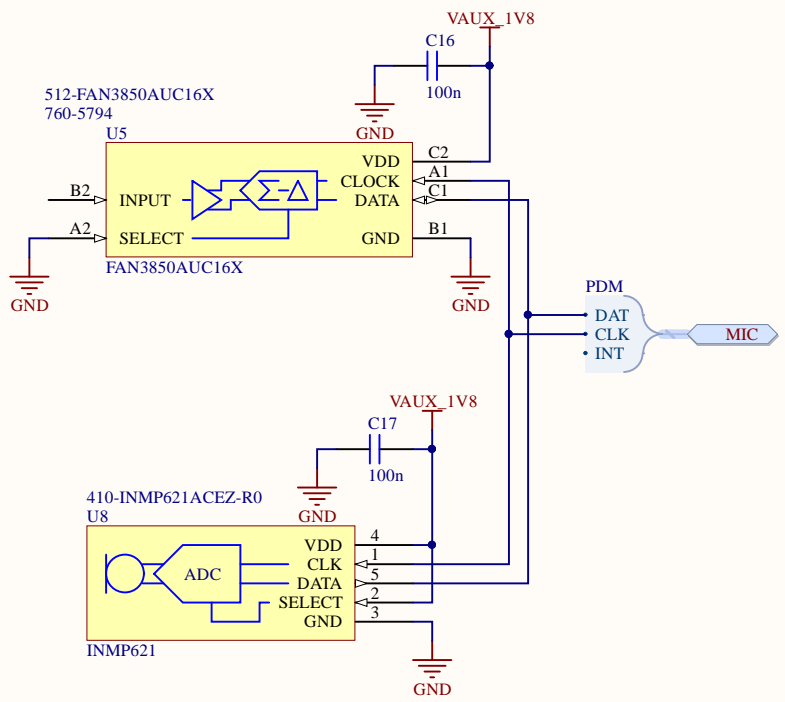
Date: **2018-10-09**

Time: **18:29:58**

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Repository: <https://github.com/gpa-fryk-industries/CDIO>





Battery voltage sense  
3 - 4.2 V maximum =>  
0.70 - 0.98 V (58 - 81% R.U.)

There is 2 power domains  
\* VSYS, always powered  
\* VAUX, controlled with a loadswitch.  
Powered on after the MCU has started (used to  
power sequence the FPGA)

1.2V LDO for FPGA  
core voltage

VSYS voltage selection jumpers.  
VSEL\_2&3 LOW => 1.8V  
VSEL\_2&3 HIGH => 2.4V

TODO:  
\* Check decoupling according to manufacturer  
\* UVLO?

