Snorkling clock

Variant: EUROPE

Block diagram:

Table of content

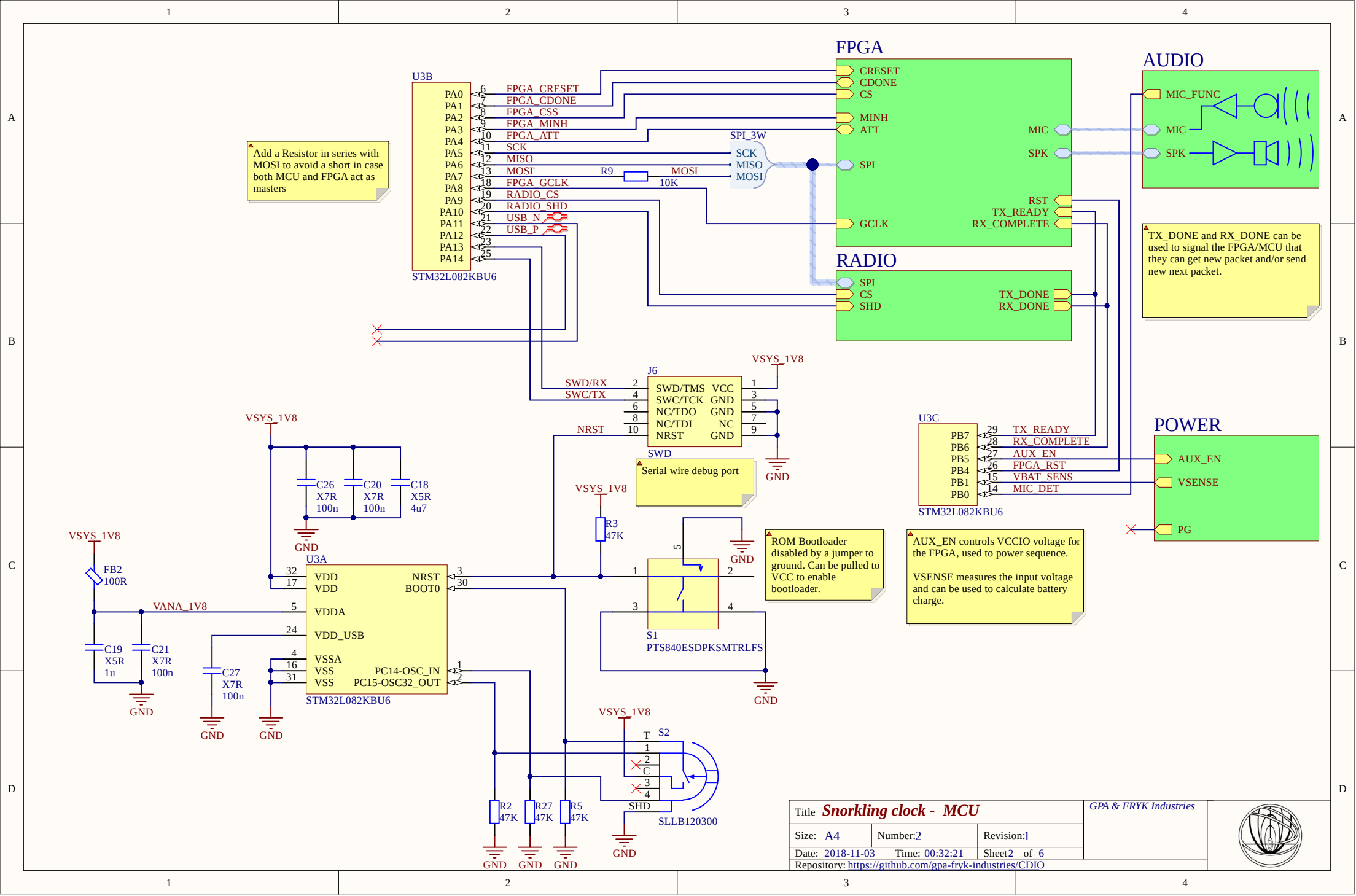
Introduction

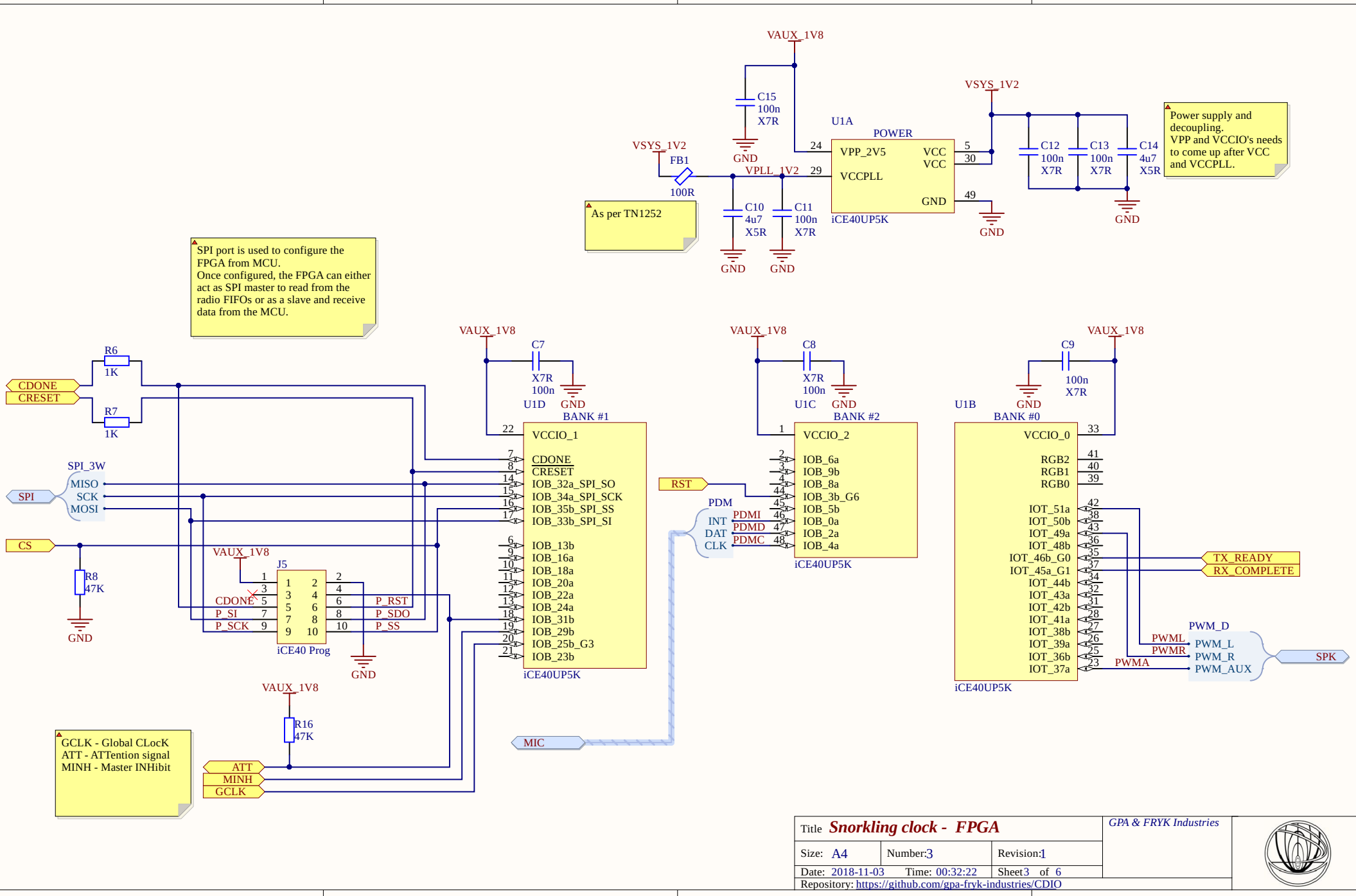
Text

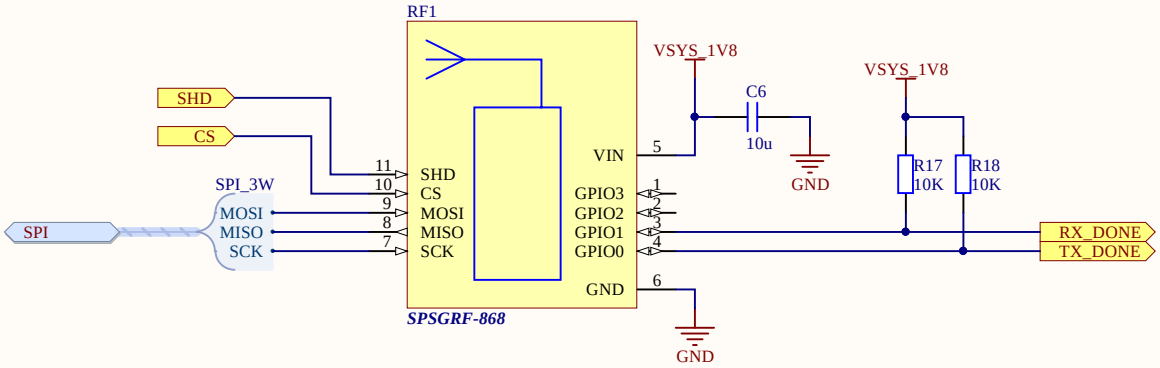
Specifications

Text

Title *Snorkling clock - Cover*			*GPA & FRYK Industries*
Size: A4	Number:1	Revision:1	
Date: 2018-11-03 Time: 00:32:21		Sheet 1 of 6	
Repository: https://github.com/gpa-fryk-industries/CDIO			

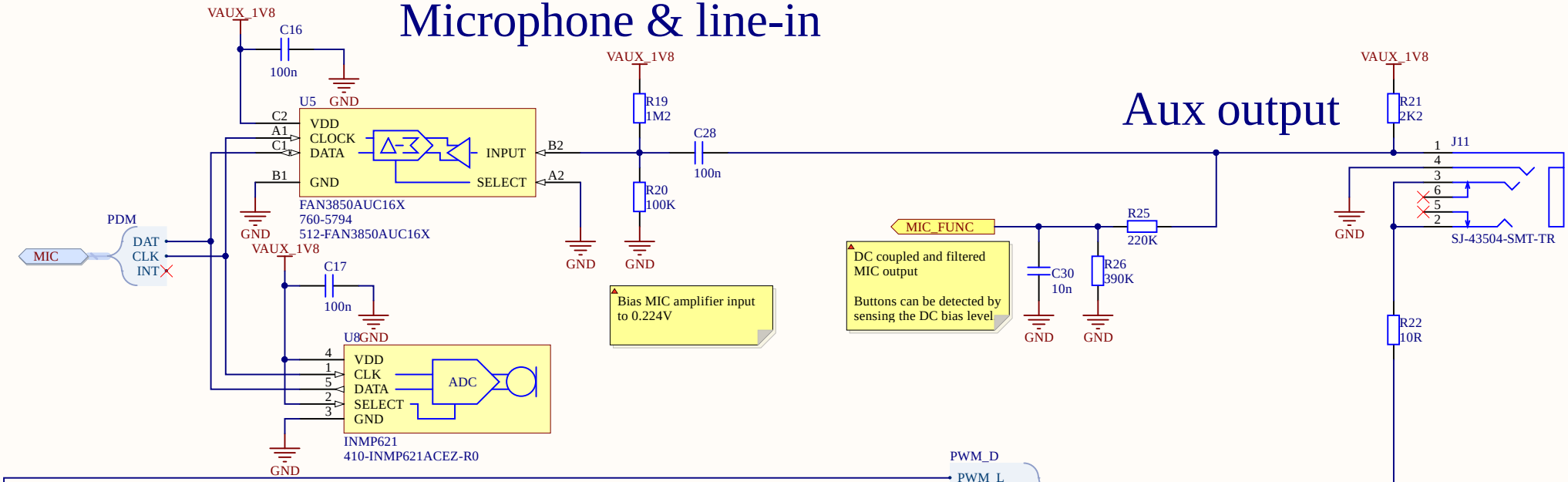

FPGA
AUDIO
RADIO
POWER
U3B
STM32L082KBU6
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11 PA12 PA13 PA14
FPGA_CRESET
FPGA_CDONE
FPGA_CSS
FPGA_MINH
FPGA_ATT
SCK
MISO
MOSI'
FPGA_GCLK
RADIO_CS
RADIO_SHD
USB_N
USB_P
Add a Resistor in series with MOSI to avoid a short in case both MCU and FPGA act as masters
R9
10K
MOSI
SPI_3W
SCK
MISO
MOSI
CRESET
CDONE
CS
MINH
ATT
SPI
GCLK
MIC
SPK
RST
TX_READY
RX_COMPLETE
MIC_FUNC
MIC
SPK
TX_DONE and RX_DONE can be used to signal the FPGA/MCU that they can get new packet and/or send new next packet.
SPI
CS
SHD
TX_DONE
RX_DONE
J6
SWD/TMS SWC/TCK NC/TDO NC/TDI NRST
VCC GND GND NC GND
SWD/RX
SWC/TX
NRST
SWD
Serial wire debug port
VSYS_1V8
GND
U3C
STM32L082KBU6
PB7 PB6 PB5 PB4 PB1 PB0
TX_READY
RX_COMPLETE
AUX_EN
FPGA_RST
VBAT_SENS
MIC_DET
AUX_EN
VSENSE
PG
C26 X7R 100n
C20 X7R 100n
C18 X5R 4u7
R3 47K
ROM Bootloader disabled by a jumper to ground. Can be pulled to VCC to enable bootloader.
AUX_EN controls VCCIO voltage for the FPGA, used to power sequence.
VSENSE measures the input voltage and can be used to calculate battery charge.
FB2 100R
VANA_1V8
C19 X5R 1u
C21 X7R 100n
C27 X7R 100n
U3A
VDD VDD VDDA VDD_USB VSSA VSS VSS
NRST BOOT0 PC14-OSC_IN PC15-OSC32_OUT
STM32L082KBU6
S1
PTS840ESDPKSMTRLFS
S2
SLLB120300
T C SHD
R2 47K
R27 47K
R5 47K
Title Snorkling clock - MCU
GPA & FRYK Industries
Size: A4
Number:2
Revision:1
Date: 2018-11-03
Time: 00:32:21
Sheet 2 of 6
Repository: https://github.com/gpa-fryk-industries/CDIO


VAUX_1V8
C15
100n
X7R
GND
VSYS_1V2
FB1
100R
VPLL_1V2
C10
4u7
X5R
C11
100n
X7R
As per TN1252
U1A
POWER
VPP_2V5
VCCPLL
VCC
VCC
GND
24
29
5
30
49
iCE40UP5K
VSYS_1V2
C12
100n
X7R
C13
100n
X7R
C14
4u7
X5R
Power supply and decoupling.
VPP and VCCIO's needs to come up after VCC and VCCPLL.
SPI port is used to configure the FPGA from MCU.
Once configured, the FPGA can either act as SPI master to read from the radio FIFOs or as a slave and receive data from the MCU.
R6
1K
R7
1K
CDONE
CRESET
SPI_3W
SPI
MISO
SCK
MOSI
CS
R8
47K
VAUX_1V8
C7
X7R
100n
U1D
BANK #1
VCCIO_1
CDONE
CRESET
IOB_32a_SPI_SO
IOB_34a_SPI_SCK
IOB_35b_SPI_SS
IOB_33b_SPI_SI
IOB_13b
IOB_16a
IOB_18a
IOB_20a
IOB_22a
IOB_24a
IOB_31b
IOB_29b
IOB_25b_G3
IOB_23b
iCE40UP5K
J5
iCE40 Prog
P_RST
P_SDO
P_SS
P_SI
P_SCK
VAUX_1V8
C8
X7R
100n
U1C
BANK #2
VCCIO_2
IOB_6a
IOB_9b
IOB_8a
IOB_3b_G6
IOB_5b
IOB_0a
IOB_2a
IOB_4a
iCE40UP5K
RST
PDM
INT
DAT
CLK
PDMI
PDMD
PDMC
VAUX_1V8
C9
100n
X7R
U1B
BANK #0
VCCIO_0
RGB2
RGB1
RGB0
IOT_51a
IOT_50b
IOT_49a
IOT_48b
IOT_46b_G0
IOT_45a_G1
IOT_44b
IOT_43a
IOT_42b
IOT_41a
IOT_38b
IOT_39a
IOT_36b
IOT_37a
iCE40UP5K
TX_READY
RX_COMPLETE
PWM_D
PWML
PWMR
PWMA
PWM_L
PWM_R
PWM_AUX
SPK
VAUX_1V8
R16
47K
GCLK - Global CLocK
ATT - ATTention signal
MINH - Master INHibit
ATT
MINH
GCLK
MIC
Title Snorkling clock - FPGA
GPA & FRYK Industries
Size: A4
Number:3
Revision:1
Date: 2018-11-03
Time: 00:32:22
Sheet3 of 6
Repository: https://github.com/gpa-fryk-industries/CDIO

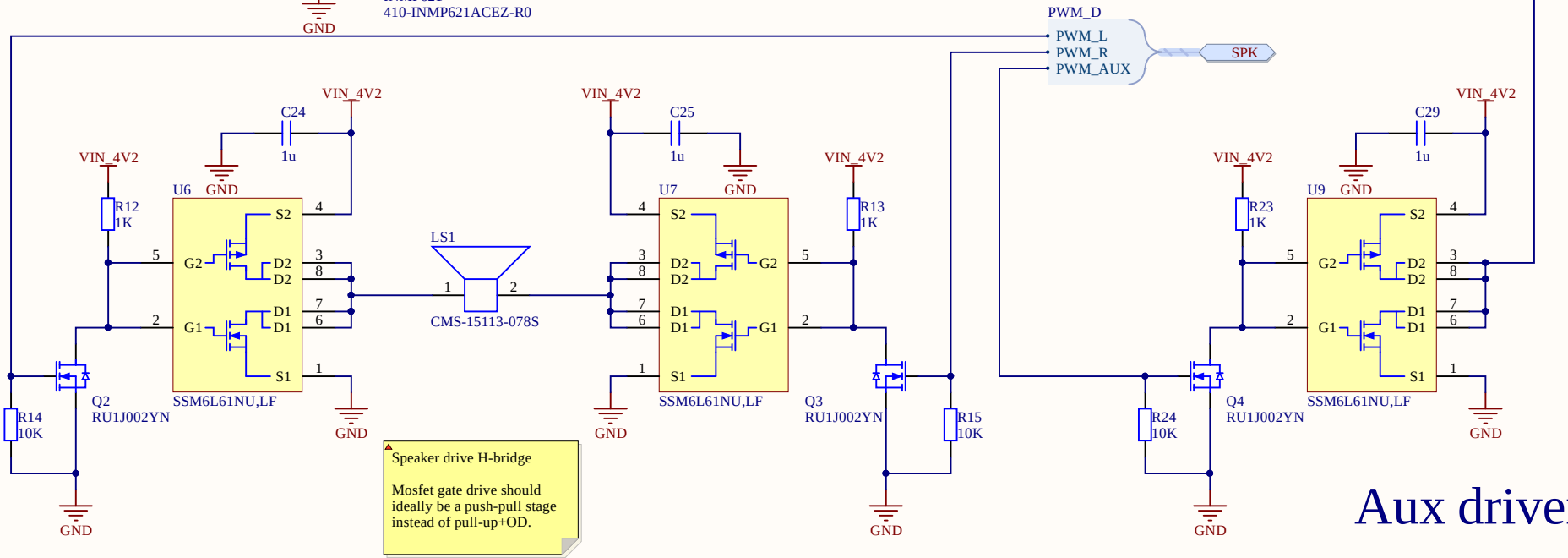


Title	***Snorkling clock - Radio module***		*GPA & FRYK Industries*
Size: A4	Number:4	Revision:1	
Date: 2018-11-03	Time: 00:32:22	Sheet 4 of 6	
Repository: https://github.com/gpa-fryk-industries/CDIO			

Microphone & line-in



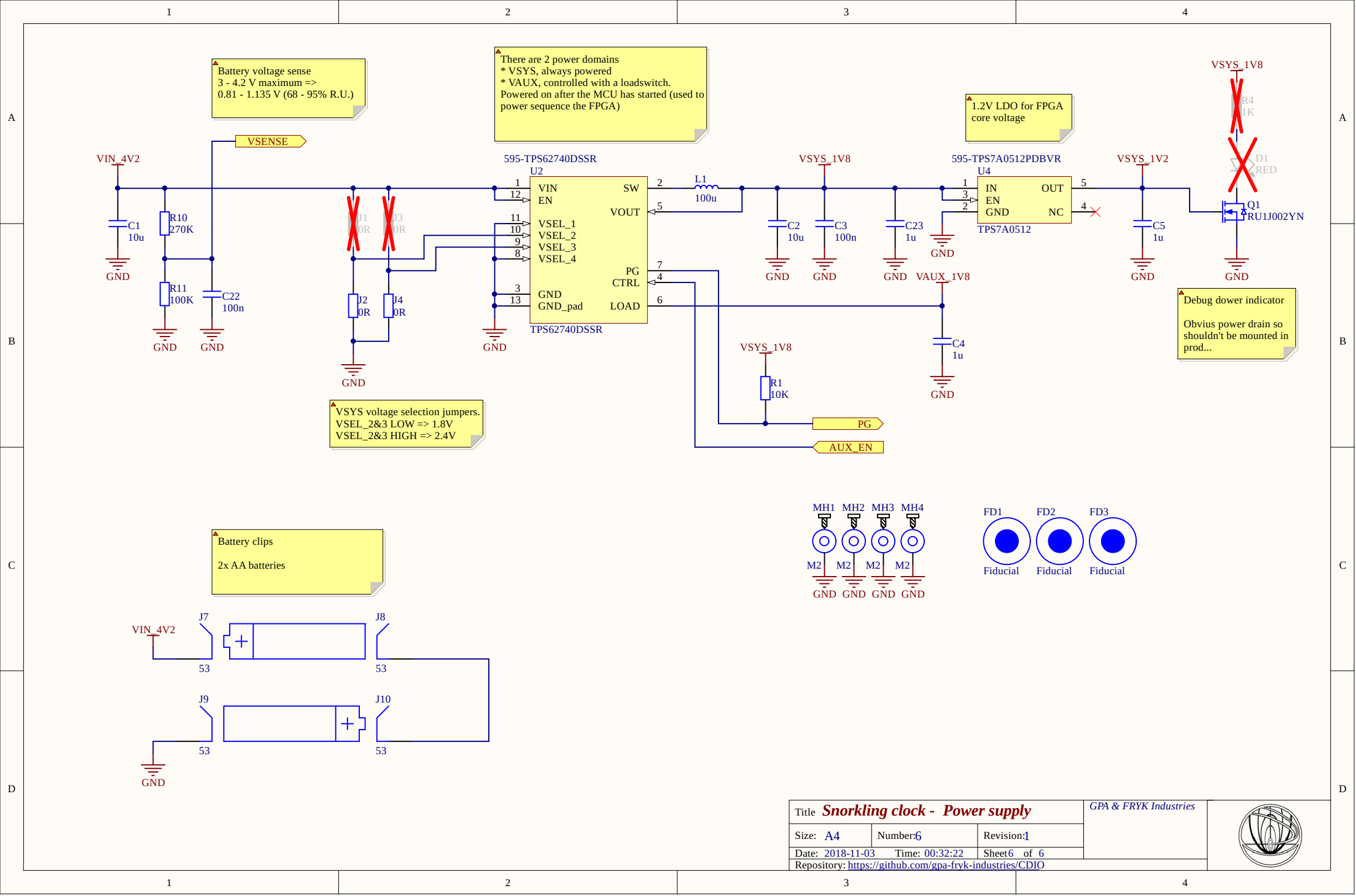
Aux output



Aux driver

Speaker & driver

Title	***Snorkling clock - Audio frontend***		*GPA & FRYK Industries*
Size: A4	Number:5	Revision:1	
Date: 2018-11-03	Time: 00:32:22	Sheet5 of 6	
Repository: https://github.com/gpa-fryk-industries/CDIO			



Title	***Snorkling clock - Power supply***		*GPA & FRYK Industries*
Size: A4	Number:6	Revision:1	
Date: 2018-11-03	Time: 00:32:22	Sheet 6 of 6	
Repository: https://github.com/gpa-fryk-industries/CDIO			