ASPIC details

Control signals (CMOS) for ASPIC:

- n_SS : Chip Select or Slave Select
- SCLK
- MOSI
- MISO

} SPI pins

- NRESET : I think this should stay go high when powering on the ASPIC and stay high for the rest of the operation
- NAP : Sleep mode, reduces the power consumption of the chip and I assume that it does not operate rather can be powered on quickly again. I believe we want it low the whole time.

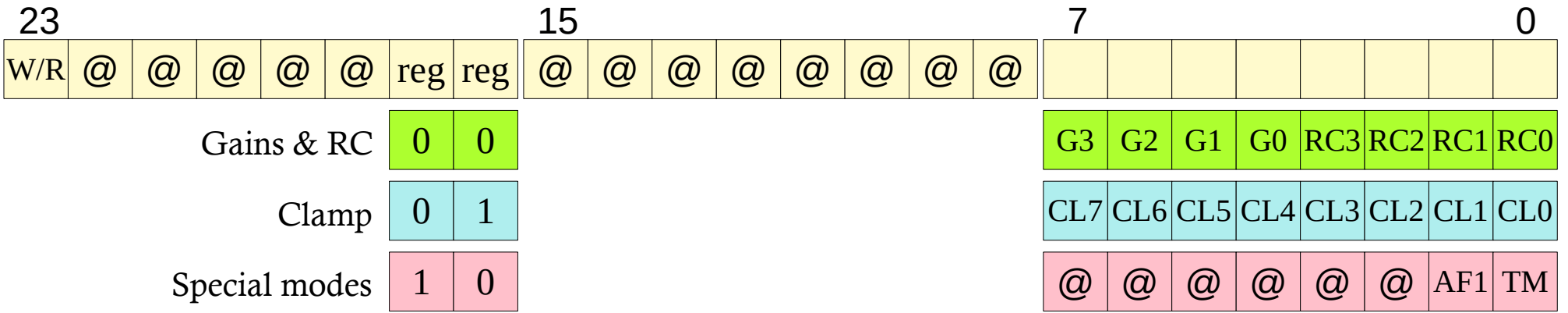
ASPIC details

The ASPIC is programmed with normal SPI communication. The sent message must always be 24-bit, but there are 3 different messages to be sent. The first bit (#23) defines the READ/WRITE action. The bits from 22 to 16 define the register address but there are only 3 registers. The bits with the @ should stay fixed. Probably 0 but it needs to be tested.

Then the bits from 15 to 0 have the data value. However, the first 8 ones should stay fixed (same as for bits 22 to 16) and especially for the special modes register only the last two get some value.

So, when powering on ASPIC one needs to program all 3 registers. Then, one can change only the register of interest.

When one wants to read the register, they should send the first 8 bits respectively (with MOSI) and then the MISO will return 16 bits with the information of the register.



ASPIC details

- Gains & RC: the programmable gain varies from 1.4 to 6.6. the programmable RC varies from 250ns to 4µs. I suspect that the minimum values come when all 4 bits are low and the max when they are high, but needs to be tested.
- Clamp: the input of the first amplifier wan be clamped to the reference, allowing for individual channel disactivation. Claire has commented that we might still be able to see some amplitude of the input signal. I do not know at which state is the channel active or not, I would say that when low the clamp is open and so the channel is active → to be tested.
- Special modes: AF1 should set the absolute gain of the amplifier equal to 1; TM is the transparent mode.