GURU PRASAD PAPANNA

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OBJECTIVE

Seeking an internship opportunity in the Physical Design domain, commencing June 2024.

EDUCATION

Masters, Electrical and Computer Engineering **GPA-3.62/4**

Portland State University, Portland, Oregon, USA (2023 Sept – 2025 June)

Courses (By June 2024) – Physical Design of Digital Integrated Circuits, Digital Integrated Circuit Design I, Digital Integrated Circuit Design II, Microprocessors System Design, ASIC Modelling and Synthesis, High-Performance Digital Systems.

Bachelor of Engineering, Electronics and Communication **GPA-3.5/4**

SJB Institute of Technology, Karnataka, India (Affiliated to Visvesvaraya TechnologicalUniversity)

TECHNICAL SKILLS & ABILITIES

- **Computer-based tools:** Extensive experience with Cadence –Innovus, Genus, Virtuoso, Voltus, Synopsys - ICC2.
- **Scripting knowledge:** Proficient in TCL, Perl and Shell
- **Programming Languages:** Verilog, System Verilog, C.
- **Operating Systems:** Comfortable with Windows, Linux
- **Certification Course:** Advanced Diploma in ASIC Physical Design **March 2021- Aug'2021**

PROFESSIONAL EXPERIENCE

Associate Engineer | SeviTech Systems Pvt. Ltd | India, Bangalore **Sep'2021 – Jan'2023**

Project 1: Texas Instruments - Physical Design of 7 individual blocks in an audio chip –130nm

- Hands-on experience in handling the Athena flow used by Texas Instruments for the Physical Design flow.
- Conducted the synthesis of Verilog files, generation of the Gate Level Netlist. Navigated the entire PD flow, from floor planning to the intricacies of PnR.
- Effectively surmounted every challenge encountered at each stage of PD, ensuring the fulfillment of blocks requirement criteria including timing and Physical Verification.

Project 2: Physical Design of a single block in an audio chip - 40nm

- Floor planning of a block housing 34 macros, secured the contiguous core area while minimizing congestion, optimizing the overall layout.
- Proficiently executed power planning, placement, clock tree synthesis (CTS), and routing. Iterated through the PD flow multiple times to craft a DRC-compliant design.

Programmer Analyst| Cognizant Technology Solutions | India, Bangalore **Dec'2019-March2021**

- Served as a dedicated SAP ABAP Consultant. Spearheaded all system refresh activities, SAP note corrections, addressing job failures, ABAP dumps, and orchestrating SPAU and SPDD activities within the project.

TECHNICAL PROJECTS **Sep' 2023- Dec'2023**

Simulation of the scheduler portion of a 16GB PC5-38400 DIMM memory controller

- Simulation of the scheduler portion of a memory controller capable serving a 12-core 4.8 GHz processor employing a single 16GB PC5-38400 DIMM in System Verilog.
- The DIMM is constructed with memory chips organized as x8 devices with a 1KB page size and 40-39-39-76 timing.
- Created a simulation loop where the DRAM cycles were kept in count to take in a line from input trace file, convert it into DRAM command and push it onto a queue and right after satisfying the timing constraints or when a pre-charge command was issued, the command was out of the queue and sent as a DRAM command onto dram.txt file.