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Energy Efficiency in High Throughput Computing

Tools, techniques and experiments

MOTIVATION: HTC, CERN & energy consumption: Higgs boson and the future

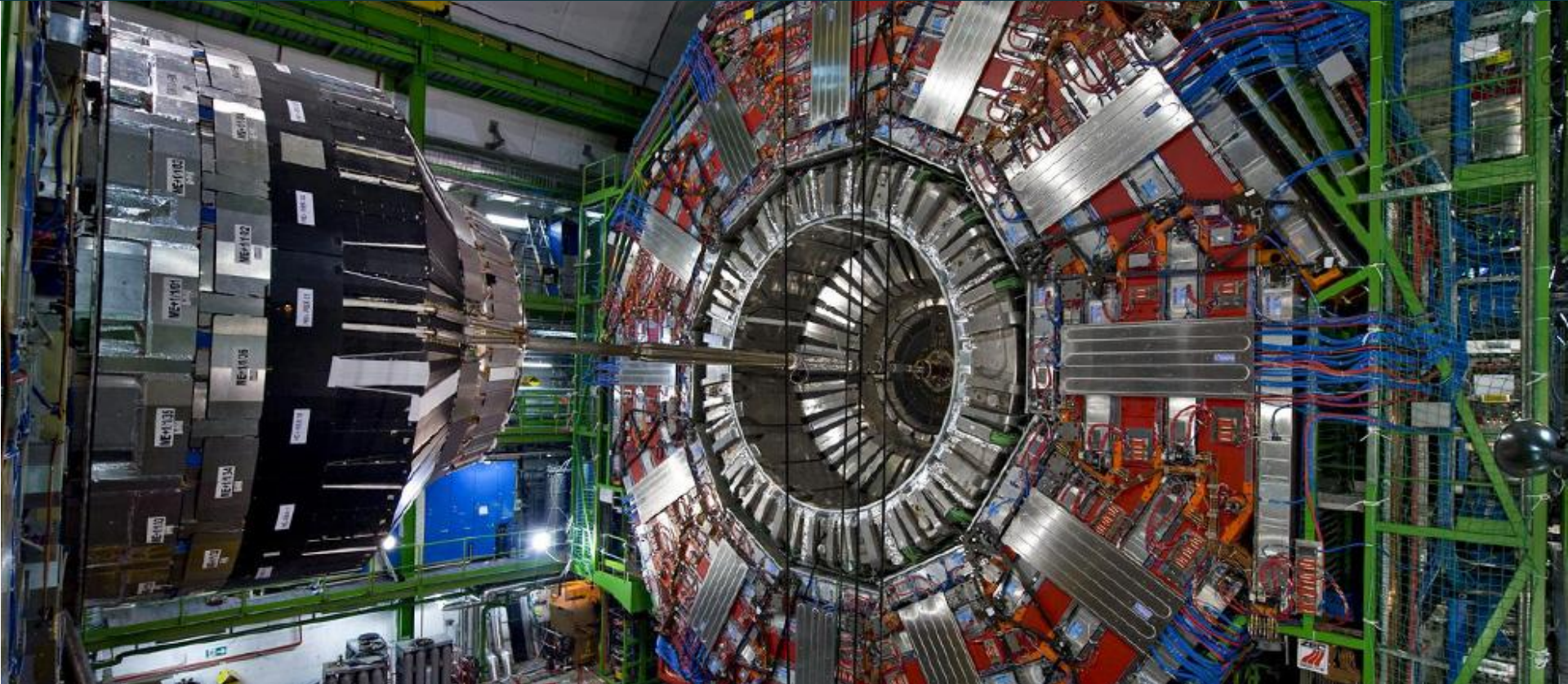
TOOLS: Measuring energy consumption

SOLUTION 1: ARM in HTC

SOLUTION 2: Dynamic pricing and task scheduling

ENERGY EFFICIENCY IN HIGH THROUGHPUT COMPUTING (HTC)

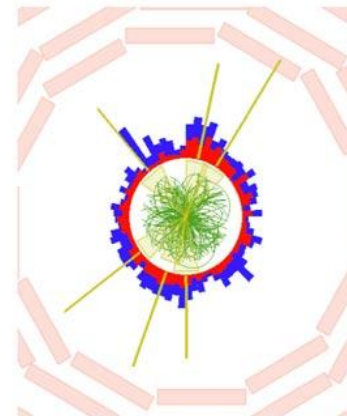
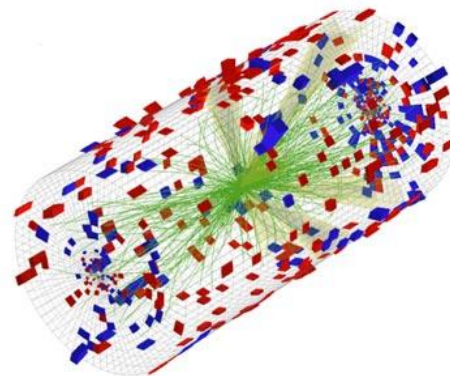
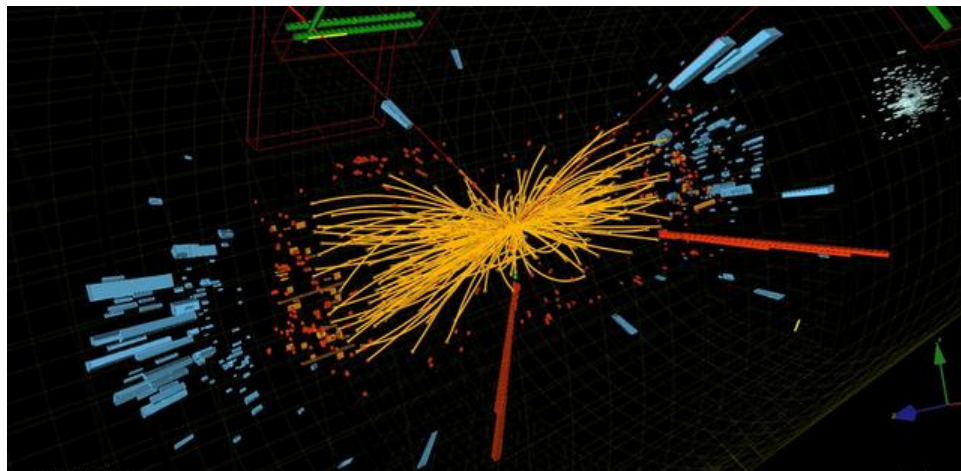
MOTIVATION: HTC, CERN & ENERGY CONSUMPTION



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Lots of data

(1 Petabyte/s \rightarrow 200 MB/s)



MOTIVATION: HTC, CERN & ENERGY CONSUMPTION

In 2012, the Worldwide LHC computing grid *equivalent capacity* of

80,000 to 100,000 x86-64 cores

result: Higgs Boson tracked down

Future

data will increase **2 - 3** orders of magnitude
processing power in proportion

Expectable to happen throughout all HTC industry

MOTIVATION: HTC, CERN & ENERGY CONSUMPTION

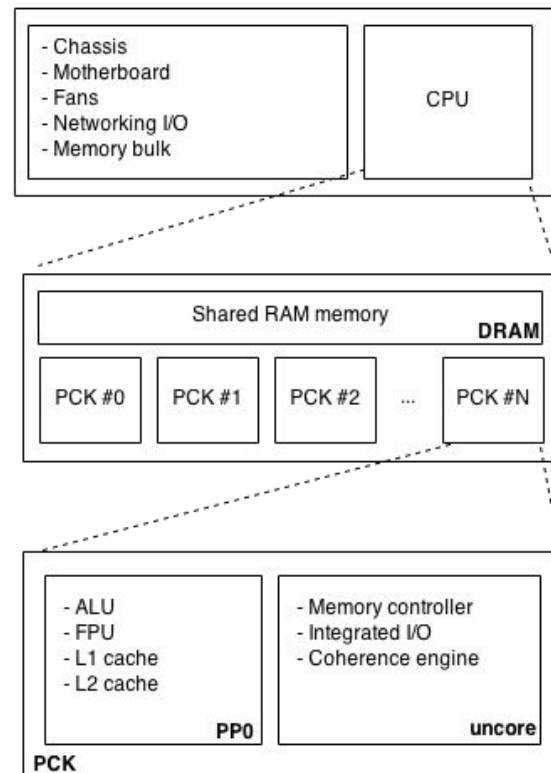
How to decrease electricity bill ?

Techniques and **tools** for measuring energy consumption are important ...

TOOLS: MEASURING ENERGY EFFICIENCY

... and systems are **complex**

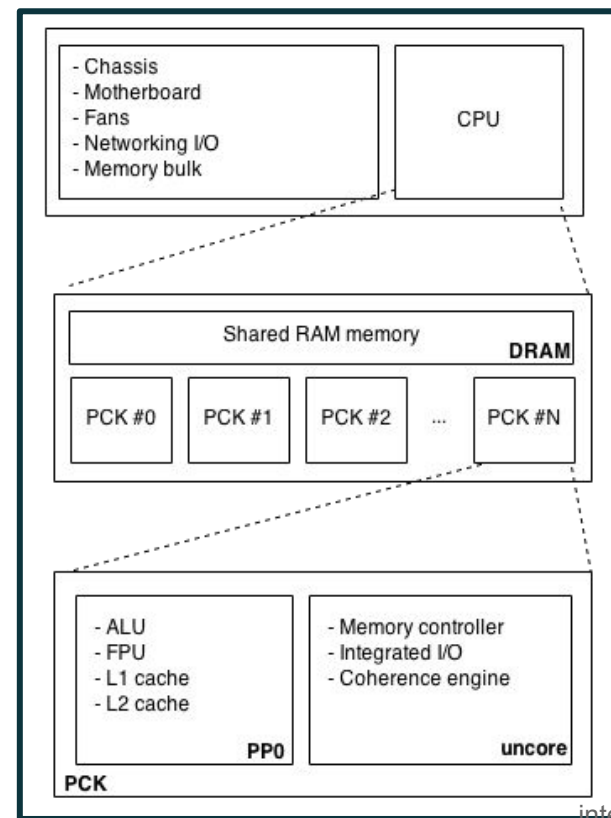
several layers and granularities



TOOLS: MEASURING ENERGY EFFICIENCY

External measurements

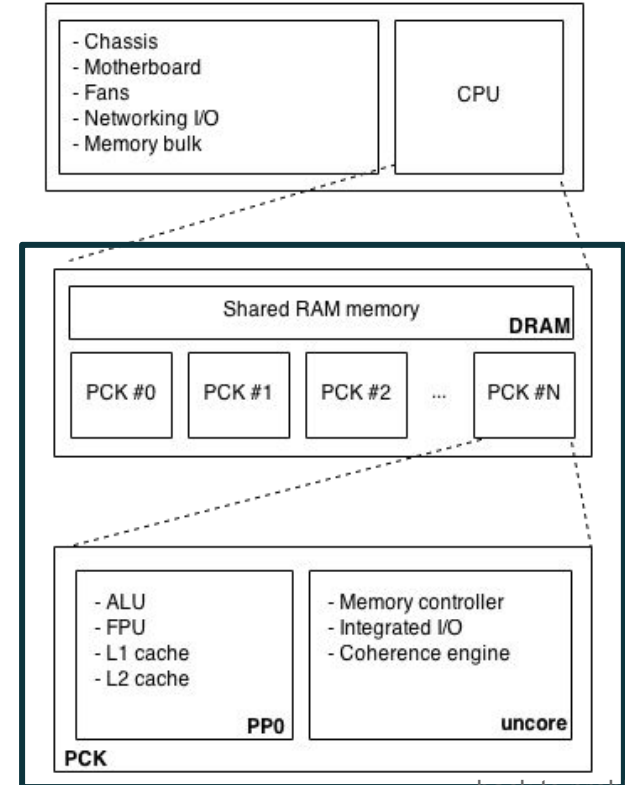
Power consumed without breaking down the system
into components



TOOLS: MEASURING ENERGY EFFICIENCY

On-chip measurements

Power consumed by different components of the CPU



back to our main problem:

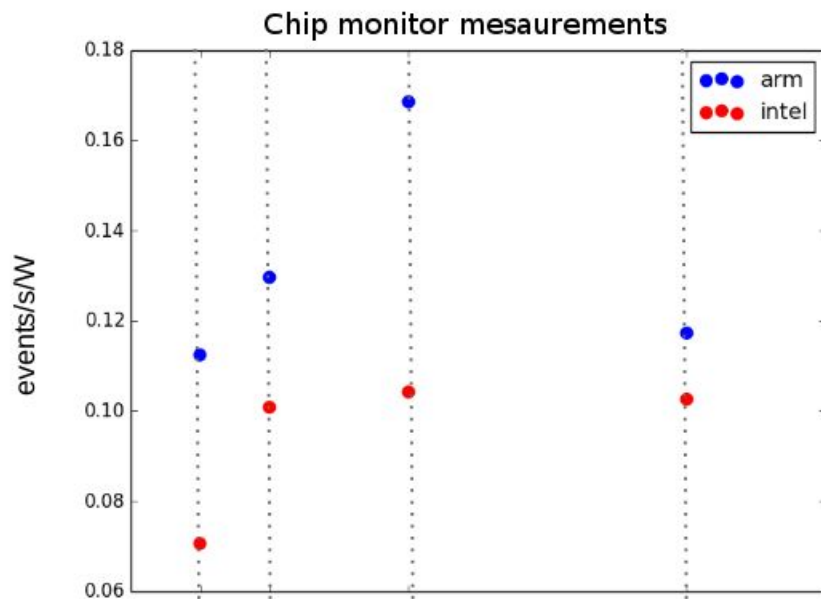
How to decrease electricity bill ?

SOLUTION 1: ARM IN HTC?



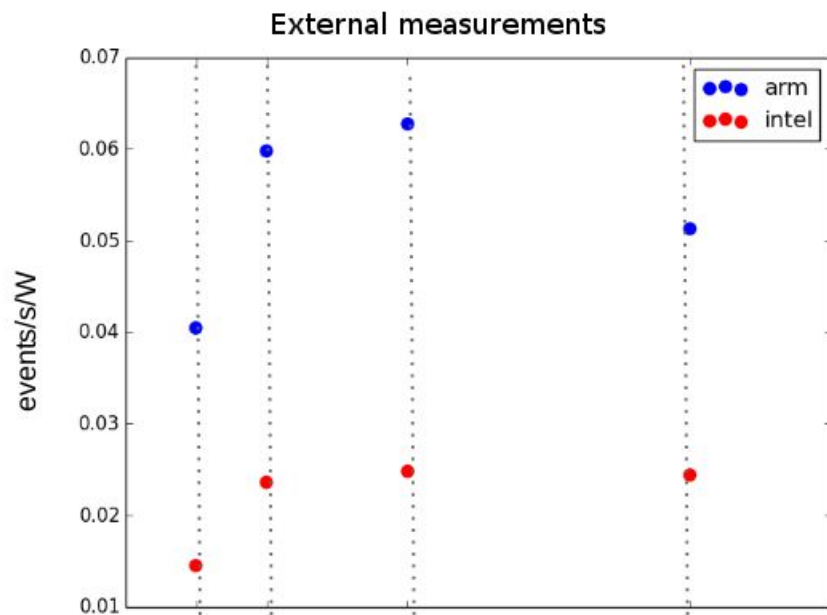
Are smartphones' CPUs
the future of High Throughput Processing ?

SOLUTION 1: ARM IN HTC?



Number events/core
ARM
Intel

1/4	1/2	1	2
1	2	4	8
8	16	32	64



Number events/core
ARM
Intel

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1	2	4	8
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SOLUTION 1: ARM IN HTC?

energy efficiency

VS

speed



back to our main problem:

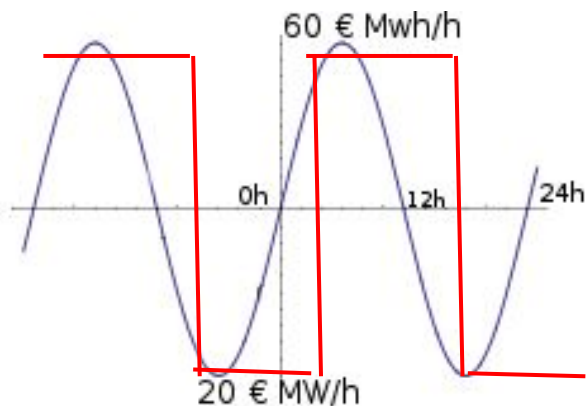
How to decrease electricity bill ?

SOLUTION 2: DYNAMIC PRICING AND TASK SCHEDULING

Task scheduling across different computing architectures in a dynamic pricing energy market

SOLUTION 2: DYNAMIC PRICING AND TASK SCHEDULING

Dynamic electricity price



Machines with different energy profiles

ARM more energy efficient, slower

INTEL less energy efficient, faster

SOLUTION 2: DYNAMIC PRICING AND TASK SCHEDULING

Idea

Schedule tasks to **INTEL** when electricity is cheaper

Schedule tasks to **ARM** when electricity is more expensive

SOLUTION 2: DYNAMIC PRICING AND TASK SCHEDULING

How

Algorithm that computes which machines should compute data based on:

- **deadline** (how many tasks in how much time)
- **energy pricing dynamics**
- **energy profiling of the machines**

CONCLUSIONS

PROBLEM: Energy consumption is bottleneck in HPC

SOLUTION 1: ARM shows potential for HPC (but tradeoffs)

SOLUTION 2: Scheduling tasks based on energy pricing

How to measure energy consumption in complex systems ?

Vague but exciting ...

CERN DD/OC

Tim Berners-Lee, CERN/DD

Information Management: A Proposal

March 1989

Information Management: A Proposal

Abstract

This proposal concerns the management of general information about accelerators and experiments at CERN. It discusses the problems of loss of information about complex evolving systems and derives a solution based on a distributed hypertext system.

Keywords: Hypertext, Computer conferencing, Document retrieval, Information management, Project control



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Q & A

backup

IgProf

application profiler developed at CERN by the CMS software team

general purpose. open source. not experiment specific

measures performance (time spent in functions) and memory usage at *runtime*

allows developer to understand:

- bottlenecks

- where code needs to be optimised

cross platform: recently ported to 64-bit ARM, also supports 32-bit ARM, Intel x86 and x86-64

IgProf & energy profiling

Uses RAPL and PAPI to measure energy consumed.

Map functions and low level operations with **energy consumption**

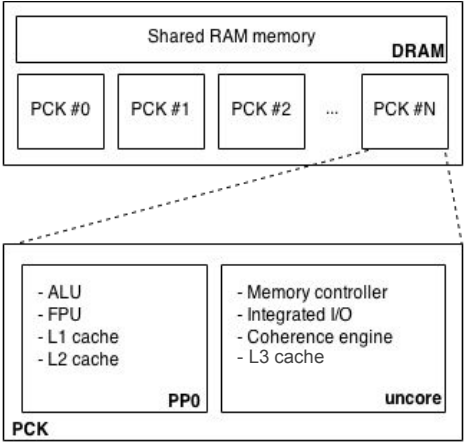
more info (strategies, results, examples)

paper and <http://igprof.org/>

Running Average Power Limiting (RAPL) by Intel

Provides a platform for power monitoring and power limiting of SoC.

Different sampling **domains**
package (*PKG*), DRAM, core



- Low level measurements** package, cores, dram
- Resolution** according to Intel, sampling frequency up to ~1 kHz
- Power capping** is also supported by RAPL
- Accuracy** high (according to *Intel*)

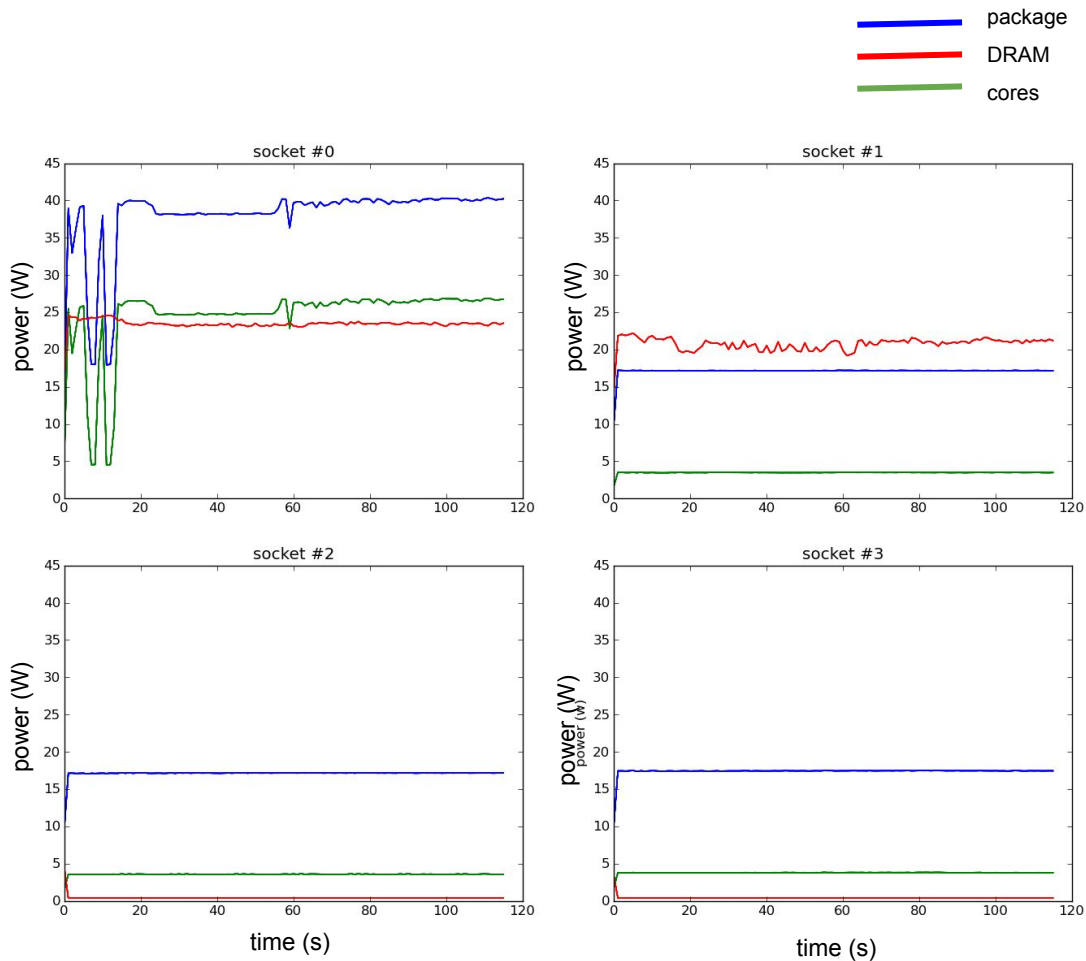
Example of RAPL

System with 4 sockets

Sockets #0 and #1 working

Sockets #2 and #3 idle

Possible to understand how
packages, cores & dram consume
energy



Comparison ARM vs Intel

Comparison ARMv7 vs Intel XEON

32bit ARMv7 is used on smartphones. comparison with Intel XEON

measurements

Internal

RAPL for *Intel*

cross platform *chip monitor* integrated (TI INA 231) for ARMv7

External

workload

ParFullCMS

Multithreaded

Geant4 benchmark application

Uses the CMS geometry

ARMv7 Exynos5 Octa Cortex™
4x A15 @ 1.6Ghz and/or A7 cores (big.LITTLE technology)
2 GB RAM
ARMv7/32bit
development board

Intel 32x Intel™ Xeon™ CPU E5-2650 @ 2.00GHz
252 GB RAM
system on a rack

