GRAHAM PEYTON, PhD

Analog & Mixed Signal IC Architect

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PROFESSIONAL SUMMARY

Analog/Mixed Signal Architect with **10+ years** of IC design experience spanning automotive radar, medical ultrasound-on-chip systems, and advanced RFIC development. Led complete AMS architecture from **concept → tapeout → production** across **11+ successful tapeouts**: Imperial College (2 tapeouts: 0.36µm, 0.18µm CMOS), Butterfly Network (3 tapeouts: 130nm BiCMOS, 65nm CMOS), TeraDAR (6 tapeouts with 4 in development: 55nm BiCMOS, 28nm, 16nm FFC, 8nm). Proven experience in mixed-signal integration, automotive functional safety (ISO26262/ISO21434/AEC-Q100), cross-functional collaboration with digital/software teams, and advanced packaging (MCM, UCIe 250+ Gbps). Utilized automation tools: ADT for parametric circuit generation; Python/C++ for verification and test automation—eager to work with AI-driven design methodologies.

CORE COMPETENCIES

Architecture & Project Leadership
Multi-project execution, schedule management, resource coordination, roadmap development, cross-functional team leadership

Tape-Out Leadership
6+ successful chips: 8nm SoC, 16nm ADC, 65nm AFE, RFIC test structures

Analog IC Design
BGR, LDO, SAR ADC, amplifiers, comparators, DAC, S&H, LVDS, SerDes PHY, OTP eFuse

RFIC System Integration
LNA, PA, mixers, phase shifters, filters—system-level integration expertise

Digital Integration
RTL, P&R (SPI, controllers, SRAM), UCIe die-to-die links, clock distribution

Advanced Packaging
MCM design, UCIe 250+ Gbps, SI/PI modeling (Sigrity/Clarity), TSMC InFO

Functional Safety
ISO26262, ISO21434, AEC-Q100 compliance and validation planning

Design Automation
Analog Design Toolkit (ADT), Verilog-AMS modeling, novel design flows

EDA Tools
Cadence Virtuoso/Spectre/RF, Calibre, Genus/Innovus, Sigrity, Altium

PROFESSIONAL EXPERIENCE

AMS Architect
2022 - Present

TeraDAR Inc.

- Architected complete TX/RX RFIC AMS systems from concept through tapeout—extensive collaboration with ADC, FPGA, co-design, digital SoC, and IP teams
- Led **6 successful tape-outs** (4 in development): TX/RX RFICs (2022-present), RFIC test structures (ongoing), 16nm FFC GHz ADC, 8nm digital SoC, 55nm BiCMOS multi-channel AFE/ADC with SerDes
- Designed AMS blocks: BGR, LDO, SAR ADC, amplifiers, comparators, muxes, LVDS drivers, SerDes PHY, DACs, level shifters; integrated RFIC blocks (LNA, PA, mixers, filters)
- Architected complex MCM package with 250+ Gbps UCIe links—led SI/PI modeling (IR-drop, PDN, clock distribution, high-speed interconnect)
- Drove ISO26262/ISO21434/AEC-Q100 compliance and drafted complete validation plan for production ATE
- Accelerated development using Analog Design Toolkit (ADT) automation software; initiated Verilog-AMS/SV RNM RF modeling
- Architected cross-functional C APIs and XML data structures unifying verification, test/bring-up, and production software

Electrical Engineering Lead
2021 - 2022

Liminal Sciences Inc.

- Led wearable medical imaging hardware development: owned PCBA design cycle (architecture, schematic, layout, SI/PI, DFM/DFT, EMC compliance, NPI)
- Key contributor to R&D strategy; hiring manager for hardware/firmware positions

Principal Imaging Engineer
2020 - 2021

Butterfly Network Inc.

- Optimized imaging presets and developed panoramic imaging algorithms using Python/C++ with clinical performance validation

Analog/Mixed-Signal ASIC Engineer
2018 - 2020

Butterfly Network Inc.

- Contributed to **ISSCC 2021 8960-element ultrasound-on-chip with MEMS-integrated transducer array**: designed/laid out OTP eFuse, 5GHz SerDes TX, LVDS drivers (3 tapeouts: 130nm BiCMOS, 65nm CMOS)
- Advanced packaging design/modeling (TSMC InFO) for MEMS-ASIC integration, chip characterization, longevity testing, V&V, board bring-up

Earlier Roles
2010 - 2018

Aqua Nova, Microsonix, Oxbridge Biotech/Roche, think3dots, RoJo Medical, ESKOM

- **Microsonix (2016-2017):** Founded startup, won 2017 Venture Catalyst Challenge (£10k seed funding)
- **Oxbridge Biotech/Roche (2016-2017):** Strategic healthcare IT consulting, presented to C-level management
- **Earlier positions:** Financial analytics, medical device engineering, power systems development

EDUCATION

PhD, Electrical Engineering (Focus: Analog/Mixed-Signal IC Design)

Imperial College London, UK | 2014-2017

Bio-inspired VLSI Circuits & Systems Group • 2 tapeouts (0.36µm, 0.18µm CMOS) • President's PhD Scholarship (top ~1% globally)

MSc Engineering (cum laude) | Electrical Engineering

University of the Witwatersrand, South Africa | 2013

BScEng Electrical (summa cum laude) | **BEngSc Biomedical (summa cum laude)**

University of the Witwatersrand | 2008-2012

SAIMM Prestige Prize (best student across all engineering disciplines)

KEY TECHNICAL SKILLS

Analog Design:
Cadence Virtuoso, Spectre/APS, Virtuoso RF, ADT, Calibre (DRC/LVS/PEX), Verilog-A/AMS

SI/PI & Packaging:
Sigrity/Clarity 3D, IR-drop/PDN analysis, high-speed modeling, TSMC InFO, MCM

Process Tech:
8nm, 16nm FFC, 65nm, 180nm (TSMC, Samsung foundries)

Digital Tools:
Genus/RTL Compiler, Innovus/Encounter, Verilog/VHDL, SystemVerilog, FPGA tools

Software:
Python, C/C++, MATLAB, OCEAN/SKILL, TCL, Git, CI/CD, AI coding tools

Standards:
ISO26262, ISO21434, AEC-Q100, Medical (FDA/CE)

PATENTS & PUBLICATIONS

6 Patent Filings: 4 US patents (wireless ultrasound architectures, data offloading, miniaturized imaging systems); 2 automotive radar patents filed

Key Publication: Nevada Sanchez, Kailiang Chen, **Graham Peyton**, et al., "An 8960-Element Ultrasound-on-Chip for Point-of-Care Ultrasound," *IEEE ISSCC 2021*

Additional: IEEE Transactions on Biomedical Circuits and Systems, BioMedical Engineering Online (first author)