GRAHAM PEYTON, PhD

Analog & Mixed Signal IC Architect

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EXECUTIVE SUMMARY

Accomplished **Analog/Mixed Signal IC Architect** with **10+ years** leading complex chip development from concept through production tape-out. **11+ successful tapeouts** across a wide range of technologies, including 0.36µm, 65nm, 28nm, 130nm HV BiCMOS, 55nm RF BiCMOS. Also currently managing projects in 16nm and 8nm with extremely tight schedules. Proven track record with ultra-high bandwidth applications such as automotive RFICs/SoCs and MEMS-integrated medical ASICs. Career highlights:

- **Mixed-signal architecture & technical roadmap leadership**—led multi-project execution from concept to production, managing schedules, resources, and cross-functional teams while balancing technical capability with customer strategy
- **Analog/mixed-signal design expertise**—BGR, LDO, SAR ADC, amplifiers, comparators, eFuse, LVDS, SerDes PHY, DAC, level shifters, clocking circuits, temperature sensors, diagnostics
- **Rare combination of hardware and software expertise**—hands-on circuit design combined with software proficiency, enabling faster development and unique systems-level understanding from silicon to software
- **Cross-functional leadership**—extensive collaboration with product, digital, verification, EE, software, test and ASIC teams
- **Experience with automation tools**—utilized ADT for parametric circuit generation; developed Python/C++ automation for verification and test workflows
- **Advanced packaging & modeling expertise**—MCM design, UCIe 250+ Gbps links, comprehensive SI/PI modeling
- **Regulatory Standards**—good understanding of a range of automotive, medical standards such as ISO26262 / ISO21434 / AEC-Q100 & IEC 60601

Combines strategic vision and adaptability with modern tools and workflows—adept at leveraging cutting-edge methodologies and technologies to drive efficient, innovative chip design in fast-paced development environments.

CORE COMPETENCIES

- **Mixed-Signal Architecture:** System architecture, roadmap development, IP selection, requirements → specifications
- **Analog IC Design:** BGR, LDO, SAR ADC, DAC, amplifiers, comparators, S&H, LVDS, SerDes PHY, eFuse, muxes, level shifters, clocking
- **RFIC Integration:** LNA, PA, mixers, phase shifters, filters—system-level integration and interface definition
- **Digital Integration:** P&R (SPI, controllers, SRAM, SAR logic), UCIe links (250+ Gbps), RTL, Verilog-A/AMS modeling
- **Advanced Packaging:** MCM design, SI/PI modeling (Sigrity/Clarity), IR-drop/PDN analysis, TSMC InFO
- **Verification & Validation:** Lab bring-up, ATE test plans, ISO26262/ISO21434/AEC-Q100 compliance, DFT/DFM
- **Tools & Automation:** Cadence Virtuoso/Spectre/Calibre, Genus/Innovus, ADT, Python/C++ for test automation

PROFESSIONAL EXPERIENCE

AMS Architect

2022 - Present

TeraDAR Inc.

Lead architect and owner for all automotive radar mixed-signal systems. Key coordinator between product, RFIC, digital, verification, EE, and systems teams.

Architecture, Roadmap & Project Leadership

- Led multi-project execution managing many tapeouts often running concurrently—coordinated schedules, resources, and deliverables across product, imaging, FPGA, digital, test and systems teams
- TX/RX RFIC AMS architect & team lead, managing block-level requirements, specifications, and AMS team members
- Led IP selection and integration strategy evaluating performance, cost, schedule, and integration risk trade-offs
- Mentored junior engineers on mixed-signal design best practices and automotive standards compliance

AMS Lead - TX/RX RFICs and Breakouts

- Current AMS lead on 55nm BiCMOS / 28nm CMOS automotive radar TX/RX RFICs—multiple successful tapeouts with ongoing product evolution
- Architected all designs in compliance with ISO26262 (Functional Safety), ISO21434 (Cybersecurity), AEC-Q100 (Automotive Qualification) standards
- Designed AMS building blocks: BGRs, LDOs, diagnostic SAR ADCs, amplifiers, comparators, analog muxes, DACs, clocking, level shifters, temperature sensors. Leveraged Analog Design Toolkit (ADT) to accelerate development
- Integrated RFIC blocks: LNA, PA, mixers, phase shifters, RF filters—responsible for system-level integration and interface definition
- Currently kicking off Verilog-AMS and SystemVerilog RNM behavioral models of RF blocks in frequency domain for faster mixed-signal verification
- Owner of all digital architecture & development: RTL, synthesis/PNR, scan chain, backend infrastructure and verification suite. Manage design repository, version control (Git).
- Architected cross-functional C APIs and gold-standard XML data structures unifying verification environment, test/bring-up software, and production software systems

Project Lead - 65nm Multi-Channel AFE/ADC ASIC

- Led complete development from concept to tapeout of 65nm multi-channel multiplexed baseband ADC chip with integrated SerDes
- Contributed to various blocks such as IF mux, amplifiers, ADC SAR controller, SerDes PHY & serializer
- Managed place & route: SPI controllers, digital state machines, ADC SAR logic, level shifters, clock distribution
- Owned chip-level characterization, lab testing, and board bring-up—developed test procedures and debugged silicon issues

Current Project Lead - 16nm ADC ASIC

- Architected high-speed, multiplexed ADC system from scratch and defined complete technical specifications for outsourced development team
- Managed external development partner: requirements definition, schedules, IP selection, design reviews, verification planning, tapeout coordination

Architectural Contributor - 8nm Digital SoC

- Ongoing architectural contributor to 8nm digital SoC—defined mixed-signal interfaces and system integration strategy
- Specified AMS UCIe interface requirements, system-level verification planning and cross-domain validation with EE, digital and AMS teams

Verification & Validation

- DRI on all AMS verification & RF modeling across all RFICs
- Busy drafting complete validation plan for production automated test equipment (ATE)—defined test coverage, fault injection strategies, and acceptance criteria
- Implemented Design-for-Test (DFT) and Design-for-Manufacturing (DFM) methodologies across all projects
- Led chip-level characterization, lab testing, and board bring-up activities—developed test procedures and debugged silicon issues

Packaging and Modeling

- Architected complex multi-chip module (MCM) package integrating AMS + digital SoCs with high-speed interconnect and massive IF fanout
- Architected 250+ Gbps UCIe die-to-die links for chip-to-chip communication
- Led comprehensive SI/PI modeling effort: IF routing SI analysis, IR-drop simulation, PDN optimization, clock distribution, high-speed UCIe interconnect characterization
- Drove packaging vendor selection and stackup optimization balancing cost, performance, reliability, and ISO26262 safety constraints

Electrical Engineering Lead

2021 - 2022

Liminal Sciences Inc.

Led wearable medical imaging hardware development from concept through manufacturing.

- Owned PCBA design cycle: architecture, schematic, layout, SI/PI analysis, DFM/DFT optimization (>95% first-pass yield)
- Led board bring-up, verification, environmental qualification, and EMC compliance (FCC Part 15, CE) certification
- Managed integration with firmware team and coordinated manufacturing NPI with contract manufacturers
- Key contributor to R&D strategy and IP development; hiring manager for hardware/firmware positions

Principal Imaging Engineer

2020 - 2021

Butterfly Network Inc.

- Led optimization of imaging presets (B-mode, Doppler, M-mode) balancing quality, frame rate, and power
- Spearheaded panoramic imaging development—stitching algorithms and real-time display integration using Python/C++
- Developed software tools in Python/C++ for image processing, algorithm optimization, and performance analysis
- Collaborated with clinical team on performance validation against regulatory requirements

Analog/Mixed-Signal ASIC Engineer

2018 - 2020

Butterfly Network Inc.

Key contributor to the world's first 8960-element MEMS-integrated ultrasound-on-chip transducer array. 4 tapeouts in 130nm BiCMOS, 65nm, 28nm CMOS.

- Designed, laid out, and tested OTP eFuse memory block
- Designed and laid out 5GHz SerDes TX link and LVDS drivers—met jitter and power specs at 1.2V supply
- Advanced packaging design/modeling using TSMC InFO technology—optimized ball assignment, routing, thermal performance for MEMS-ASIC integration
- Chip characterization and board bring-up—automated test procedures, PVT corner analysis
- Longevity testing, V&V, reliability assessment for medical device requirements

Earlier Roles

2010 - 2018

AquaNova, Microsonix, Oxbridge Biotech/Roche, think3dots, RoJo Medical, ESKOM

- **Microsonix (2016-2017):** Founded medical ultrasound startup. Winner: 2017 Venture Catalyst Challenge (£10k seed funding). Filed UK patent GB1621423 for miniaturized wireless ultrasound system
- **Oxbridge Biotech/Roche (2016-2017):** Strategic healthcare IT consulting; led team and presented to C-level management at Roche HQ, Basel
- **Earlier positions (2010-2013):** Financial analytics consulting (machine learning), medical device engineering, power systems development

TECHNICAL SKILLS & TOOLS

EDA Tools & Software

Analog Design

- Cadence Virtuoso (Schematic, Layout, ADE/ADE-XL), Spectre, APS, Virtuoso RF
- Analog Design Toolkit (ADT), Calibre (DRC, LVS, PEX)
- Verilog-A, Verilog-AMS, SystemVerilog RNM

Digital Design

- Cadence Genus, RTL Compiler, Cadence Innovus, Encounter
- Verilog, VHDL, SystemVerilog
- Xilinx Vivado, Intel Quartus

PCB, SI/PI & Packaging

- Ansys Sigrity, Cadence Clarity 3D Solver
- Altium Designer, Eagle PCB

Programming & Scripting

- Python, C/C++, MATLAB
- OCEAN, SKILL, TCL, Bash/Shell
- Proficient with a variety of web-based languages, though only consider myself a vibe coder :)
- Git, GitHub, GitLab, SVN

EDUCATION

PhD, Electrical Engineering

2014 - 2017

Imperial College London, United Kingdom

Focus: Analog/Mixed-Signal IC Design (Bio-inspired VLSI Circuits & Systems Group)

- **2 tapeouts:** 0.36µm, 0.18µm CMOS—custom AFE, digital beamformer, PCB design
- **President's PhD Scholarship:** Top ~1% of global applicants

MSc Engineering (cum laude) | Electrical Engineering

2013

University of the Witwatersrand, South Africa

BScEng Electrical (summa cum laude) | BEngSc Biomedical (summa cum laude)

2008 - 2012

University of the Witwatersrand, South Africa

- **SAIMM Prestige Prize:** Best student across all engineering disciplines

PATENTS & PUBLICATIONS

6 Patent Filings: 4 US patents (wireless ultrasound architectures, data offloading, miniaturized imaging systems); 2 automotive radar patents filed

Key Publication: Nevada Sanchez, Kailiang Chen, **Graham Peyton**, et al., "An 8960-Element Ultrasound-on-Chip for Point-of-Care Ultrasound," *IEEE ISSCC 2021*

Additional: IEEE Transactions on Biomedical Circuits and Systems, BioMedical Engineering Online (first author)

PROFESSIONAL AWARDS & HONORS

President's Imperial College PhD Scholarship (2014-2017): Top ~1% of global applicants

Winner: 2017 Venture Catalyst Challenge: UK's largest university innovation competition—£10k seed funding

SAIMM Prestige Prize (2012): Best student across all engineering disciplines, Wits University