Impedance Matching

Objectives

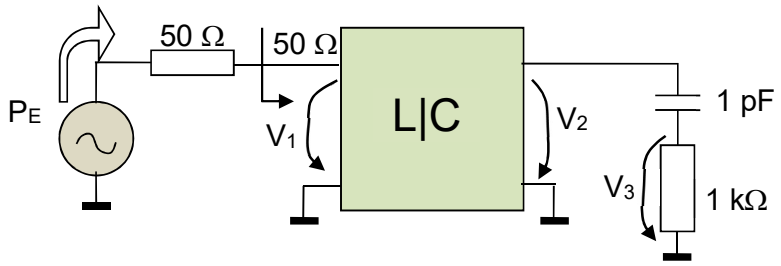
- Introduction to the simulation of electronic circuits with Spice-based simulators
- Study the use of RLC networks in impedance matching networks.

1. Introduction

SPICE is the acronym for "Simulation Program with Integrated Circuit Emphasis". The first version of this program was developed in the early 1970s at the University of California, Berkeley, by Larry Nagel, under the name SPICE1. In 1971 it was made available in the public domain and since then it has undergone several improvements and has allowed the emergence of several commercial products that have SPICE at their core, such as Pspice, IS_Spice, Rspice, Micro_Cap V, Electronics Workbench, HSPICE, and LTSpice. The latter, distributed by Analog Devices, will be used in ESC classes. A user's guide and a download link can be found in the ESC course's Moodle space.

2. Power Transmission and Impedance Matching

I - Consider the following interconnection between the output of a circuit (source), with an internal resistance of 50 Ω, and a load impedance formed by the series of a 1 pF capacitor and a 1 kΩ resistor.



a) Calculate the rms values of voltages V_1, V_2, and V_3 (in V) for a source power of P_E = 1 mW @ 40 MHz. Notice that the input impedance seen at V_1 is assumed to be 50 Ω. Assume that the L|C network provides a perfect impedance matching @ 40 MHz.

b) Design an L|C network to be inserted between source and load that ensures maximum power transmission at 40 MHz.

c) Simulate the designed circuit and confirm the results obtained with the hand calculations.

II - Admit you want to transmit a power of 4.5 mW to a 100 Ω load in a 6 MHz band around a frequency of 50 MHz using an amplifier with an output resistance of 1 kΩ, whose maximum output voltage (sinusoidal) is 6 V_{peak}. Design the L|C impedance matching network (with low-pass characteristics) to be used so that the amplifier delivers this power within the allowable voltage excursion limits.

a) Using an L-shaped network.

b) Using a π network.

c) Simulate the designed circuits and confirm the results obtained with the hand calculations.

III - The clock signal of a CMOS digital integrated circuit (IC) shows an amplitude of 0 – 1,5 V, frequency of 2,5 GHz, and a rising/falling time of $t_{r,f}$ = 40 ps. It is provided by a square wave oscillator whose output resistance is 5 Ω. The length of the trace (microstrip like) that connects the two ICs is 1 cm long and shows a thickness of T=34,8 μm. The PCB is of FR4 type (H=0,78 mm) and presents a dielectric constant ε_r=4 ($\varepsilon_0 = 8.854 \times 10^{-12}$ F/m).

a) Calculate the width (W) recommended for the PCB microstrip so that its characteristic impedance is Z_0 = 50 Ω.

b) Is this connection likely to show clock ringing at receiver IC? Design the impedance matching (line termination) solution that would prevent this to occur.