

Gilead Posluns

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gposluns

Education

- 2022–2026 **PhD**, *University of Toronto*, Toronto
Electrical and Computer Engineering
○ Bell Graduate Scholarship
- 2020–2022 **MASc**, *University of Toronto*, Toronto,
Electrical and Computer Engineering
○ Edward S Rogers Sr. Graduate Scholarship
- 2015–2020 **BASc in Engineering Science**, *University of Toronto*, Toronto
Electrical and Computer Engineering
○ President's Entrance Scholarship
○ Dean's list 2015–2016, 2016–2017, 2017–2018, 2019–2020

Research

- 2022 **Publication**, *A Scalable Architecture for Reprioritizing Ordered Parallelism*, ISCA 2022, DOI: 10.1145/3470496.3527387
- 2022 **Masters Thesis**, *A Speculative Hardware Scheduler Supporting Priority Updates*
- 2020 **Undergraduate Thesis**, *Extending Multi-path Execution to a Multiprocessor Context*

Experience

- 2020–2023 **Teaching Assistant**, *University of Toronto*
○ ESC180/ESC190 Intro to Computer Programming
○ ECE243 Computer Organization
○ ECE344/ECE353 Operating Systems
○ ECE552 Computer Architecture
○ ECE1755 Parallel Computer Architecture and Programming
- 2018–2019 **SoC Design Engineering Intern**, *Intel Corporation*, Toronto
Developed and maintained tools used for silicon correlation and test pattern generation
○ Designed and ran ML-based analysis of silicon correlation results for previous design families to inform correlation test stamp allocation for new Agilex device family;
○ Maintained an updated internal silicon correlation and pattern generation tools:
- Documented and automated update process for pattern generation tools;
- Architected major refactor of silicon correlation flow to enable new analysis types;
○ Designed and created new pattern generation tools;
- Automated previously manual pattern generation processes for some test pattern types;
- Improved wire coverage of previously manual pattern types by an order of magnitude;
- 2017–2017 **Research Assistant**, *Intelligent Sensory Microsystems Lab*, University of Toronto
NSERC USRA funded position
Developed FPGA/C++ interface to send commands to and receive output from two-bucket camera sensor prototype.

Skills

Programming: C/C++, Java, Python, Perl
CAD Tools: IAR, Quartus, Vivado

FPGAs: Verilog
Other: Arduino, Matlab, etc