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Research Interests

I explore different ways to schedule tasks for parallel execution. This is a challenging problem because scheduling constraints are not always known when building the schedule, so a good scheduler must adapt to new information. When building these schedulers, we can go beyond simply adhering to constraints and use our available flexibility to seek the best schedules, which could not necessarily have been generated statically even if all constraints were known. My past work has been published at ISCA, a top tier computer architecture conference.

Education

2022–present **PhD**, *University of Toronto*, Toronto
Electrical and Computer Engineering
- Advisor: Professor Mark Jeffrey

2020–2022 **MASc**, *University of Toronto*, Toronto,
Electrical and Computer Engineering
- Thesis: A Scalable Architecture for Reprioritizing Ordered Parallelism
- Advisor: Professor Mark Jeffrey

2015-2020 **BASc in Engineering Science**, *University of Toronto*, Toronto
Electrical and Computer Engineering
- Graduated with Honours
- Thesis: Extending Multi-path Execution to a Multiprocessor Context
- Dean's list 2015-2016, 2016-2017, 2017-2018, 2019-2020

Peer-Reviewed Publications

Scholarships and Awards

2022-2023 **Bell Graduate Scholarship**, *University of Toronto*
$20000

2021-2022 **Queen Elizabeth II GSST**, *University of Toronto*
$15000

2017 **NSERC Undergraduate Student Research Award**, *University of Toronto*
$6000

2015 **President's Entrance Scholarship**, *University of Toronto*
$2000

Work Experience

2020-2023 **Teaching Assistant**, *University of Toronto*
- ESC180/ESC190 Intro to Computer Programming
- ECE243 Computer Organization
- ECE344/ECE353 Operating Systems
- ECE552 Computer Architecture
- ECE1755 Parallel Computer Architecture and Programming

2018-2019 **SoC Design Engineering Intern**, *Intel Corporation*, Toronto

Developed and maintained tools used for silicon correlation and test pattern generation

- Designed and ran ML-based analysis of silicon correlation results for previous design families to inform correlation test stamp allocation for new Agilex device family;
- Maintained an updated internal silicon correlation and pattern generation tools:
  - Documented and automated update process for pattern generation tools;
  - Architected major refactor of silicon correlation flow to enable new analysis types;
- Designed and created new pattern generation tools;
  - Automated previously manual pattern generation processes for some test pattern types;
  - Improved wire coverage of previously manual pattern types by an order of magnitude;

2017-2017 **Research Assistant**, *Intelligent Sensory Microsystems Lab*, University of Toronto

NSERC USRA funded position

Developed FPGA/C++ interface to send commands to and receive output from two-bucket camera sensor prototype.