Laboratorio VHDL

Hoja de respuestas del laboratorio “Máquinas de Estados Finitos”

Asignatura: DSED

Número de grupo:1

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1-1: Haz una demo del comportamiento de tu diseño al profesor. Copia y pega el contenido de los ficheros .vhd:

```
entity lab5_1_1 is
  Port ( clk : in STD_LOGIC;
      reset : in STD_LOGIC;
      ain : in STD_LOGIC;
      yout : out STD_LOGIC;
      cont : out STD_LOGIC_VECTOR (3 downto 0));
end lab5_1_1;

architecture Behavioral of lab5_1_1 is

  type state_type is (S0,S1,S2);
  signal state, next_state : state_type;
  signal next_cont : STD_LOGIC_VECTOR(3 downto 0) := "0000";
  signal cont_reg: STD_LOGIC_VECTOR(3 downto 0) := "0000";
  signal yout_reg: std_logic;

begin
  SYNC_PROC : process (clk)
  begin
    if rising_edge(clk) then
      if (reset = '1') then
        cont_reg <= (others=>'0');
        state <= S0;
      else
        state <= next_state;
        cont_reg <= next_cont;
      end if;
    end if;
end process;

OUTPUT_DECODE : process (state,ain)
begin
    yout_reg <= '0';
    case (state) is
      when S0 =>
        yout_reg <= '1';

      when S1 =>
        yout_reg <= '0';

      when S2 =>
       yout_reg <= '0';

      when others =>
        yout_reg <= '0';
    end case;
end process;

NEXT_STATE_DECODE : process (state,ain,cont_reg)
begin
    next_state <= S0;
    next_cont <= cont_reg;
    case (state) is
      when S0 =>
        if (ain = '1') then
          next_state <= S1;
          next_cont <= std_logic_vector(unsigned(cont_reg)+1);
        elsif(ain = '0') then
          next_state <= S0;
        end if;

      when S1 =>
        if (ain = '1') then
          next_state <= S2;
          next_cont <= std_logic_vector(unsigned(cont_reg)+1);
        elsif(ain = '0') then
          next_state <= S1;
        end if;

      when S2 =>
        if (ain = '1') then
          next_state <= S0;
          next_cont <= std_logic_vector(unsigned(cont_reg)+1);
        elsif(ain = '0') then
            next_state <= S2;
        end if;

      when others =>
        next_state <= S0;
    end case;
  end process;
```

```
yout <= yout_reg;

cont <= cont_reg;


end Behavioral;
```

2-1: Haz una demo del comportamiento de tu diseño al profesor. Copia y pega el contenido de los ficheros .vhd:

```
entity lab5_2_1 is
  Port ( clk : in STD_LOGIC;
         reset : in STD_LOGIC;
         ain : in STD_LOGIC_VECTOR (1 downto 0);
         yout : out STD_LOGIC);
end lab5_2_1;

architecture Behavioral of lab5_2_1 is

type state_type is (Sres,S00,S01,S10,S11,St0,St1);
signal state, next_state : state_type;
signal yout_s : STD_LOGIC := '0';

  begin
  SYNC_PROC : process (clk)
    begin
      if rising_edge(clk) then
        if (reset = '1') then
          state <= Sres;
        else
          state <= next_state;
        end if;
      end if;
  end process;

  OUTPUT_DECODE : process (state)
    begin
     case (state) is
        when Sres =>
```

```
          yout_s <= '0';
        when S00 =>
        when S01 =>
          yout_s <= '0';
        when S10 =>
        when S11 =>
          yout_s <= '1';
        when St0 =>
        when St1 =>
          yout_s <= not(yout_s);
        when others =>
    end case;
end process;

NEXT_STATE_DECODE : process (state, ain)
  begin

  if(ain = "01") then
     next_state <= S00;
  elsif(ain = "10") then
     next_state <= St0;
  elsif(ain = "11") then
     next_state <= S10;
  end if;

  case (state) is
      when Sres =>
        if (ain = "00") then
           next_state <= Sres;
        end if;
      when S00 =>
```

```
         if (ain = "00") then
             next_state <= S01;
         end if;

      when S01 =>
         if (ain = "00") then
             next_state <= S01;
         end if;

       when S10 =>
         if (ain = "00") then
             next_state <= S11;
         end if;

       when S11 =>
         if (ain = "00") then
             next_state <= S11;
         end if;

       when St0 =>
         if (ain = "00") then
             next_state <= St1;
         end if;

       when St1 =>
         if (ain = "00") then
             next_state <= St1;
         end if;
    end case;
end process;
```

```
yout <= yout_s;

end Behavioral;
```

3-1: Haz una demo del comportamiento de tu diseño al profesor. Copia y pega el contenido de los ficheros .vhd:

```
entity lab5_3_1 is
    Port ( clk : in STD_LOGIC;
           reset : in STD_LOGIC;
           count : out STD_LOGIC_VECTOR (2 downto 0));
end lab5_3_1;

architecture Behavioral of lab5_3_1 is

    type state_type is (S000,S001,S011,S101,S111,S010);
    signal state, next_state : state_type;
    signal cont_reg, next_cont: STD_LOGIC_VECTOR(2 downto 0) := "000";

begin

    SYNC_PROC : process (clk)
    begin
        if rising_edge(clk) then
            if (reset = '1') then
                cont_reg <= "000";
                state <= S000;
            else
                state <= next_state;
                cont_reg <= next_cont;
            end if;
        end if;
    end process;

    NEXT_STATE_DECODE : process (state)
    begin
```

```
        next_cont <= "000";
        next_state <= S000;

        case(state) is
          when S000 =>
            next_cont <= "001";
            next_state <= S001;
          when S001 =>
            next_cont <= "011";
            next_state <= S011;
          when S011 =>
            next_cont <= "101";
            next_state <= S101;
          when S101 =>
            next_cont <= "111";
            next_state <= S111;
          when S111 =>
            next_cont <= "010";
            next_state <= S010;
          when S010 =>
            next_cont <= "000";
            next_state <= S000;
          when others =>
            next_cont <= "000";
            next_state <= S000;
          end case;
    end process;

count <= cont_reg;

end Behavioral;
```