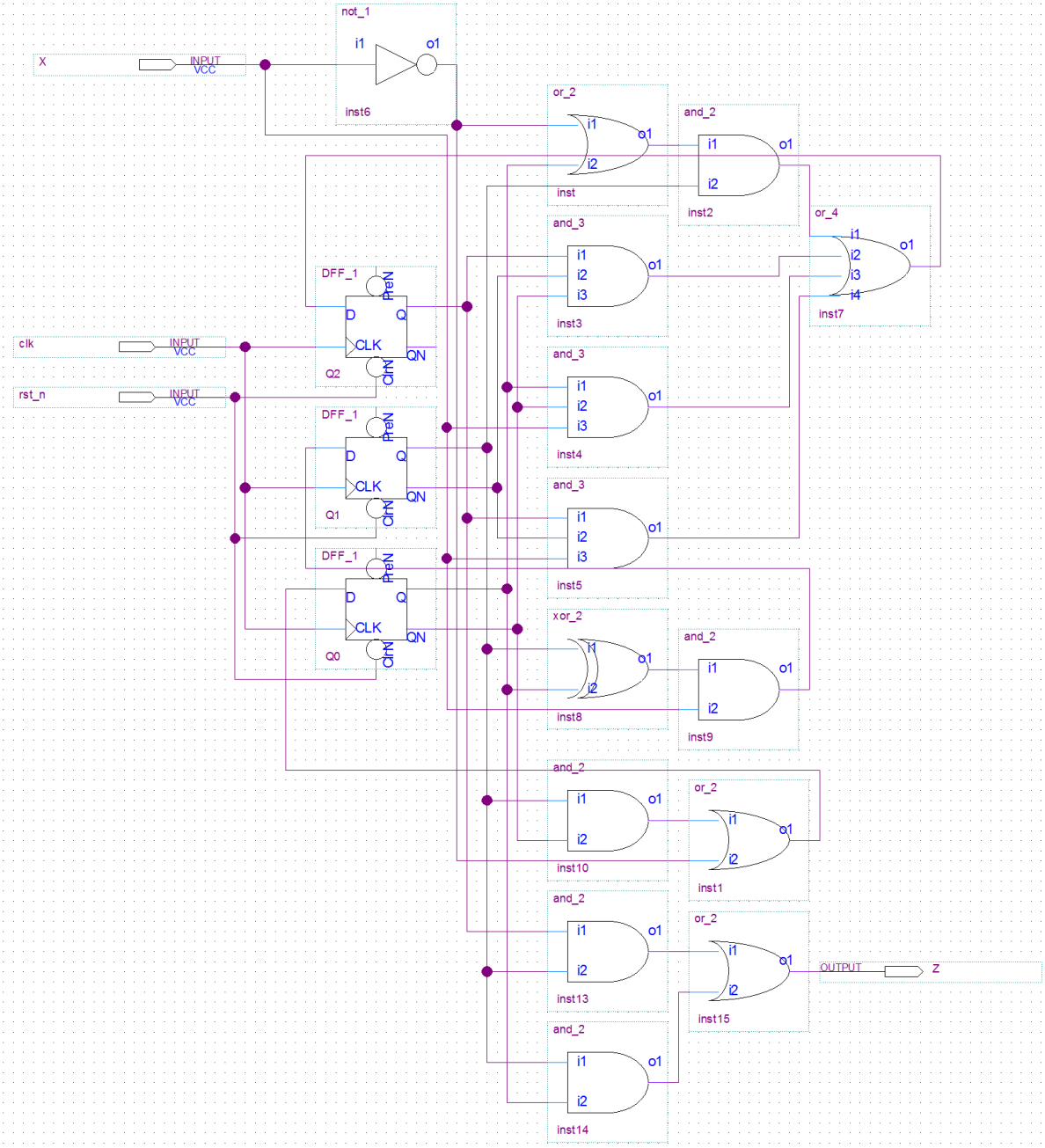
Quartus II Lab2 — Sequential Circuits

NTU Switching Circuit and Logic Design 2023

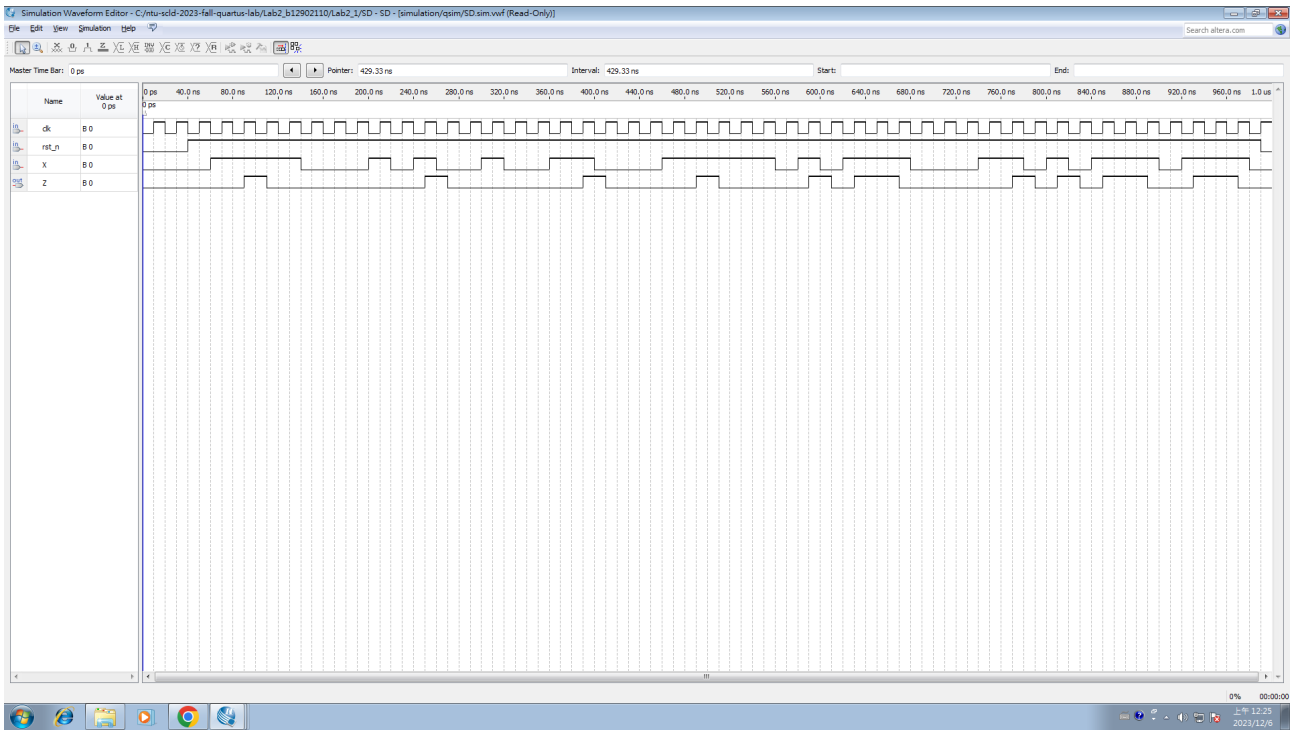
B12902110 呂承諺

1 Lab2_1

1.1 SD: Sequence Detector



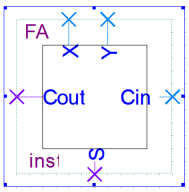
SD.bdf



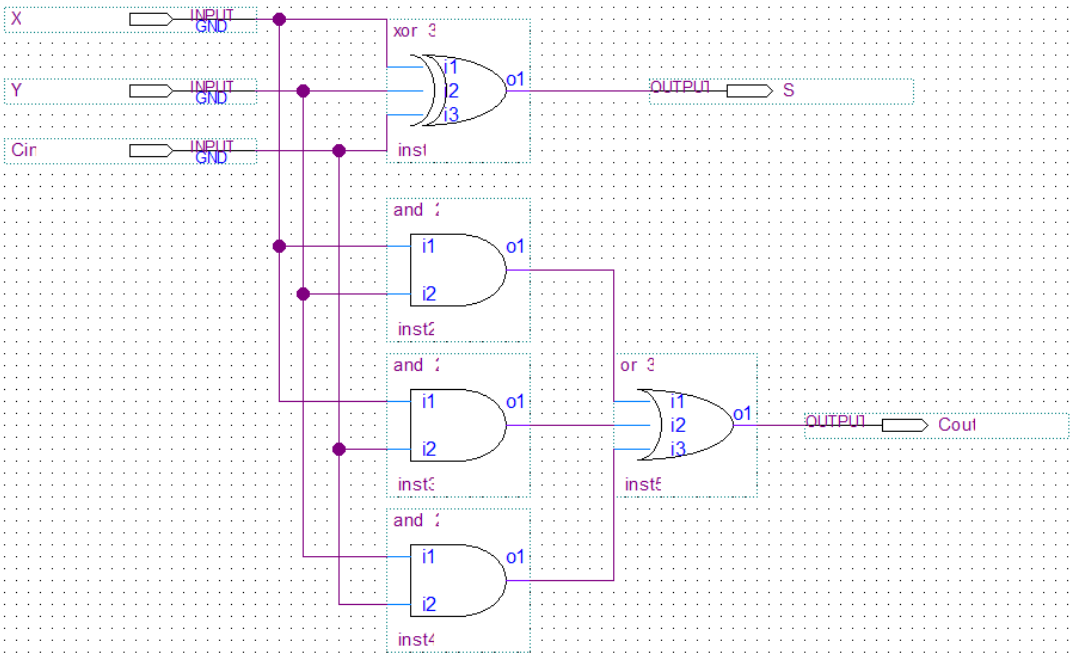
SD simulation result

2 Lab2_2

2.1 FA: 1-bit Full Adder

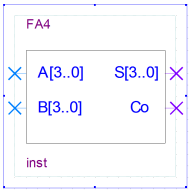


FA.bsf

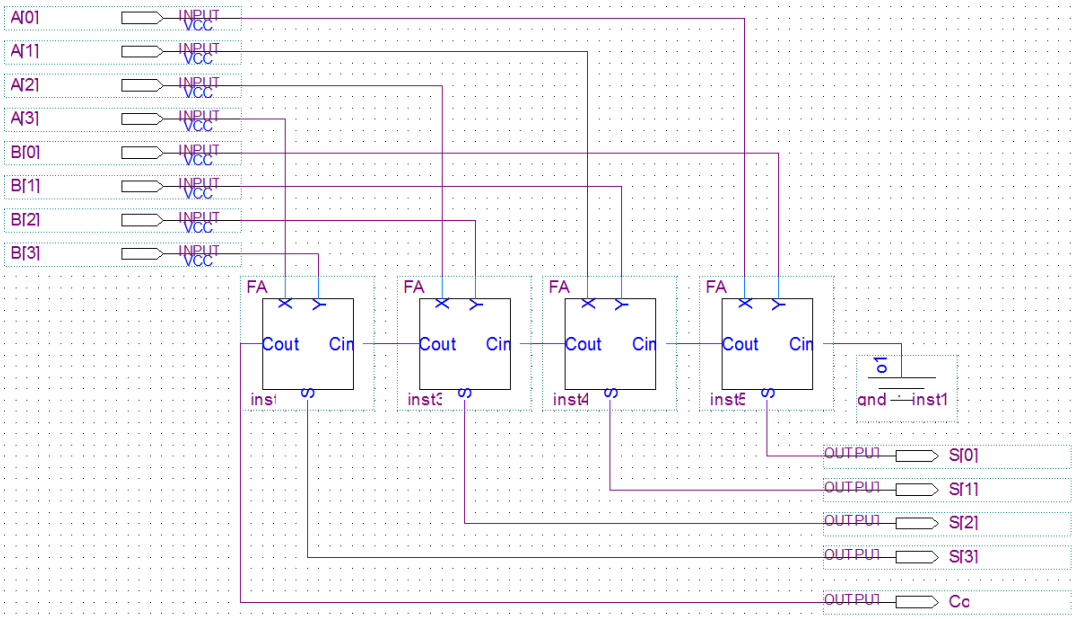


FA.bdf

2.2 FA4: 4-bit Adder

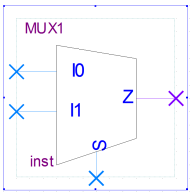


FA4.bsf

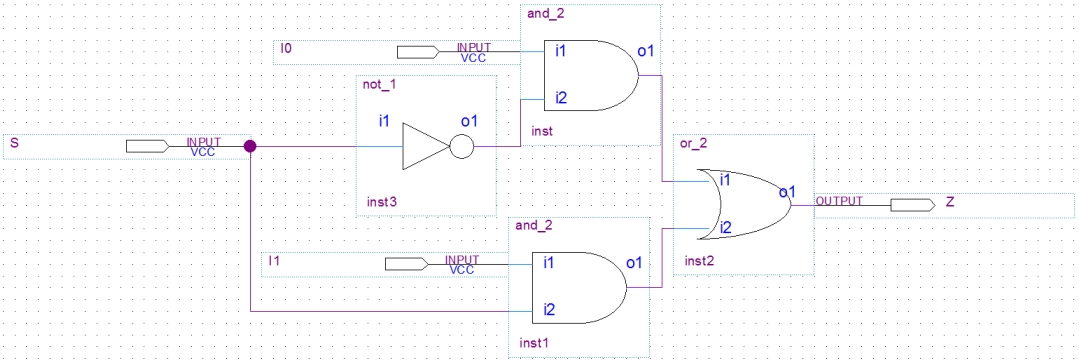


FA4.bdf

2.3 MUX1: 1-bit 2-to-1 Multiplexer

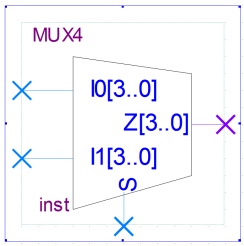


MUX1.bsf

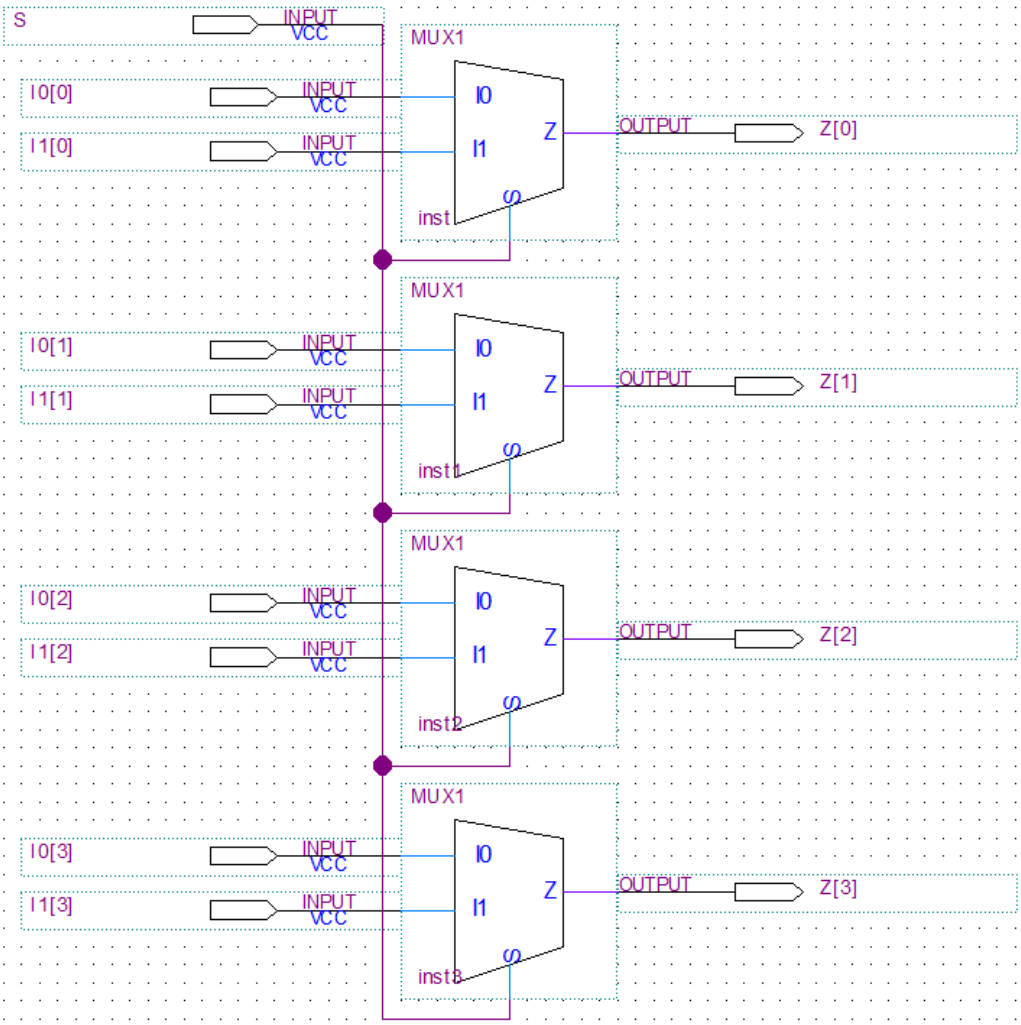


MUX1.bdf

2.4 MUX4: 4-bit 2-to-1 Multiplexer

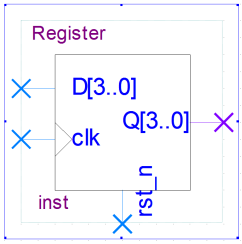


MUX4.bsf

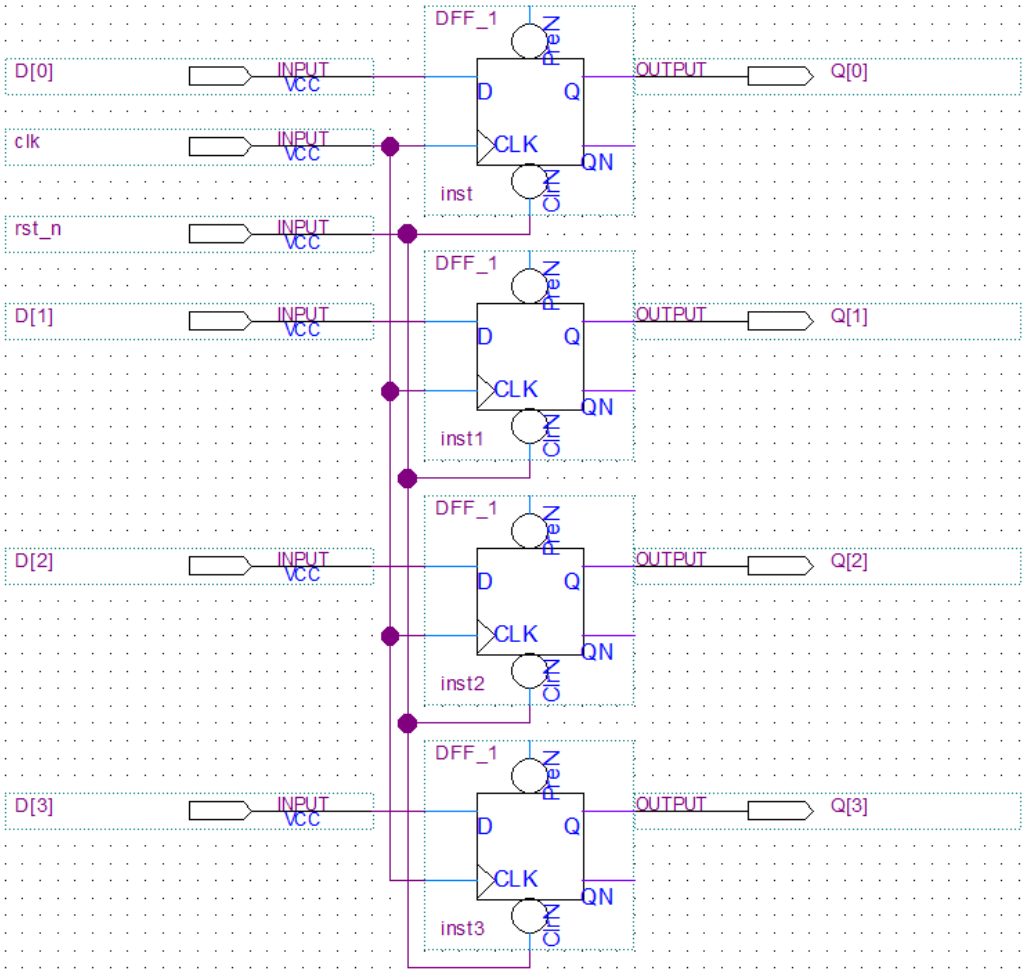


MUX4.bdf

2.5 Register: 4-bit Register

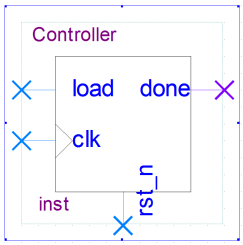


Register.bsf

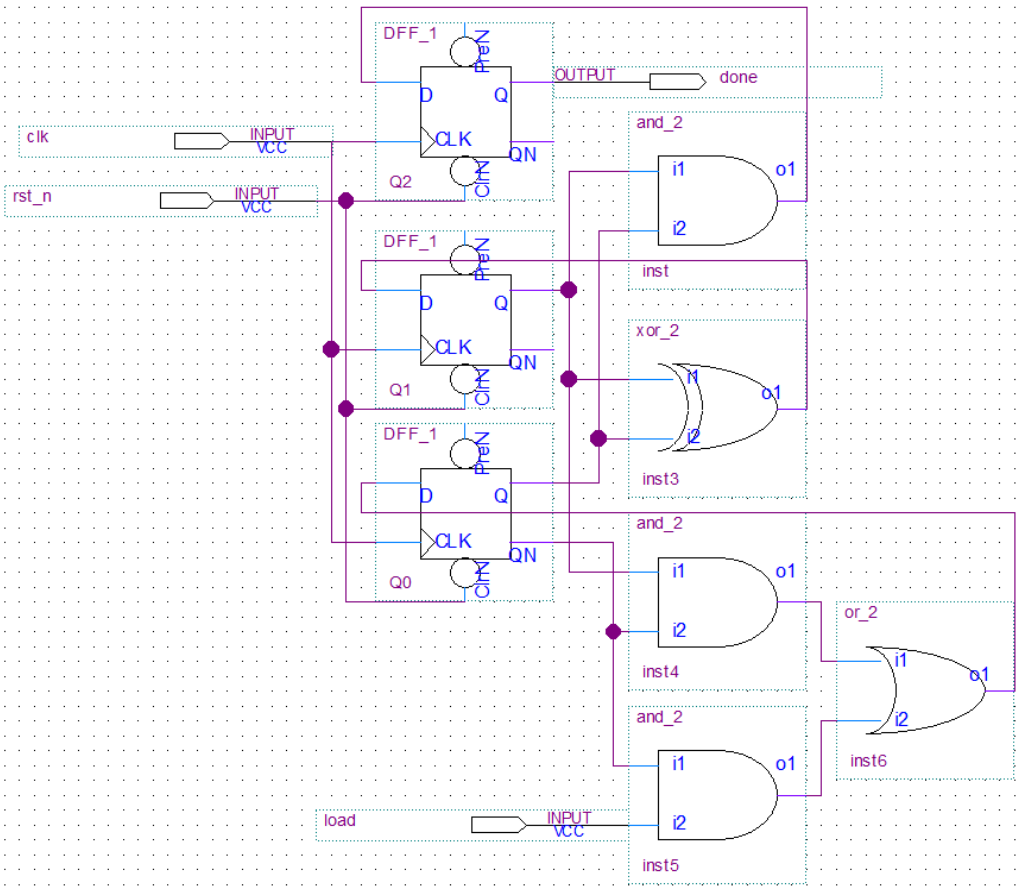


Register.bdf

2.6 Controller: Finite-state Machine

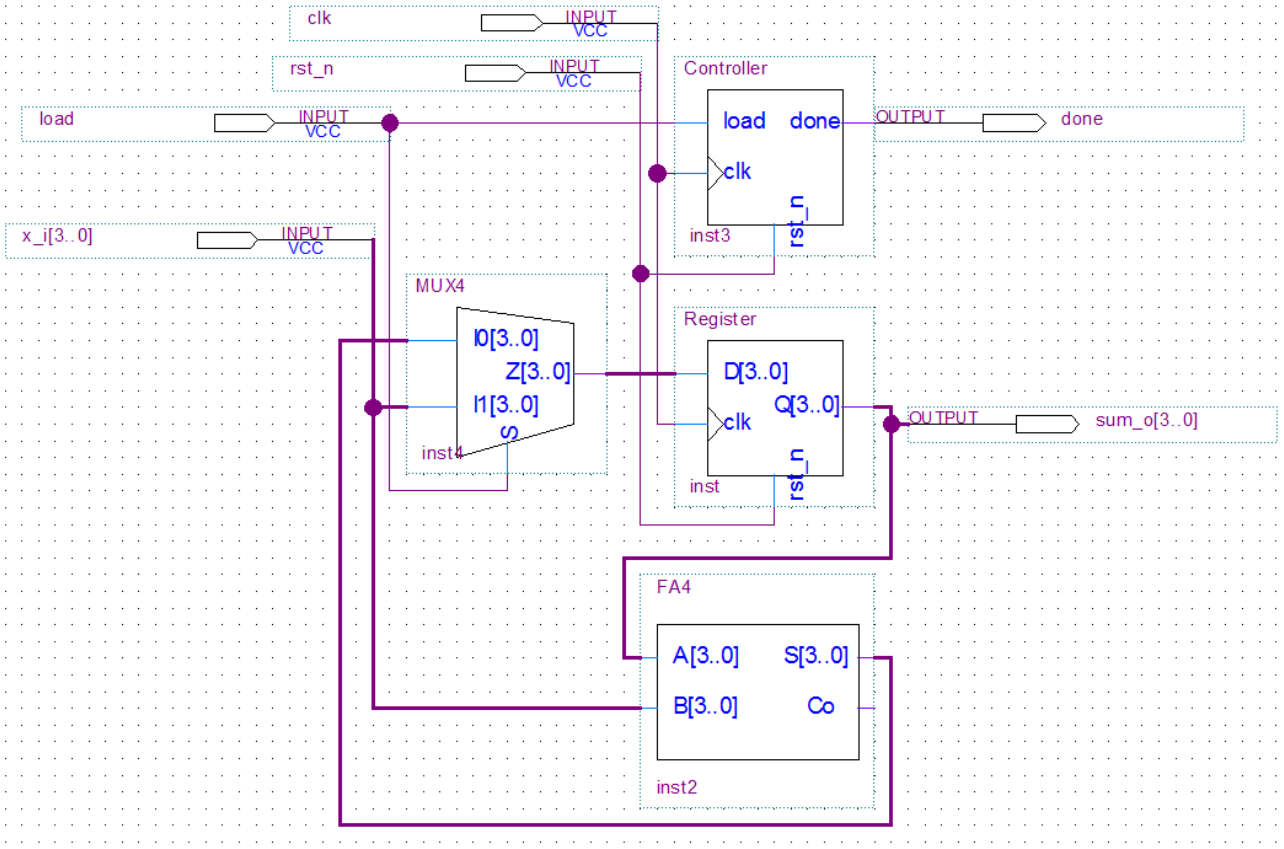


Controller.bsf

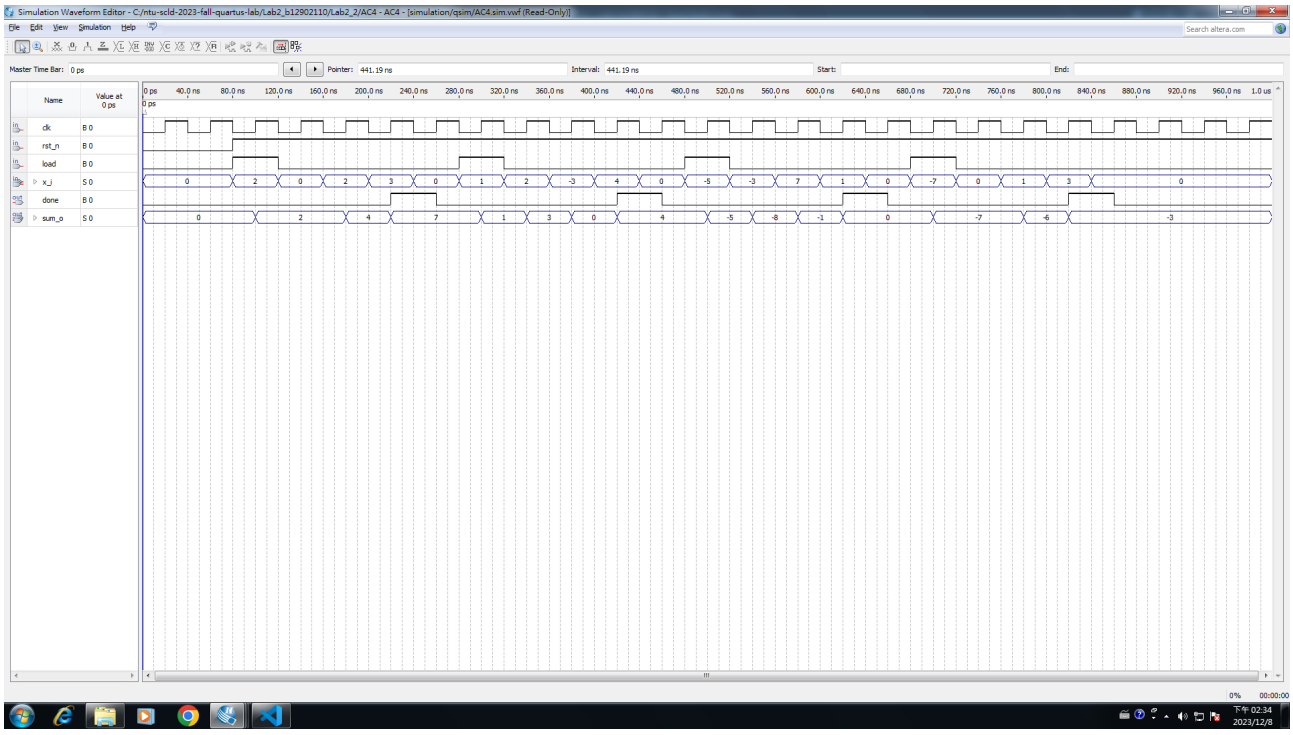


Controller.bdf

2.7 AC4: 4-bit Accmulator



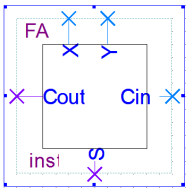
AC4.bdf



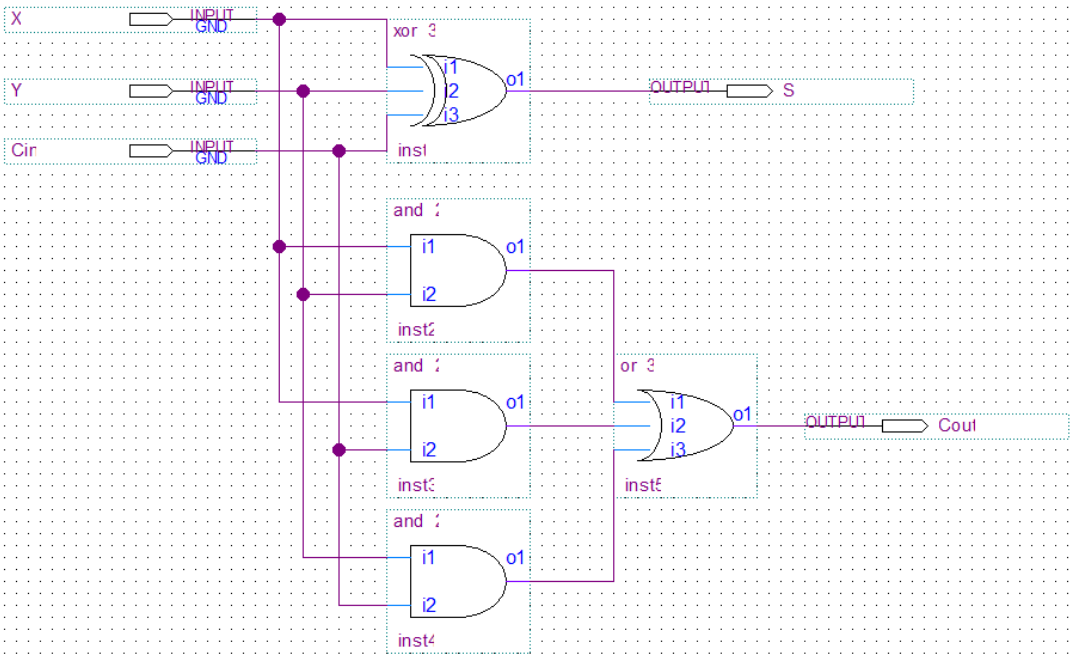
AC4 simulation result

3 Lab2_3

3.1 FA: 1-bit Full Adder

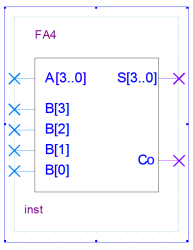


FA.bsf

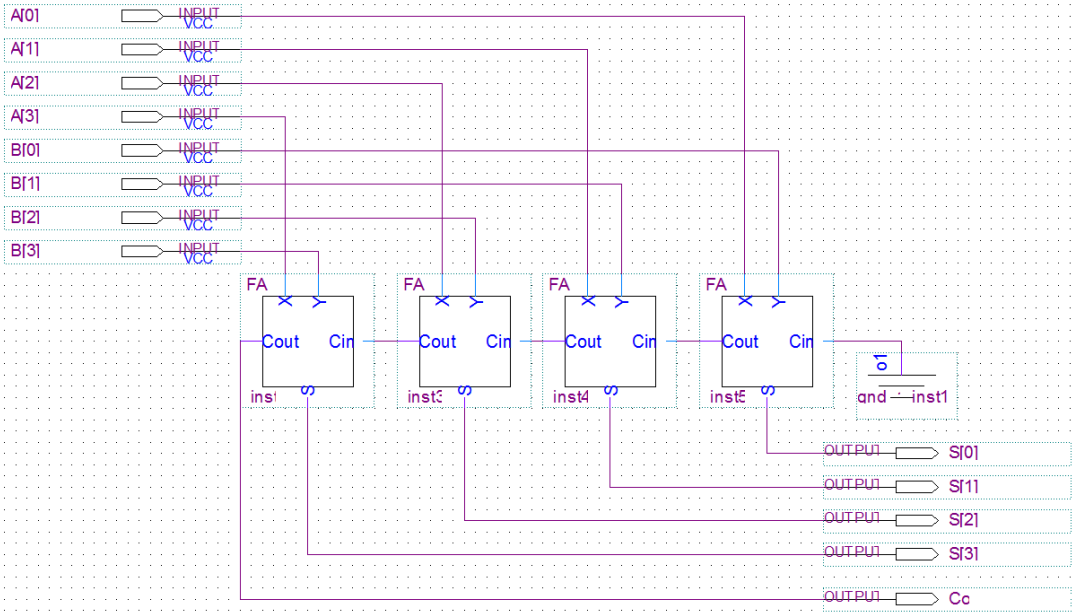


FA.bdf

3.2 FA4: 4-bit Adder

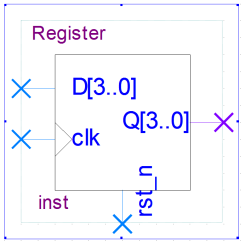


FA4.bsf

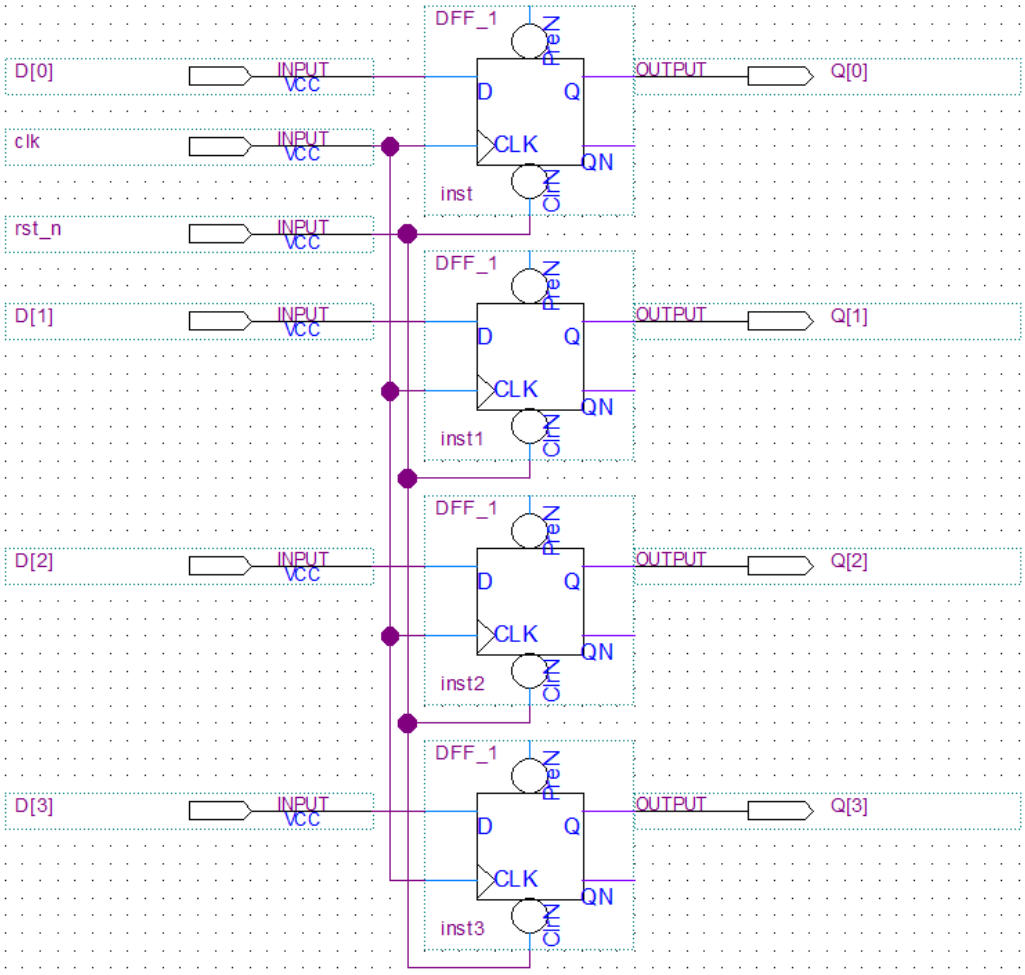


FA4.bdf

3.3 Register: 4-bit Register

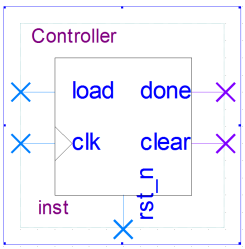


Register.bsf

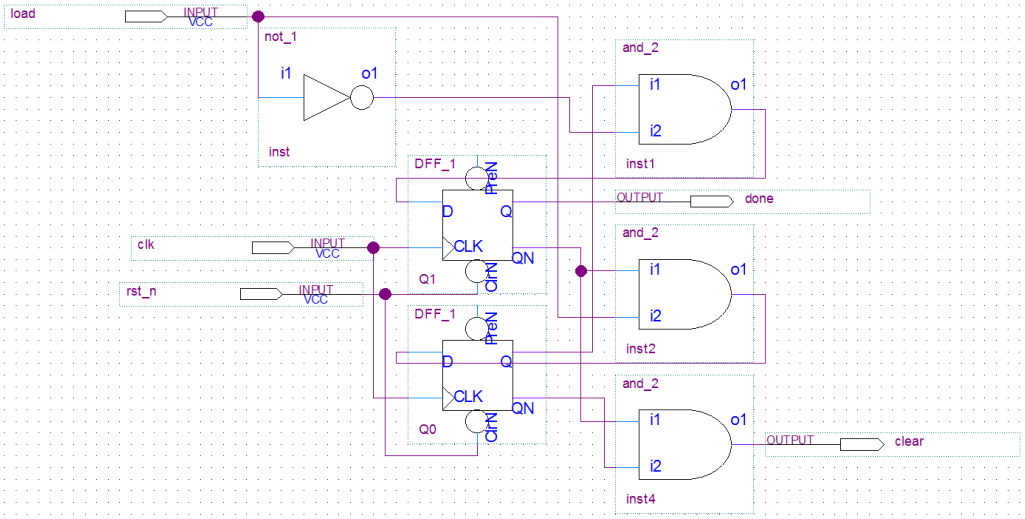


Register.bdf

3.4 Controller: Finite-state Machine

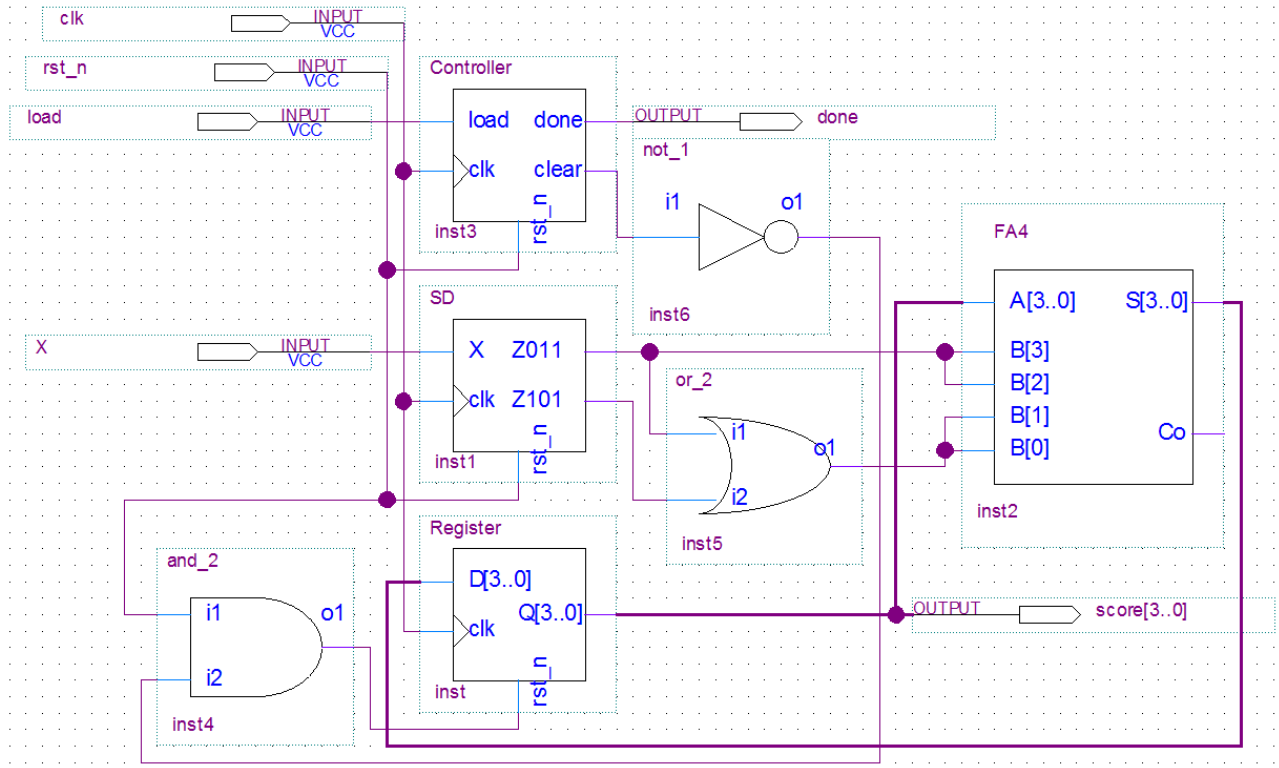


Controller.bsf

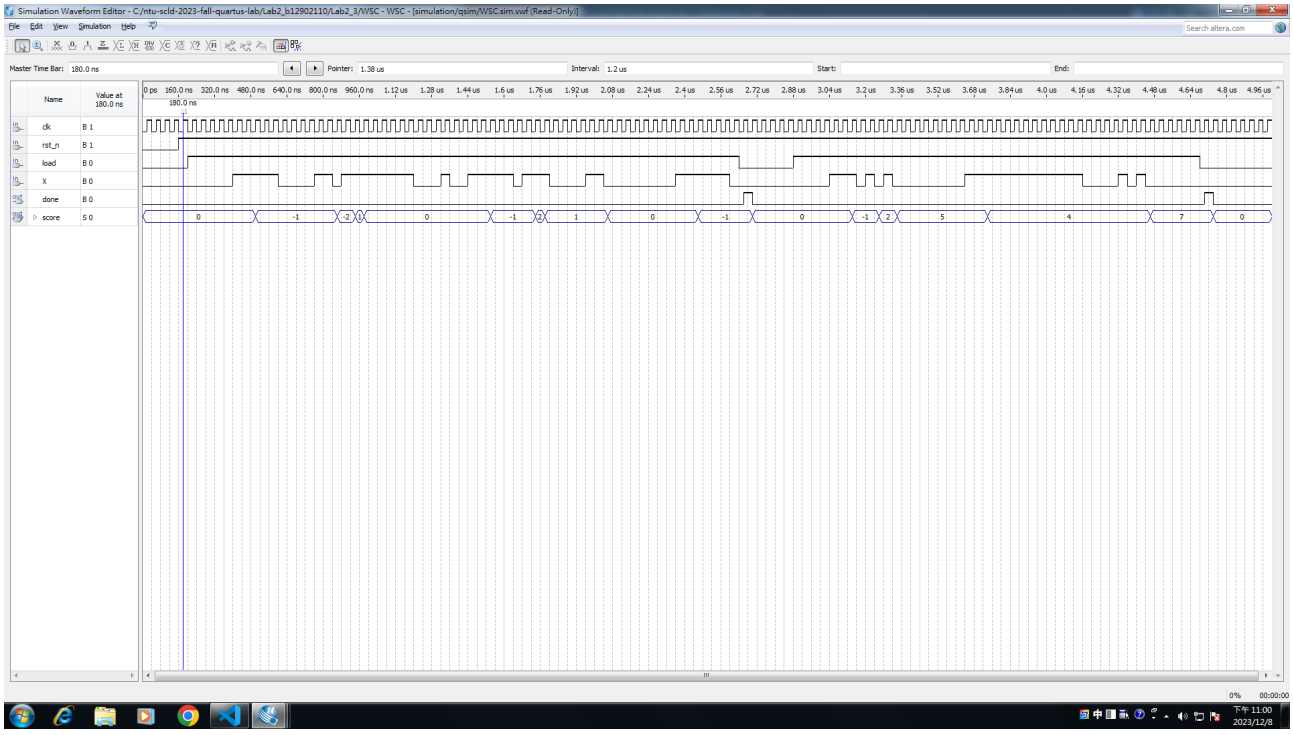


Controller.bdf

3.5 WSC: Weighted Sequence Counter



WSC.bdf



WSC simulation result