Switching Circuit and Logic Design 2023

Lab1-Combinational Circuit

Deadline: 2023.11.24 23:59:59

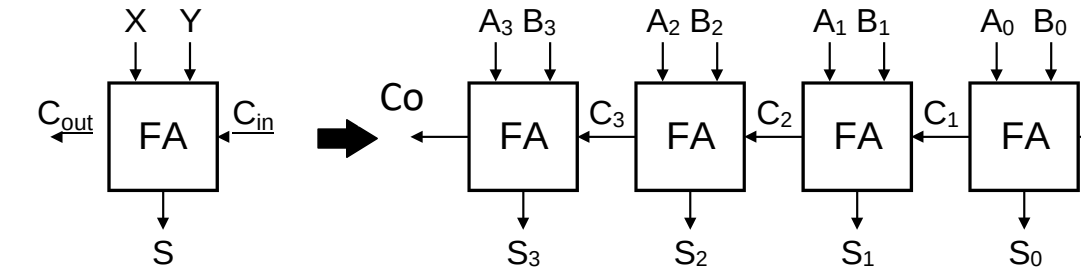
Introduction

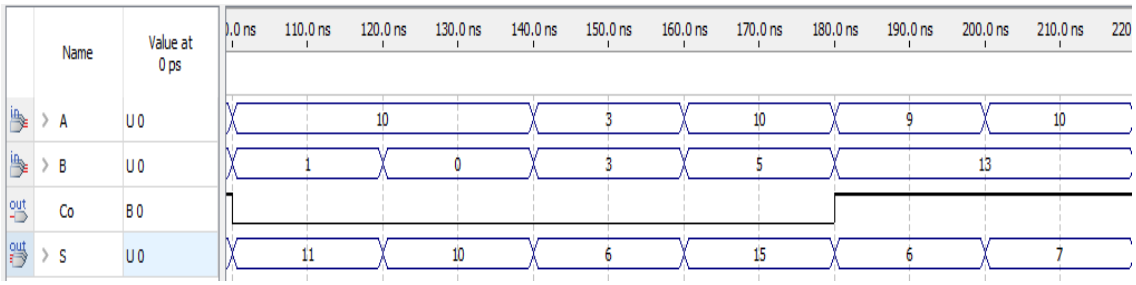
In this lab, you are asked to design three combinational circuits, **four-bit adder**, **four-bit subtractor**, and **four-bit multiplier**. You will learn how to use software tool Quartus-II to simulate your designed circuits, verify their functionality through testing patterns, and visualize the digital waveform.

Tasks

- **4-bit Adder**

Implement a 4-bit **unsigned** adder with unsigned input A[3:0], B[3:0], unsigned output S[3:0] and carry out Co. Please first design a sub-circuit of full adder, then realize a 4-bit adder by cascading 4 full adders. The block diagram and tested waveform are shown as below.

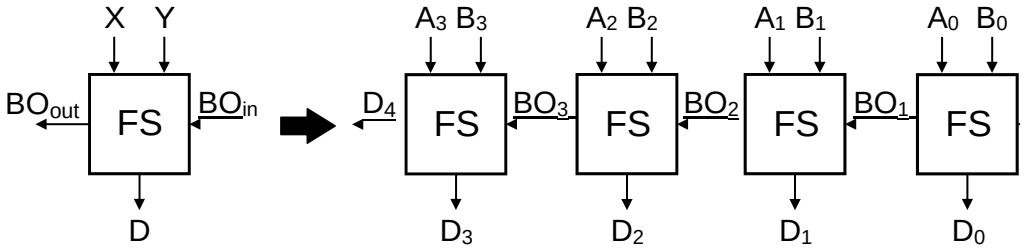




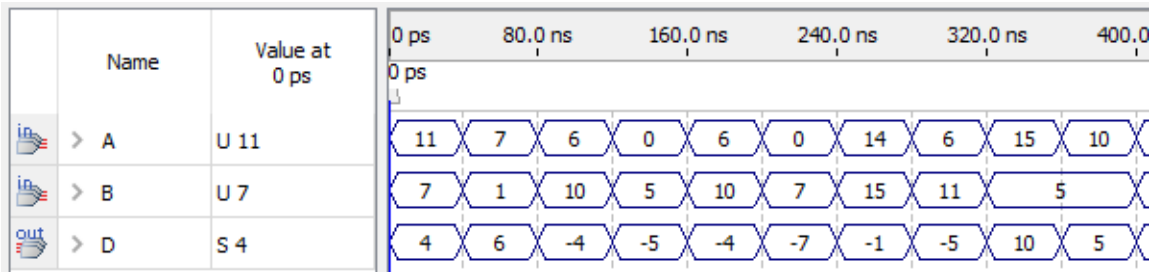
The design of this 4-bit full adder is **fully demonstrated** in tutorial file (Lab01_tutorial.pdf), and it **is totally the same** as this task. Please follow the steps and you can accomplish the task easily.

◆ 4-bit Subtractor

Implement a 4-bit subtractor with **unsigned input** A[3:0], B[3:0], and **signed output** D[4:0]. One reference design is similar to the adder design. Firstly, design a sub-circuit of full subtractor, then realize a 4-bit subtractor by cascading 4 full subtractors. The block diagram and tested waveform are shown as below.



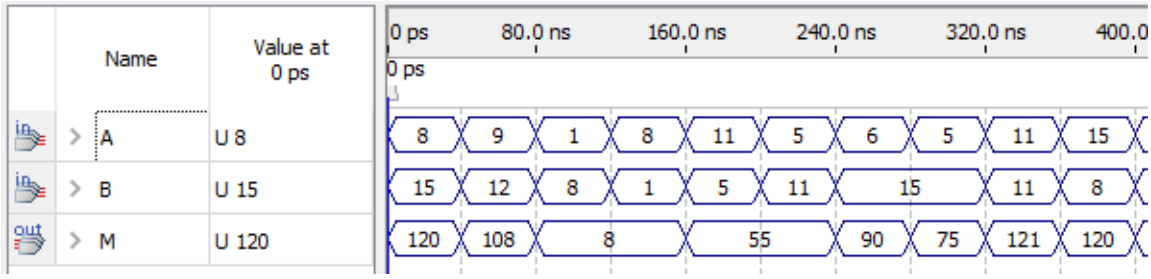
1-bit Full Subtractor (FS) 4-bit Subtractor



For this task, you are not necessary to follow the reference design provided above. **You can choose your own design, but neither the one that using the expression of A − B = A + $\bar{B}$ + 1, nor implementing with full adders.**

◆ 4-bit Multiplier

Implement a 4-bit **unsigned** multiplier with unsigned input A[3:0], B[3:0], and unsigned output M[7:0]. Due to the high similarity of bit addition in multiplication, the multiplier can be realized by an array of full adders with extra AND gates. **Please refer to how to design a multiplier.pdf for more details.** The tested waveform is shown as below.



Report

◆ Name your report as Your_Student_ID_report.pdf (e.g. b12901001_report.pdf)

◆ In your report, there must includes:

- All the figures of your designs, including sub-circuits.

  e.g. 4-bit adder → FA4.jpg and FA.jpg

  4-bit subtractor → FS4.jpg and FS.jpg

  4-bit multiplier → MU4.jpg, no need to paste FA4.jpg or FA.jpg if you have included above

  Note: If you have used more sub-circuits, please paste them all.

- Screenshot your waveform and paste them to your report for each task.

◆ You can export your designs including all sub-circuits to .jpg file or take a screenshot

See Lab01_tutorial.pdf (p.68) for more detail.

Requirements

◆ Pass the test patterns provided by TAs for correct functionality.

◆ You are restricted to use the same I/O pin name as shown above. Any violation of this rule will lead to some penalty to your score. (your total score *0.8).

e.g. 4-bit adder → Inputs: A[3:0] and B[3:0]; Output: S[3:0] and Co

4-bit subtractor → Inputs: A[3:0] and B[3:0]; Output: D[4:0]

4-bit multiplier → Inputs: A[3:0] and B[3:0]; Output: M[7:0]

◆ You can **only** use the logic gates provided by TAs to design your circuits. (i.e. Only the logic gates in NTUEE_LogicDesign_Lib folder.)

◆ **For each task, export your design including all sub modules to Verilog (.v) file.** e.g. if you have FA4.bdf and FA.bdf in your folder, you should put FA4.v and FA.v in this folder too. **See Lab01_tutorial.pdf (p.66) for more detail.**

Submission

◆ Submit your .zip file to Ceiba by the deadline (11/24).

◆ The project names of 3 tasks, please name as following:

- 4-bit adder → project name: FA4
  Contain: FA4.qpf, FA4.bdf, FA4.v and all the other sub-circuit files. (such as FA.bdf, FA.bsf, FA.v)

- 4-bit subtractor → project name: FS4
  Contain: FS4.qpf, FS4.bdf, FS4.v and all the other sub-circuit files. (such as FS.bdf, FS.bsf, FS.v)

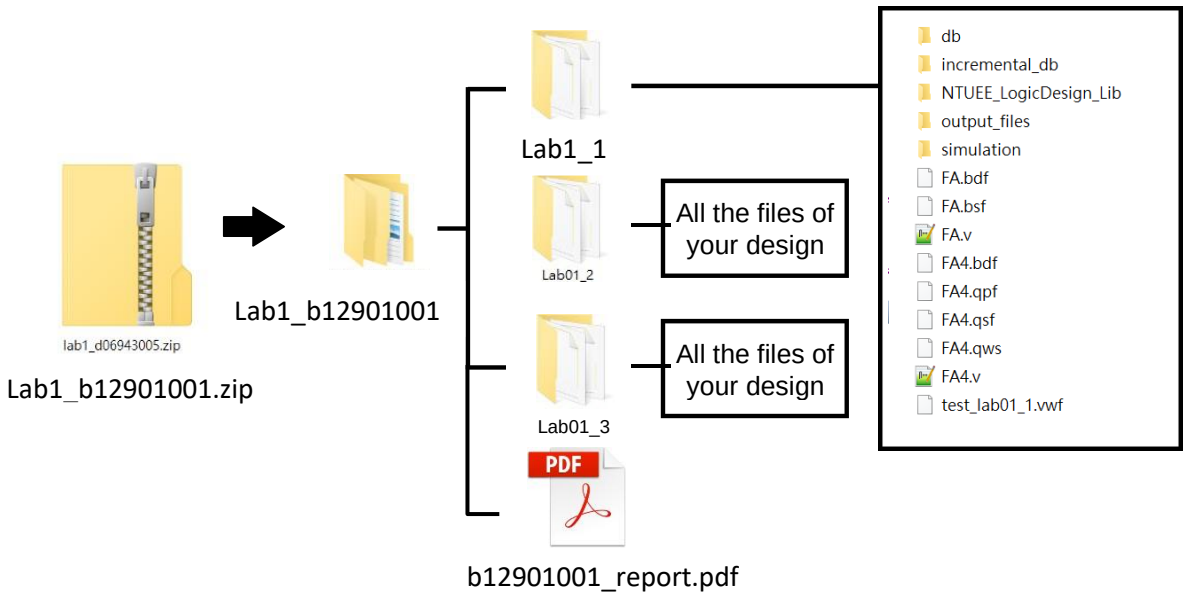
- 4-bit multiplier → project name: MU4
  Contain: MU4.qpf, MU4.bdf, MU4.v and all the other sub module file (like FA4.bdf, FA4.bsf, FA4.v)

  Note: Any violation of this naming rule will lead to some penalty to your score. (your total score *0.8). But you can use any name you want for the sub module (like FA.bdf, FA1.bdf or FullAdder1.bdf), just make sure you use the same name for all .bdf, .bsf and .v files.

◆ Please archive all the files and name as Lab1_StudentID.zip (e.g. Lab1_b12901001.zip)

◆ Your directory should be like following and put all the related files in the same folder for each task.

◆ Please follow the naming rule of folders and hierarchy indicated below, any violation of this rule will lead to some penalty to your score. (your total score *0.8)



Grading

- 4-bit adder (40%), 4-bit subtractor (40%), and 4-bit multiplier (20%).

Reminder

- Be sure you have uploaded all the required files.
- Be sure to match all the pin name, folder name and (.qpf, .bdf, .bsf, .v) files names.
- **DO NOT COPY OTHERS WORK!!! WE WILL CHECK YOUR DESIGN CAREFULLY. THOSE WHO HAVE IDENTICAL DESIGN WILL GET 0 POINT AND REPORT TO PREFESSOR.**