- Nucleo has Flash, SRAM
    - 4-Kbyte backup SRAM is an EEPROM-like memory area. It can be used to store data which need to be retained in VBAT and standby mode.
    - 20, 32-bit registers, can store 80bytes of of user data
    - Flash - 512KB
    - Embedded SRAM - 128KB
- DMA controller - two general-purpose dual-port DMAs
    - FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB)
    - Support circular buffer management
    - Double buffering feature - automate use and switching of two memory buffers
    - Can be used with peripherals - I2C, SPI, DAC, timers, ADC, etc.
- Flexible memory controller - FMC
    - even Chip Select outputs supporting the following
    - modes: SDRAM/LPSDR SDRAM, SRAM, PSRAM, NOR Flash and NAND Flash. With the possibility to remap FMC bank 1 (NOR/PSRAM 1 and 2) and FMC SDRAM bank 1/2 in the Cortex-M4 code area
    - Good to use with graphic LCD controllers - supports the Intel 8080 and Motorola 6800 modes

Using Flash as virtual EEPROM

- https://community.st.com/t5/stm32-mcus/lightweight-eeprom-emulation/ta-p/812171
- https://www.st.com/resource/en/application_note/an4894-how-to-use-eeprom-emulation-on-stm32-mcus-stmicroelectronics.pdf
- https://deepbluembedded.com/stm32-eeprom-flash-emulation-fee-read-write-examples/

Other stm32 memory stuff

- https://www.st.com/resource/en/application_note/dm00083249-use-stm32f3stm32g4-ccm-sram-with-iar-embedded-workbench-keil-mdkarm-stmicroelectronics-stm32cubeide-and-other-gnubased-toolchains-stmicroelectronics.pdf

Memory Maps

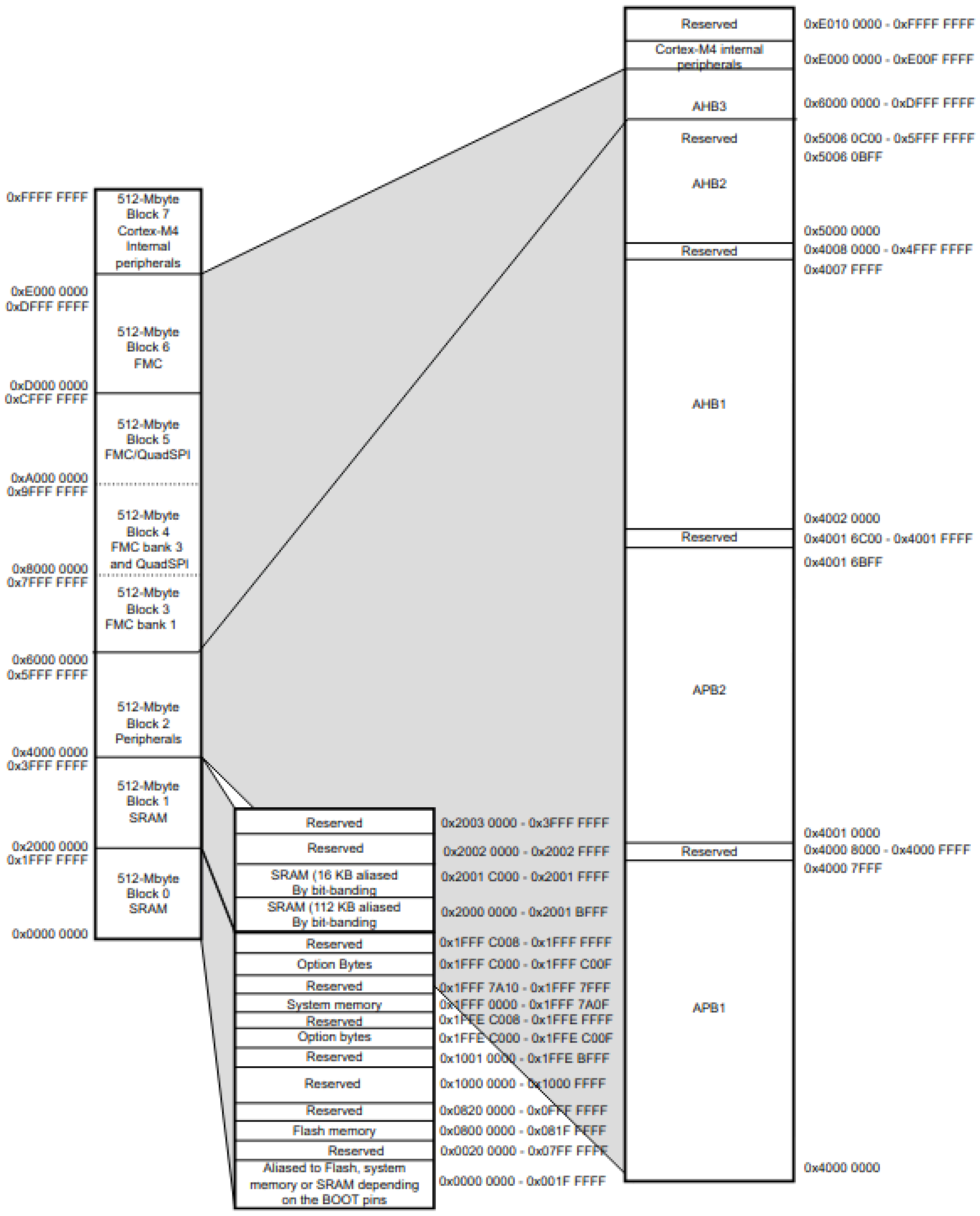
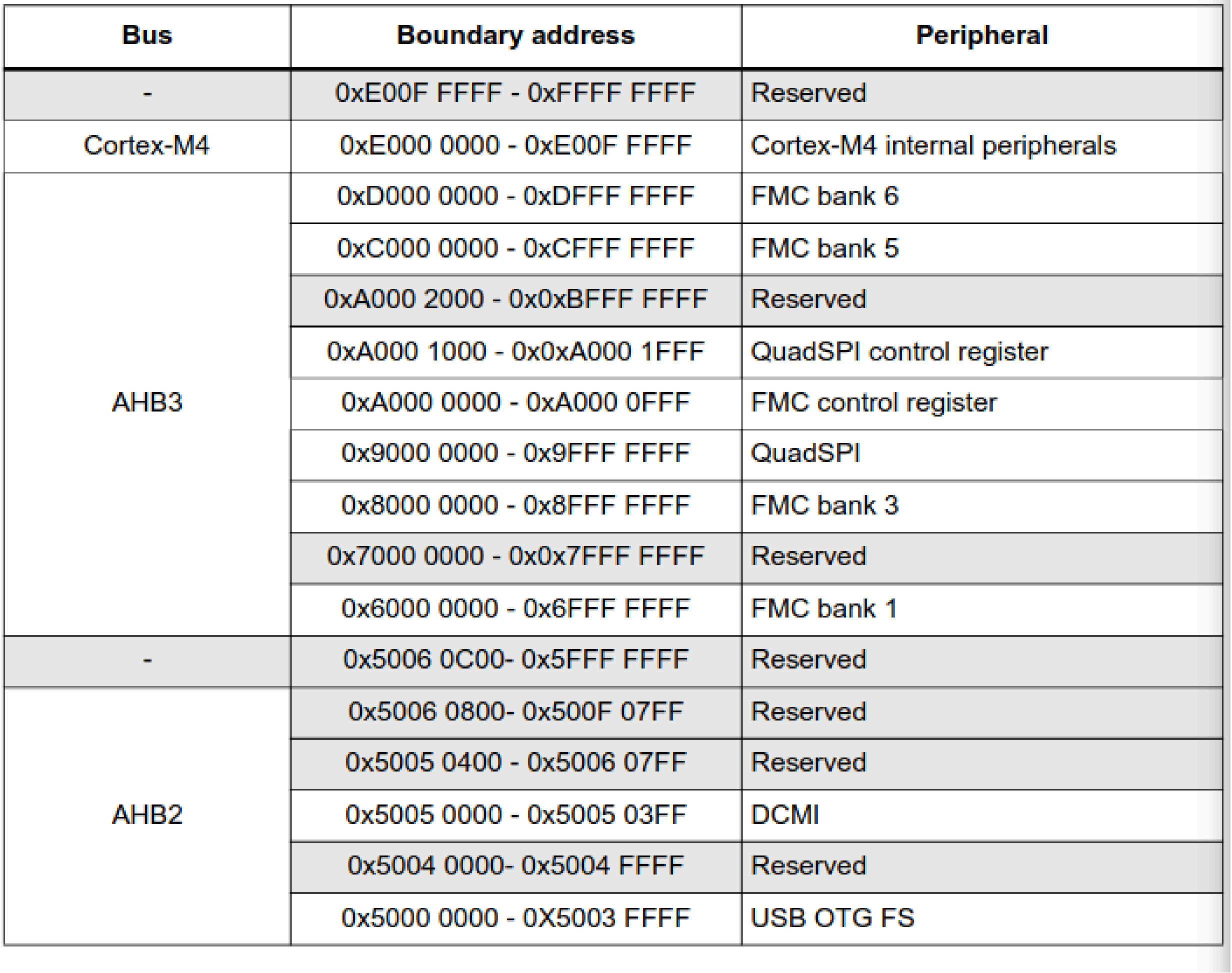

0xFFFF FFFF
512-Mbyte Block 7 Cortex-M4 Internal peripherals
0xE000 0000
0xDFFF FFFF
512-Mbyte Block 6 FMC
0xD000 0000
0xCFFF FFFF
512-Mbyte Block 5 FMC/QuadSPI
0xA000 0000
0x9FFF FFFF
512-Mbyte Block 4 FMC bank 3 and QuadSPI
0x8000 0000
0x7FFF FFFF
512-Mbyte Block 3 FMC bank 1
0x6000 0000
0x5FFF FFFF
512-Mbyte Block 2 Peripherals
0x4000 0000
0x3FFF FFFF
512-Mbyte Block 1 SRAM
0x2000 0000
0x1FFF FFFF
512-Mbyte Block 0 SRAM
0x0000 0000
Reserved
0x2003 0000 - 0x3FFF FFFF
Reserved
0x2002 0000 - 0x2002 FFFF
SRAM (16 KB aliased By bit-banding
0x2001 C000 - 0x2001 FFFF
SRAM (112 KB aliased By bit-banding
0x2000 0000 - 0x2001 BFFF
Reserved
0x1FFF C008 - 0x1FFF FFFF
Option Bytes
0x1FFF C000 - 0x1FFF C00F
Reserved
0x1FFF 7A10 - 0x1FFF 7FFF
System memory
0x1FFF 0000 - 0x1FFF 7A0F
Reserved
0x1FFE C008 - 0x1FFE FFFF
Option bytes
0x1FFE C000 - 0x1FFE C00F
Reserved
0x1001 0000 - 0x1FFE BFFF
Reserved
0x1000 0000 - 0x1000 FFFF
Reserved
0x0820 0000 - 0x0FFF FFFF
Flash memory
0x0800 0000 - 0x081F FFFF
Reserved
0x0020 0000 - 0x07FF FFFF
Aliased to Flash, system memory or SRAM depending on the BOOT pins
0x0000 0000 - 0x001F FFFF
Reserved
0xE010 0000 - 0xFFFF FFFF
Cortex-M4 internal peripherals
0xE000 0000 - 0xE00F FFFF
AHB3
0x6000 0000 - 0xDFFF FFFF
Reserved
0x5006 0C00 - 0x5FFF FFFF
0x5006 0BFF
AHB2
0x5000 0000
Reserved
0x4008 0000 - 0x4FFF FFFF
0x4007 FFFF
AHB1
0x4002 0000
Reserved
0x4001 6C00 - 0x4001 FFFF
0x4001 6BFF
APB2
0x4001 0000
Reserved
0x4000 8000 - 0x4000 FFFF
0x4000 7FFF
APB1
0x4000 0000

Table 12. STM32F446xC/E register boundary addresses[1]



Bus	Boundary address	Peripheral
-	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
AHB3	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 2000 - 0x0xBFFF FFFF	Reserved
	0xA000 1000 - 0x0xA000 1FFF	QuadSPI control register
	0xA000 0000 - 0xA000 0FFF	FMC control register
	0x9000 0000 - 0x9FFF FFFF	QuadSPI
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x0x7FFF FFFF	Reserved
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
-	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800- 0x500F 07FF	Reserved
	0x5005 0400 - 0x5006 07FF	Reserved
	0x5005 0000 - 0x5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0X5003 FFFF	USB OTG FS

Table 12. STM32F446xC/E register boundary addresses[1] (continued)

Bus	Boundary address	Peripheral
-	0x4008 0000- 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00- 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	
	0x4002 9400 - 0x4002 AFFF	
	0x4002 9000 - 0x4002 93FF	
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0X4002 5000 - 0X4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0X4002 3400 - 0X4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	
	0x4002 2400 - 0x4002 27FF	
	0x4002 2000 - 0x4002 23FF	
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0X4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Table 12. STM32F446xC/E register boundary addresses[1] (continued)

Bus	Boundary address	Peripheral
-	0x4001 6C00- 0x4001 FFFF	Reserved
APB2	0x4001 6800 - 0x4001 6BFF	
	0x4001 5C00 - 0x4001 5FFF	SAI2
	0x4001 6000 - 0x4001 67FF	Reserved
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	Reserved
	0x4001 5000 - 0x4001 53FF	
	0x4001 4C00 - 0x4001 4FFF	
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

Table 12. STM32F446xC/E register boundary addresses[1] (continued)

Bus	Boundary address	Peripheral
-	0x4000 8000- 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	
	0x4000 7800 - 0x4000 7BFF	
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	HDMI-CEC
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	FMPI2C1
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	SPDIFRX
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	Reserved
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	Reserved
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

[1] The grey color is used for reserved boundary addresses.

Planning for Memory

Settings/Configurations

- Flash as EEPRM or backup SRAM?
- Flash has a 10,000 program/erase cycle limit per sector
- DMA - will want to use to communicate with PI, sending sensor data

Using flash: https://controllerstech.com/flash-programming-in-stm32/
https://medium.com/teamarimac/stm32-flash-programming-3418bf09231c
STM32 EEPROM Emulation API