PART – A

(25 Marks)

1.a) Differentiate computer organization and architecture. [2]
b) What must the address field of an indexed addressing modes instruction be to make it the same as a registrar indirect mode instruction? [2]
c) Why should the sign of the reminder after a division be the same as the sign of the dividend? [2]
d) How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes? [2]
e) What are the various physical forms available for establishing an interconnection network? [2]
f) How many references to memory are needed for each type of instruction to bring an operand into a processor register? [3]
g) Is it possible to design a microprocessor without a micro program? Are all micro programmed computers also microprocessors? [3]
h) Represent decimal number 6027 in: i) BCD ii) excess-3. [3]
i) Why are the read and write control lines in a DMA controller bidirectional? Under what condition and for what purpose are they are they used as inputs? [3]
j) Write a short note on array processor. [3]

PART – B

(50 Marks)

2.a) Derive the control gates for the write input of the memory in the basic computer.
b) Design a 4 bit combinational circuit decrementer using four full adder circuits. [5+5]

OR

3. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.
a) How many selection inputs are there in each multiplexer?
b) What sizes of multiplexers are needed?
c) How many multiplexers are there in the bus? [10]

4.a) Make a comparison between the hardwired control and micro programmed control. Is it possible to have a hardwired control associated with a control memory?
b) Explain about Stack Organization in detail. [5+5]

OR

5.a) Draw the block diagram of micro program sequencer for a control memory and explain its operations in detail.
b) How many times does the control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is:
i) a computational type requiring an operand from memory
ii) a branch type. [5+5]

6.a) Convert the following decimal numbers to binary: 1231; 673; and 1998.
b) Show that there can be no mantissa overflow after a multiplication operation. [5+5]

OR

7. What is floating point representation? Explain the IEEE standard for floating point representation with examples. [10]

8. Explain associative memory hardware organization in detail. [10]

OR

9.a) Give a neat sketch that illustrates the components in a typical memory hierarchy.
b) A computer uses RAM chips of 1024× 1 capacity.
i) How many chips are needed, and should their address lines be connected to provide a memory capacity of 1024 bytes.
ii) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus. [5+5]

10.a) Discuss the various conflicts that might arise in a pipeline. How are they resolved?
b) Draw and explain the structure of general purpose multicomputer. [5+5]

OR

11. Consider the multiplication of two 40×40 matrices using a vector processor.
a) How many product terms are there in each inner product and how many inner products must be evaluated?
b) How many multiply add operations are needed to calculate the product matrix? [5+5]

R18

Code No: 153AG

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, March - 2021
COMPUTER ORGANIZATION AND ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) Discuss the functional units of a digital computer.
b) Demonstrate construction of a common bus system with multiplexers. [7+8]

2.a) Design a 4-bit combinational circuit decrementer using four full-adder circuits.
b) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? [7+8]

3.a) Discuss the need of memory stack and stack limits.
b) Explain the general register organization of the processor. [7+8]

4. Explain addition and subtraction of floating point numbers with an example and necessary flowchart. [15]

5.a) A two way set associative cache has lines of 16 bytes and a total size of 8 K bytes. The 64 Mbytes main memory is byte addressable. Show the format of main memory address.
b) How does SDRAM differ from ordinary DRAM? [8+7]

6.a) Explain the major differences between the central computer and peripheral. How to resolve these differences?
b) Discuss the Strobe control method of Asynchronous data transfer. [8+7]

7.a) What is parallel processing? Explain Flynn's classification of computer.
b) Illustrate vector operations and vector processing. [8+7]

8.a) Discuss about RISC Pipeline.
b) What is cache coherence problem? Discuss solutions for it. [7+8]

---ooOoo---

R18

Code No: 153AG

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, October - 2020
COMPUTER ORGANIZATION AND ARCHITECTURE
(Computer Science and Engineering)

Time: 2 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
\- - -

1.a) Draw the bus system for four registers and explain.
b) An 8-bit register contains the binary value 10011100. What is the register value after an Arithmetic Shift Right? Starting from the initial number 10011100, determine the register value after an arithmetic Shift Left, and state whether there is an overflow. [7+8]

2. Draw block diagram of a control memory and the associated hardware needed for selecting the next micro instruction address. [15]

3. Perform the arithmetic operation (+42)+(-13) and (-42)-(-13) in binary using signed 2's complement representation for negative numbers. [15]

4.a) Differentiate between Isolated I/O and memory-mapped I/O.
b) Explain programmed-I/O in detail. [8+7]

5.a) Write the major characteristics of RISC processors.
b) Draw a space-time diagram for a four-segment pipeline showing the time it takes to process six tasks and explain. [7+8]

6.a) Draw the flowchart for instruction cycle and explain.
b) Explain the following instructions: BUN, ISZ, BSA, LDA, STA. [7+8]

7. Explain various Data Manipulation instructions with examples. [15]

8. With an example, explain Booth Multiplication algorithm. [15]

---ooOoo---

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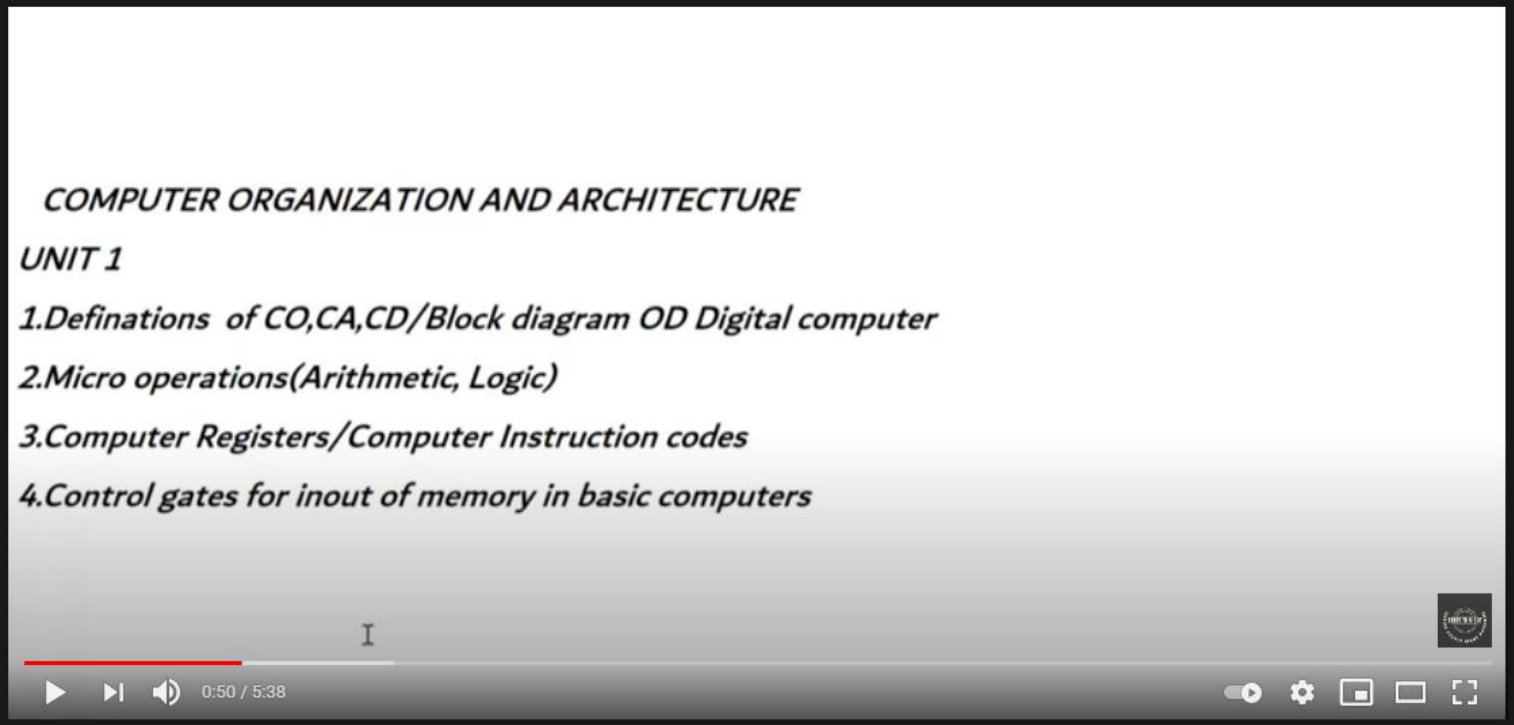

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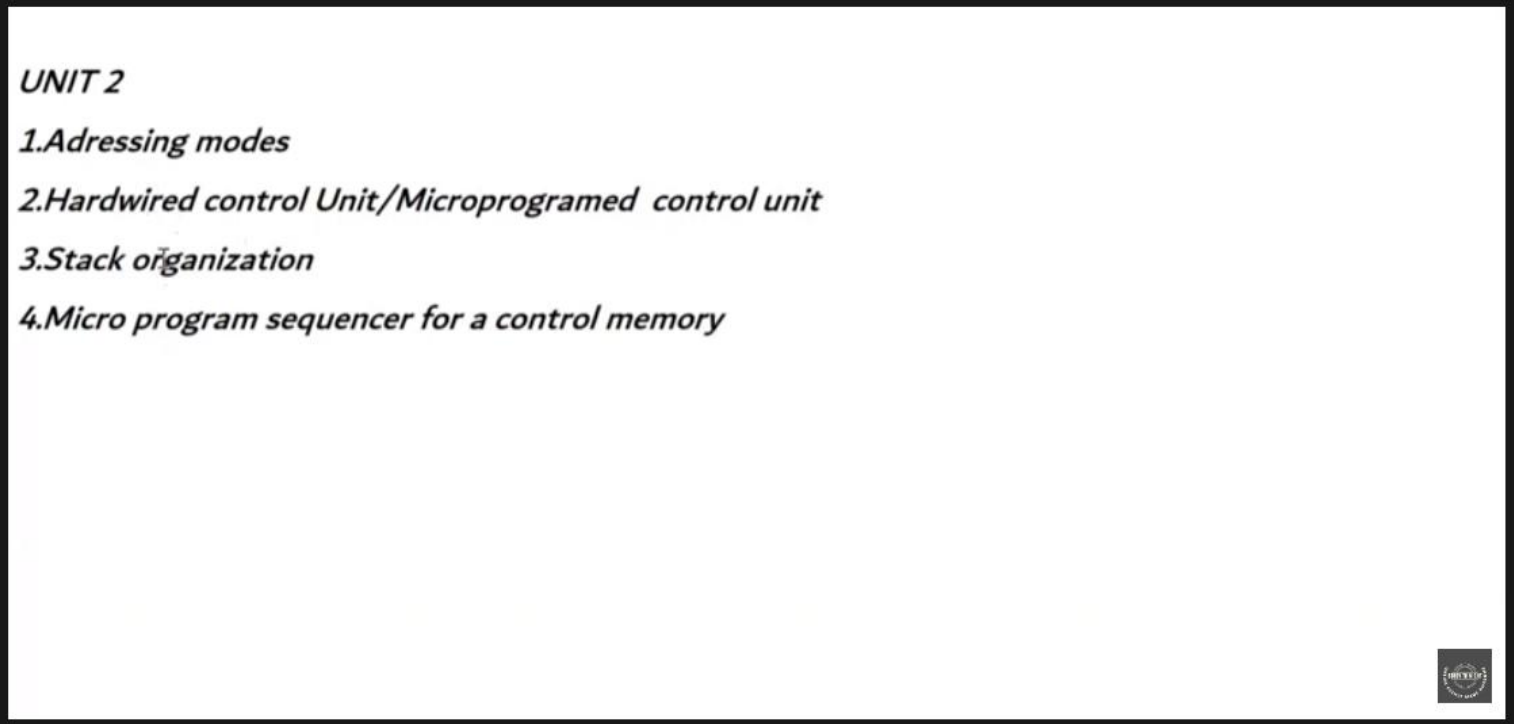

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UNIT 4

1.Asynchronous data transfer

2.Modes of Transfer/Direct memory access

3.Memory Hierarchy

Short note on Auxiliary,Associative ,Cache memory

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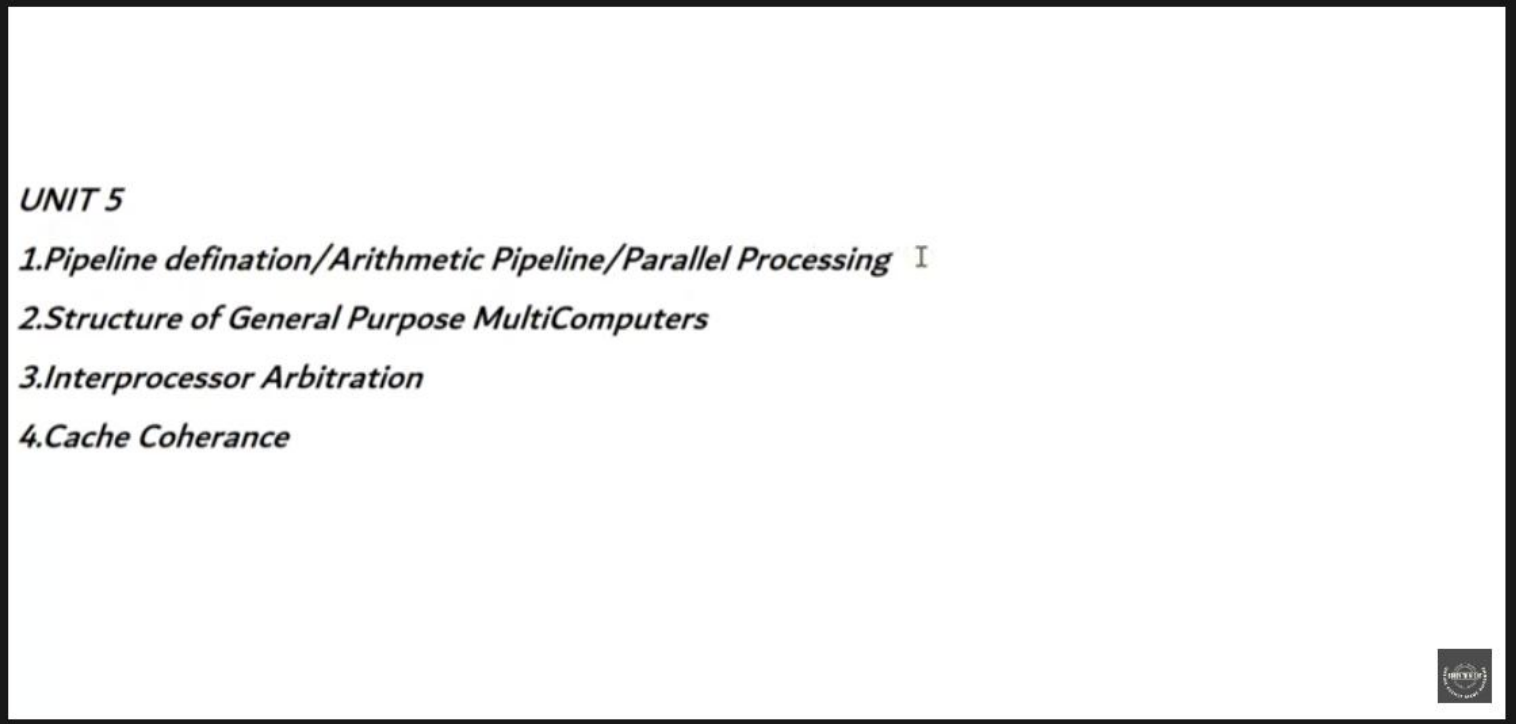

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