ECED3403 – Assignment 4

Grace Yu

B00902046

July 19th, 2024

1. Testing

1. BL branches with link

Purpose: Checks for successful implementation of BL instruction.

Configuration: The below xme file is loaded into the emulator. It uses BL to branch to another label, returning by restoring the program counter (PC), with the link register (LR).

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bl.txt
Time of assembly: Tue 30 Jul 2024 23:15:04
  1                             BP      equ     R4
  2                             LR      equ     R5
  3                             SP      equ     R6
  4                             PC      equ     R7
  5                                     org #1000
  6                     MAIN
  7     1000    0001            bl      LOOP
  8     1002    3C02            bra     DONE
  9                     LOOP
 10     1004    67F8            movl    #FF,R0          ; loop
 11     1006    4C2F            mov     LR,PC
 12                     DONE
 13     1008    3FFF            bra     DONE
 14                     end MAIN
Successful completion of assembly - 2P
```

Expected Results:	Actual Results:
The PC should change to the beginning of LOOP, at address 1004. It should then successfully set R0 to 0x00FF before returning to its place in MAIN, at address 1002, when it is restored using LR.	Start: PC: 1000 PSW: 60E0 Brkpt: 0000 Clk: 2 1000: BL OFF: 0002 R0: 0000 R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 1002 R6 (SP): 0000 R7 (PC): 1004 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 1004 Clk: 4 Option: g Start: PC: 1004 PSW: 60E0 Brkpt: 0000 Clk: 4 End: PC: 1004 Clk: 6 Option: g Start: PC: 1004 PSW: 60E0 Brkpt: 0000 Clk: 6 1004: MOVL BYTE: FF DST: R0 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 1002 R6 (SP): 0000 R7 (PC): 1006 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 1006 Clk: 8 Option: g Start: PC: 1006 PSW: 60E0 Brkpt: 0000 Clk: 8 1006: MOV WB: 0 SRC: R5 DST: R7 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 1002 R6 (SP): 0000 R7 (PC): 1002 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 1002 Clk: 10 Option: g Start: PC: 1002 PSW: 60E0 Brkpt: 0000 Clk: 10 End: PC: 1002 Clk: 12

Pass/Fail: PASS

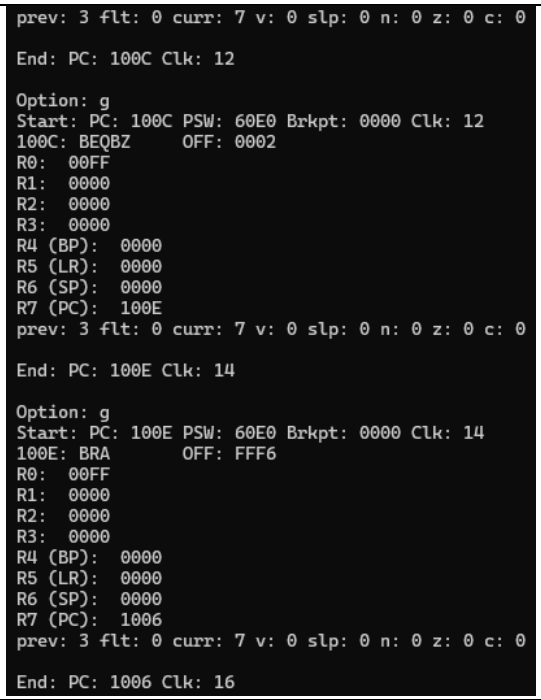
2. BEQ/BZ

Purpose: Checks for successful implementation of BEQ/BZ instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BEQ when the PSW's zero flag is both set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: beqbz.txt
Time of assembly: Wed 31 Jul 2024 09:55:13
  1                             BP      equ     R4
  2                             LR      equ     R5
  3                             SP      equ     R6
  4                             PC      equ     R7
  5                                     org #1000
  6                     MAIN
  7     1000    4DA2            setcc   z
  8     1002    2002            beq     EQUAL
  9     1004    3C00            bra     DONE
 10                     DONE
 11     1006    3FFF            bra     DONE
 12                     EQUAL
 13     1008    67F8            movl    #FF,R0          ; loop
 14     100A    4DC2            clrcc   z
 15     100C    2001            beq     UNEQUAL
 16     100E    3FFB            bra     DONE
 17                     UNEQUAL
 18     1010    67F8            movl    #FF,R0
 19     1012    3FF9            bra     DONE
 20                     end MAIN
Successful completion of assembly - 2P
```

Expected Results:	**Actual Results:**
• When BEQ is encountered with a PSW Zero flag set, it should branch to the EQUAL label and set R0 to 0x00FF. • It should not execute the BRA DONE instruction immediately after the BEQ, as the PC should change.	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 1 c: 0 End: PC: 1002 Clk: 4 Option: g Start: PC: 1002 PSW: 60E2 Brkpt: 0000 Clk: 4 1002: BEQBZ OFF: 0004 R0: 0000 R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1008 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 1 c: 0 End: PC: 1008 Clk: 6 Option: g Start: PC: 1008 PSW: 60E2 Brkpt: 0000 Clk: 6 End: PC: 1008 Clk: 8 Option: g Start: PC: 1008 PSW: 60E2 Brkpt: 0000 Clk: 8 1008: MOVL BYTE: FF DST: R0 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 100A prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 1 c: 0 End: PC: 100A Clk: 10

• When BEQ is encountered with a PSW Zero flag cleared, it should not branch to the UNEQUAL label and it should not set R0 to 0x0000. • It should execute the BRA DONE instruction immediately after the BEQ, as the PC should not change.	

Pass/Fail: PASS

3. BNE/BNZ

Purpose: Checks for successful implementation of BNE/BNZ instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BNE when the PSW's zero flag is both set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bnebnz.txt
Time of assembly: Wed 31 Jul 2024 10:03:45
  1                             BP      equ     R4
  2                             LR      equu    R5
  3                             SP      equ     R6
  4                             PC      equ     R7
  5                                     org #1000
  6                     MAIN
  7     1000    4DC2            clrcc   z
  8     1002    2402            bne     TRUE
  9     1004    3C00            bra     DONE
 10                     DONE
 11     1006    3FFF            bra     DONE
 12                     TRUE
 13     1008    67F8            movl    #FF,R0          ; loop
 14     100A    4DA2            setcc   z
 15     100C    2401            bne     FALSE
 16     100E    3FFB            bra     DONE
 17                     FALSE
 18     1010    67F8            movl    #FF,R0
 19     1012    3FF9            bra     DONE
 20                     end MAIN
Successful completion of assembly - 2P
```

Expected Results:	Actual Results:
• When BNE is encountered with a PSW Zero flag cleared, it should branch to the TRUE label and set R0 to 0x00FF. • It should not execute the BRA DONE instruction immediately after the BNE, as the PC should have changed.	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 1 c: 0 End: PC: 1002 Clk: 4 Option: g Start: PC: 1002 PSW: 60E2 Brkpt: 0000 Clk: 4 1002: BEQBZ OFF: 0004 R0: 0000 R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1008 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 1 c: 0 End: PC: 1008 Clk: 6 Option: g Start: PC: 1008 PSW: 60E2 Brkpt: 0000 Clk: 6 End: PC: 1008 Clk: 8 Option: g Start: PC: 1008 PSW: 60E2 Brkpt: 0000 Clk: 8 1008: MOVL BYTE: FF DST: R0 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 100A prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 1 c: 0 End: PC: 100A Clk: 10
• When BNE is encountered with a PSW Zero flag set, it should not branch to the FALSE label and it should not set R0 to 0x0000. • It should execute the BRA DONE instruction immediately after the BNE, as the PC should not have changed.	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 100C Clk: 12 Option: g Start: PC: 100C PSW: 60E0 Brkpt: 0000 Clk: 12 100C: BEQBZ OFF: 0002 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 100E prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 100E Clk: 14 Option: g Start: PC: 100E PSW: 60E0 Brkpt: 0000 Clk: 14 100E: BRA OFF: FFF6 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1006 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 1006 Clk: 16

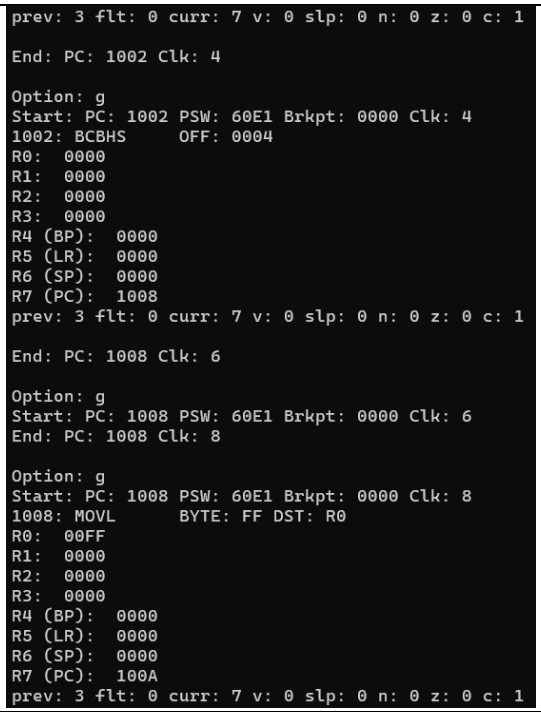
Pass/Fail: PASS

4. BC/BHS

Purpose: Checks for successful implementation of BC/BHS instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BC when the PSW's carry flag is both set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bcbhs.txt
Time of assembly: Wed 31 Jul 2024 10:19:18
  1                             BP      equ     R4
  2                             LR      equ     R5
  3                             SP      equ     R6
  4                             PC      equ     R7
  5                                     org #1000
  6                     MAIN
  7     1000    4DA1            setcc   c
  8     1002    2802            bc      TRUE
  9     1004    3C00            bra     DONE
 10                     DONE
 11     1006    3FFF            bra     DONE
 12                     TRUE
 13     1008    67F8            movl    #FF,R0          ; loop
 14     100A    4DC1            clrcc   c
 15     100C    2801            bc      FALSE
 16     100E    3FFB            bra     DONE
 17                     FALSE
 18     1010    67F8            movl    #FF,R0
 19     1012    3FF9            bra     DONE
 20                     end MAIN
Successful completion of assembly - 2P
```

Expected Results:	**Actual Results:**
• When BC is encountered with a PSW Carry flag set, it should branch to the TRUE label and set R0 to 0x00FF. • It should not execute the BRA DONE instruction immediately after the BC, as the PC should have changed.	

• When BC is encountered with a PSW Zero flag set, it should not branch to the FALSE label and it should not set R0 to 0x0000. • It should execute the BRA DONE instruction immediately after the BC, as the PC should not have changed.	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 100C Clk: 12 Option: g Start: PC: 100C PSW: 60E0 Brkpt: 0000 Clk: 12 100C: BCBHS OFF: 0002 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 100E prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 100E Clk: 14 Option: g Start: PC: 100E PSW: 60E0 Brkpt: 0000 Clk: 14 100E: BRA OFF: FFF6 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1006 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0

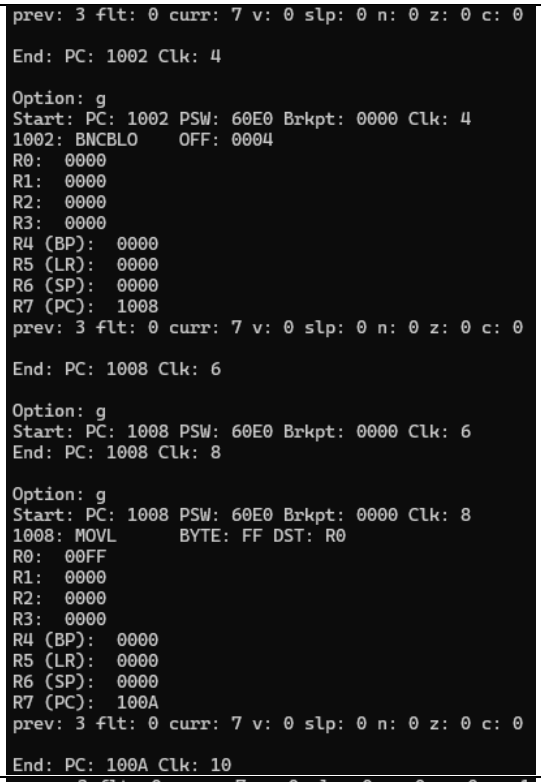
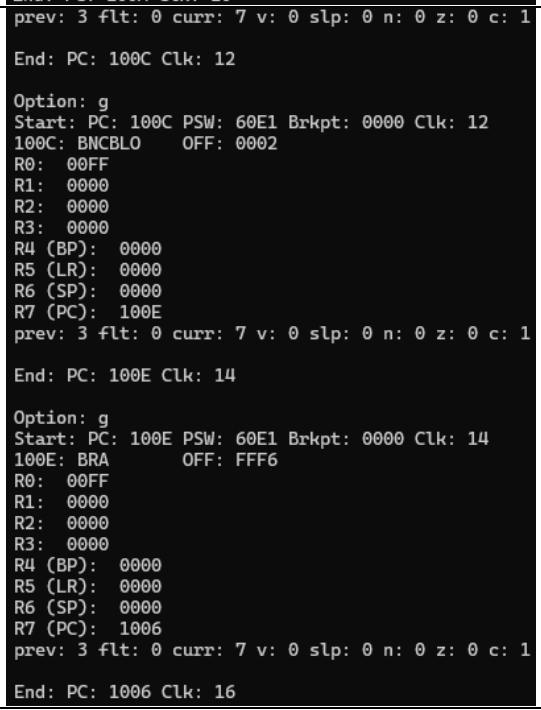
Pass/Fail: PASS

5. BNC/BLO

Purpose: Checks for successful implementation of BNC/BLO instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BNC when the PSW's Carry flag is both set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bncblo.txt
Time of assembly: Wed 31 Jul 2024 10:25:20
  1                             BP      equ     R4
  2                             LR      equ     R5
  3                             SP      equ     R6
  4                             PC      equ     R7
  5                                     org #1000
  6                     MAIN
  7     1000    4DC1            clrcc   c
  8     1002    2C02            bnc     TRUE
  9     1004    3C00            bra     DONE
 10                     DONE
 11     1006    3FFF            bra     DONE
 12                     TRUE
 13     1008    67F8            movl    #FF,R0          ; loop
 14     100A    4DA1            setcc   c
 15     100C    2C01            bnc     FALSE
 16     100E    3FFB            bra     DONE
 17                     FALSE
 18     1010    67F8            movl    #FF,R0
 19     1012    3FF9            bra     DONE
 20                     end MAIN
Successful completion of assembly - 2P
```

Expected Results:	Actual Results:
• When BNC is encountered with a PSW Carry flag cleared, it should branch to the TRUE label and set R0 to 0x00FF. • It should not execute the BRA DONE instruction immediately after the BNC, as the PC should have changed.	
• When BNC is encountered with a PSW Carry flag set, it should not branch to the FALSE label and it should not set R0 to 0x0000. • It should execute the BRA DONE instruction immediately after the BNC, as the PC should not have changed.	

Pass/Fail: PASS

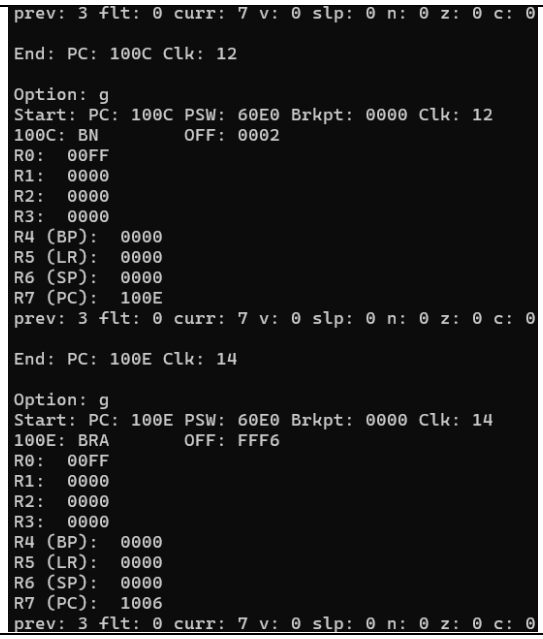
6. BN

Purpose: Checks for successful implementation of BN instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BN when the PSW's Negative flag is both set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bn.txt
Time of assembly: Wed 31 Jul 2024 10:43:47
  1                             BP      equ     R4
  2                             LR      equ     R5
  3                             SP      equ     R6
  4                             PC      equ     R7
  5                                     org #1000
  6                     MAIN
  7     1000    4DA4            setcc   n
  8     1002    3002            bn      TRUE
  9     1004    3C00            bra     DONE
 10                     DONE
 11     1006    3FFF            bra     DONE
 12                     TRUE
 13     1008    67F8            movl    #FF,R0          ; loop
 14     100A    4DC4            clrcc   n
 15     100C    3001            bn      FALSE
 16     100E    3FFB            bra     DONE
 17                     FALSE
 18     1010    67F8            movl    #FF,R0
 19     1012    3FF9            bra     DONE
 20                     end MAIN
Successful completion of assembly - 2P
```

Expected Results:	**Actual Results:**
• When BN is encountered with a PSW Negative flag set, it should branch to the TRUE label and set R0 to 0x00FF. • It should not execute the BRA DONE instruction immediately after the BN, as the PC should have changed.	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 End: PC: 1002 Clk: 4 Option: g Start: PC: 1002 PSW: 60E4 Brkpt: 0000 Clk: 4 1002: BN OFF: 0004 R0: 0000 R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1008 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 End: PC: 1008 Clk: 6 Option: g Start: PC: 1008 PSW: 60E4 Brkpt: 0000 Clk: 6 End: PC: 1008 Clk: 8 Option: g Start: PC: 1008 PSW: 60E4 Brkpt: 0000 Clk: 8 1008: MOVL BYTE: FF DST: R0 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 100A prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0

• When BN is encountered with a PSW Negative flag cleared, it should not branch to the FALSE label and it should not set R0 to 0x0000. • It should execute the BRA DONE instruction immediately after the BN, as the PC should not have changed.	

```
prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0

End: PC: 100C Clk: 12

Option: g
Start: PC: 100C PSW: 60E0 Brkpt: 0000 Clk: 12
100C: BN        OFF: 0002
R0:  00FF
R1:  0000
R2:  0000
R3:  0000
R4 (BP):  0000
R5 (LR):  0000
R6 (SP):  0000
R7 (PC):  100E
prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0

End: PC: 100E Clk: 14

Option: g
Start: PC: 100E PSW: 60E0 Brkpt: 0000 Clk: 14
100E: BRA       OFF: FFF6
R0:  00FF
R1:  0000
R2:  0000
R3:  0000
R4 (BP):  0000
R5 (LR):  0000
R6 (SP):  0000
R7 (PC):  1006
prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0
```

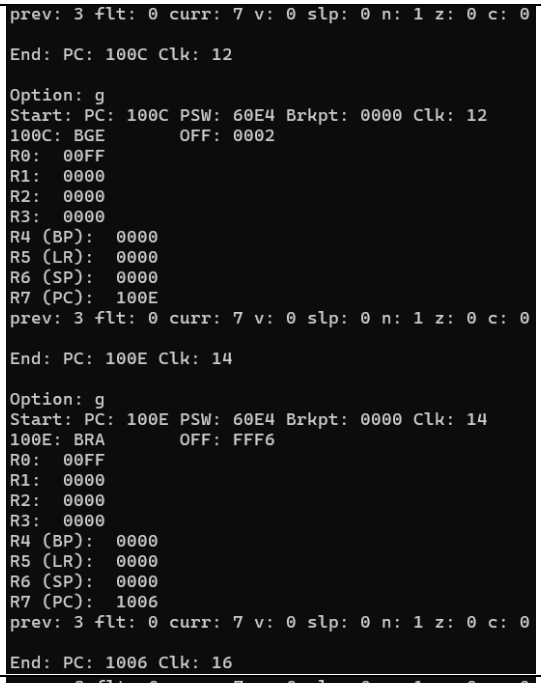
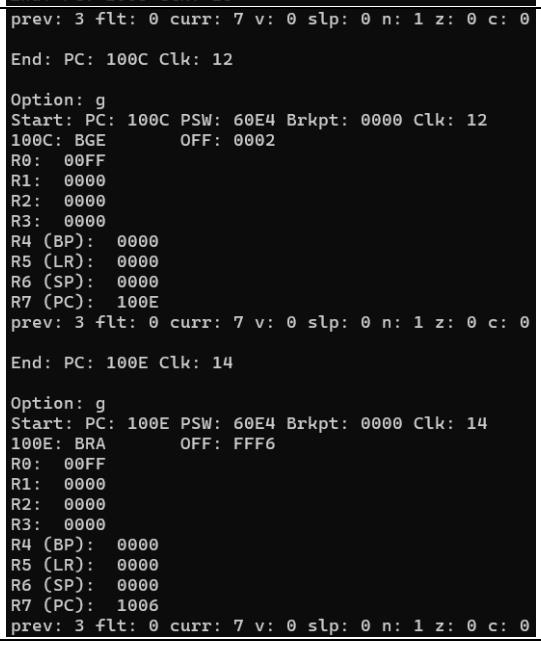
Pass/Fail: PASS

7. BGE

Purpose: Checks for successful implementation of BGE instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BGE when the PSW's Negative and oVerflow flags are set and cleared

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bge.txt
Time of assembly: Wed 31 Jul 2024 10:51:52
  1                             BP      equ     R4
  2                             LR      equ     R5
  3                             SP      equ     R6
  4                             PC      equ     R7
  5                                     org #1000
  6                     MAIN
  7     1000    4DB4            setcc   nv
  8     1002    3402            bge     TRUE
  9     1004    3C00            bra     DONE
 10                     DONE
 11     1006    3FFF            bra     DONE
 12                     TRUE
 13     1008    67F8            movl    #FF,R0          ; loop
 14     100A    4DD0            clrcc   v
 15     100C    3401            bge     FALSE
 16     100E    3FFB            bra     DONE
 17                     FALSE
 18     1010    6000            movl    #00,R0
 19     1012    3FF9            bra     DONE
 20                     end MAIN
Successful completion of assembly - 2P
```

Expected Results:	Actual Results:
• When BGE is encountered with a PSW Negative flag set and oVerflow flag set, it should branch to the TRUE label and set R0 to 0x00FF. • It should not execute the BRA DONE instruction immediately after the BGE, as the PC should have changed.	
• When BGE is encountered with a PSW Negative flag set and oVerflow flag cleared, it should not branch to the FALSE label and it should not set R0 to 0x0000. • It should execute the BRA DONE instruction immediately after the BGE, as the PC should not have changed.	

Pass/Fail: PASS

8. BLT

Purpose: Checks for successful implementation of BLT instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BLT when the PSW's Negative flag and oVerflow flag are set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: beqbz.txt
Time of assembly: Wed 31 Jul 2024 09:55:13
  1                             BP      equ     R4
  2                             LR      equu    R5
  3                             SP      equ     R6
  4                             PC      equ     R7
  5                                     org #1000
  6                     MAIN
  7     1000    4DA2            setcc   z
  8     1002    2002            beq     EQUAL
  9     1004    3C00            bra     DONE
 10                     DONE
 11     1006    3FFF            bra     DONE
 12                     EQUAL
 13     1008    67F8            movl    #FF,R0          ; loop
 14     100A    4DC2            clrcc   z
 15     100C    2001            beq     UNEQUAL
 16     100E    3FFB            bra     DONE
 17                     UNEQUAL
 18     1010    67F8            movl    #FF,R0
 19     1012    3FF9            bra     DONE
 20                     end MAIN
Successful completion of assembly - 2P
```

Expected Results:	**Actual Results:**
• When BLT is encountered with a PSW Negative flag set and oVerflow flag cleared, it should branch to the TRUE label and set R0 to 0x00FF. • It should not execute the BRA DONE instruction immediately after the BLT, as the PC should have changed.	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 End: PC: 1002 Clk: 4 Option: g Start: PC: 1002 PSW: 60E4 Brkpt: 0000 Clk: 4 1002: BLT OFF: 0004 R0: 0000 R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1008 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 End: PC: 1008 Clk: 6 Option: g Start: PC: 1008 PSW: 60E4 Brkpt: 0000 Clk: 6 End: PC: 1008 Clk: 8 Option: g Start: PC: 1008 PSW: 60E4 Brkpt: 0000 Clk: 8 1008: MOVL BYTE: FF DST: R0 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 100A prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 End: PC: 100A Clk: 10

• When BLT is encountered with a PSW Negative flag set and oVerlow flag set, it should not branch to the FALSE label and it should not set R0 to 0x0000. • It should execute the BRA DONE instruction immediately after the BGE, as the PC should not have changed.	prev: 3 flt: 0 curr: 7 v: 1 slp: 0 n: 1 z: 0 c: 0 End: PC: 100C Clk: 12 Option: g Start: PC: 100C PSW: 60F4 Brkpt: 0000 Clk: 12 100C: BLT OFF: 0002 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 100E prev: 3 flt: 0 curr: 7 v: 1 slp: 0 n: 1 z: 0 c: 0 End: PC: 100E Clk: 14 Option: g Start: PC: 100E PSW: 60F4 Brkpt: 0000 Clk: 14 100E: BRA OFF: FFF6 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1006 prev: 3 flt: 0 curr: 7 v: 1 slp: 0 n: 1 z: 0 c: 0 End: PC: 1006 Clk: 16

Pass/Fail: PASS

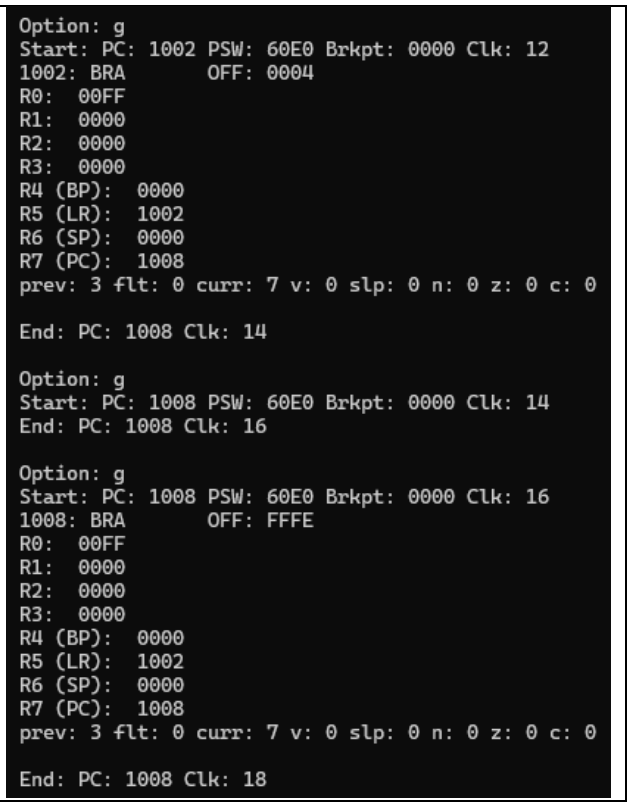
9. BRA always branches

Purpose: Checks for successful implementation of BRA instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BRA instruction to continuously branch to the label DONE, creating a loop.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bl.txt
Time of assembly: Tue 30 Jul 2024 23:15:04
  1                             BP      equ     R4
  2                             LR      equu    R5
  3                             SP      equ     R6
  4                             PC      equ     R7
  5                                     org #1000
  6                     MAIN
  7     1000    0001            bl      LOOP
  8     1002    3C02            bra     DONE
  9                     LOOP
 10     1004    67F8            movl    #FF,R0          ; loop
 11     1006    4C2F            mov     LR,PC
 12                     DONE
 13     1008    3FFF            bra     DONE
 14                     end MAIN
Successful completion of assembly - 2P
```

Expected Results:	Actual Results:

Within LOOP, when the BRA command is encountered it sends the PC back to the beginning of LOOP.	

Pass/Fail: PASS