ECED3403 – Assignment 4

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1. Testing

1. BL branches with link

Purpose: Checks for successful implementation of BL instruction.

Configuration: The below xme file is loaded into the emulator. It uses BL to branch to another label, returning by restoring the program counter (PC), with the link register (LR).

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bl.txt
Time of assembly: Tue 30 Jul 2024 23:15:04
                                        equ
                                                 R4
                                LR
                                                R5
                                        equ
  3
                                SP
                                        equ
                                                R6
                                PC
                                        equ
                                        org #1000
  6
                        MAIN
        1000
                0001
                                bl
                                        LOOP
  8
        1002
                3C02
                                        DONE
                                bra
                        LOOP
  9
 10
        1004
                67F8
                                         #FF,R0
                                                         ; loop
        1006
 11
                4C2F
                                        LR,PC
                                mov
                        DONE
 12
 13
        1008
                                        DONE
 14
                        end MAIN
Successful completion of assembly - 2P
```

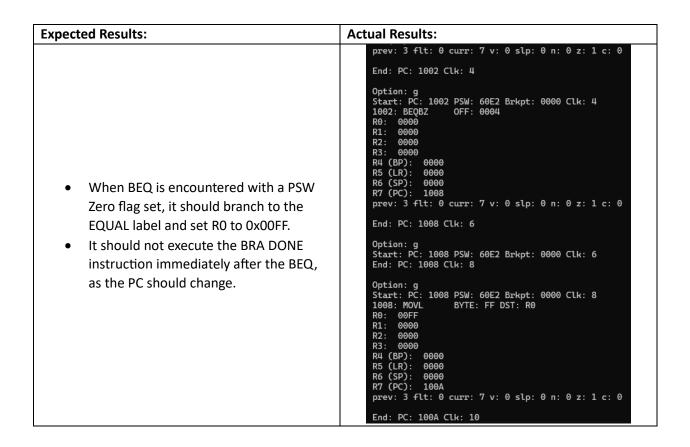
Expected Results:	Actual Results:
The PC should change to the beginning of LOOP, at address 1004. It should then successfully set R0 to 0x00FF before returning to its place in MAIN, at address 1002, when it is restored using LR.	Start: PC: 1000 PSW: 60E0 Brkpt: 0000 Clk: 2 1000: BL
	R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 1002 R6 (SP): 0000 R7 (PC): 1002 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 1002 Clk: 10
	Option: g Start: PC: 1002 PSW: 60E0 Brkpt: 0000 Clk: 10 End: PC: 1002 Clk: 12

2. BEQ/BZ

Purpose: Checks for successful implementation of BEQ/BZ instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BEQ when the PSW's zero flag is both set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: beqbz.txt
Time of assembly: Wed 31 Jul 2024 09:55:13
                                                    R4
                                  BP
                                           equ
                                  LR
                                                    R5
                                           equ
                                  SP
                                                    R6
  3
                                           eau
  4
                                  PC
                                                    R7
                                           equ
                                           org #1000
  5
                         MAIN
  6
        1000
                 4DA2
                                  setcc
  8
        1002
                 2002
                                           EQUAL
                                  beq
        1004
                 3C00
                                  bra
                                           DONE
 10
                         DONE
 11
        1006
                 3FFF
                                           DONE
                          EQUAL
 12
 13
        1008
                 67F8
                                           #FF,R0
                                                            ; loop
        100A
                 4DC2
                                  clrcc
 15
        100C
                 2001
                                           UNEQUAL
                                   beq
 16
        100E
                 3FFB
                                           DONE
 17
                         UNEQUAL
                 67F8
 18
        1010
                                  mov1
                                           #FF,R0
 19
        1012
                 3FF9
                                  bra
                                           DONE
 20
                         end MAIN
Successful completion of assembly - 2P
```



- When BEQ is encountered with a PSW
 Zero flag cleared, it should not branch to
 the UNEQUAL label and it should not set
 R0 to 0x0000.
- It should execute the BRA DONE instruction immediately after the BEQ, as the PC should not change.

```
prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0
End: PC: 100C Clk: 12
Option: g
Start: PC: 100C PSW: 60E0 Brkpt: 0000 Clk: 12
100C: BEQBZ OFF: 0002
      00FF
R1:
     0000
R2:
      0000
R3:
      0000
R4 (BP):
R5 (LR):
R6 (SP):
            0000
            0000
R7 (PC): 100E
prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0
End: PC: 100E Clk: 14
Option: g
Start: PC: 100E PSW: 60E0 Brkpt: 0000 Clk: 14
100E: BRA OFF: FFF6
R0:
      00FF
   (BP):
   (LR):
   (PC):
           1006
prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0
End: PC: 1006 Clk: 16
```

3. BNE/BNZ

Purpose: Checks for successful implementation of BNE/BNZ instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BNE when the PSW's zero flag is both set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bnebnz.txt
Time of assembly: Wed 31 Jul 2024 10:03:45
                                BP
                                LR
                                                 R5
                                         equ
                                SP
                                         equ
                                                 R6
 4
                                PC
                                         equ
                                        org #1000
                        MAIN
        1000
                4DC2
                                clrcc
        1002
                2402
                                bne
                                         TRUE
        1004
                3C00
                                bra
                                        DONE
 10
                        DONE
 11
        1006
                3FFF
                                bra
                                        DONE
                        TRUE
                67F8
 13
        1008
                                movl
                                        #FF,R0
                                                         ; loop
 14
        100A
                4DA2
                                setcc
                                         FALSE
15
        100C
                2401
                                bne
16
        100E
                3FFB
                                bra
                                        DONE
17
                        FALSE
                67F8
18
        1010
                                mov1
                                         #FF,R0
19
        1012
                3FF9
                                bra
                                        DONE
                        end MAIN
20
Successful completion of assembly - 2P
```

Expected Results:	Actual Results:
 When BNE is encountered with a PSW Zero flag cleared, it should branch to the TRUE label and set R0 to 0x00FF. It should not execute the BRA DONE instruction immediately after the BNE, as the PC should have changed. 	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 1 c: 0 End: PC: 1002 Clk: 4 Option: g Start: PC: 1002 PSW: 60E2 Brkpt: 0000 Clk: 4 1002: BEQBZ OFF: 0004 R0: 0000 R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1008 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 1 c: 0 End: PC: 1008 Clk: 6 Option: g Start: PC: 1008 PSW: 60E2 Brkpt: 0000 Clk: 6 End: PC: 1008 Clk: 8 Option: g Start: PC: 1008 PSW: 60E2 Brkpt: 0000 Clk: 8 1008: MOVL BYTE: FF DST: R0 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 100A prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 1 c: 0 End: PC: 100A Clk: 10
 When BNE is encountered with a PSW Zero flag set, it should not branch to the FALSE label and it should not set R0 to 0x0000. It should execute the BRA DONE instruction immediately after the BNE, as the PC should not have changed. 	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 100C Clk: 12 Option: g Start: PC: 100C PSW: 60E0 Brkpt: 0000 Clk: 12 100C: BEQBZ OFF: 0002 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R7 (PC): 100E prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 100E Clk: 14 Option: g Start: PC: 100E PSW: 60E0 Brkpt: 0000 Clk: 14 100E: BRA OFF: FFF6 R0: 00FF R1: 0000 R2: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R7 (PC): 1006 PF (SP): 0000 R7 (PC): 1006 PF (SP): 0000 R7 (PC): 1006 PF (SP): 0000 R7 (PC): 1006 PF (PC: 1006 Clk: 16

4. BC/BHS

Purpose: Checks for successful implementation of BC/BHS instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BC when the PSW's carry flag is both set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bcbhs.txt
Time of assembly: Wed 31 Jul 2024 10:19:18
                                                R4
                                        eau
                                LR
                                                R5
                                        equ
                                SP
                                                R6
 3
                                        eau
  4
                                PC
                                                R7
                                        equ
                                        org #1000
 5
                        MAIN
  6
                4DA1
       1000
                                setcc
  8
       1002
                2802
                                bc
                                        TRUE
       1004
                3C00
                                bra
                                        DONE
 10
                        DONE
       1006
                3FFF
                                        DONE
 11
 12
        1008
                67F8
                                movl
                                        #FF,R0
                                                        ; loop
 13
       100A
                4DC1
                                clrcc
        100C
                2801
                                        FALSE
                                bc
                                        DONE
 17
                        FALSE
       1010
                67F8
                                movl
                                        #FF,R0
 19
       1012
               3FF9
                                bra
                                        DONE
                        end MAIN
Successful completion of assembly - 2P
```

Expected Results: Actual Results: prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 1 End: PC: 1002 Clk: 4 Option: g R0: 0000 0000 R1: R2: 0000 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1008 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 1 When BC is encountered with a PSW Carry flag set, it should branch to the TRUE label and set R0 to 0x00FF. End: PC: 1008 Clk: 6 It should not execute the BRA DONE Option: g Start: PC: 1008 PSW: 60E1 Brkpt: 0000 Clk: 6 End: PC: 1008 Clk: 8 instruction immediately after the BC, as the PC should have changed. Option: g Start: PC: 1008 PSW: 60E1 Brkpt: 0000 Clk: 8 1008: MOVL BYTE: FF DST: R0 R0: 00FF R1: 0000 R2: 0000 0000 R4 (BP): R5 (LR): R6 (SP): R7 (PC): 0000 0000 100A flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 1

- When BC is encountered with a PSW
 Zero flag set, it should not branch to the
 FALSE label and it should not set R0 to
 0x0000.
- It should execute the BRA DONE instruction immediately after the BC, as the PC should not have changed.

```
rev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c:
End: PC: 100C Clk: 12
Option: g
Start: PC: 100C PSW: 60E0 Brkpt: 0000 Clk: 12
100C: BCBHS OFF: 0002
R0:
       00FF
       0000
R1:
R2:
       0000
       0000
R3:
R3: 0000
R4 (BP): 0000
R5 (LR): 0000
R6 (SP): 0000
R7 (PC): 100E
prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0
End: PC: 100E Clk: 14
Option: g
Start: PC: 100E PSW: 60E0 Brkpt: 0000 Clk: 14
100E: BRA OFF: FFF6
R0: 00FF
       0000
       0000
R3:
       0000
    (BP):
(LR):
              0000
              0000
              0000
            flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0
```

5. BNC/BLO

Purpose: Checks for successful implementation of BNC/BLO instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BNC when the PSW's Carry flag is both set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bncblo.txt
Time of assembly: Wed 31 Jul 2024 10:25:20
                                         equ
                                 LR
                                                 R5
                                         equ
                                 SP
                                         equ
                                                 R6
 4
                                 PC
                                         equ
                                         org #1000
                        MAIN
        1000
                4DC1
                                 clrcc
        1002
                2C02
                                         TRUE
        1004
                3C00
                                         DONE
 10
                        DONE
 11
        1006
                3FFF
                                         DONE
 12
                        TRUE
 13
        1008
                67F8
                                 movl
                                         #FF,R0
                                                          ; loop
 14
        100A
                4DA1
                                 setcc
 15
        100C
                2C01
                                 bnc
                                         FALSE
 16
        100E
                3FFB
                                         DONE
 17
                        FALSE
                67F8
 18
        1010
                                 mov1
                                         #FF,R0
 19
        1012
                3FF9
                                 bra
                                         DONE
20
                        end MAIN
Successful completion of assembly - 2P
```

Expected Results:	Actual Results:
 When BNC is encountered with a PSW Carry flag cleared, it should branch to the TRUE label and set R0 to 0x00FF. It should not execute the BRA DONE instruction immediately after the BNC, as the PC should have changed. 	Prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 1002 Clk: 4 Option: g Start: PC: 1002 PSW: 60E0 Brkpt: 0000 Clk: 4 1002: BNCBLO OFF: 0004 R0: 0000 R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1008 Prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 1008 Clk: 6 Option: g Start: PC: 1008 PSW: 60E0 Brkpt: 0000 Clk: 6 End: PC: 1008 Clk: 8 Option: g Start: PC: 1008 PSW: 60E0 Brkpt: 0000 Clk: 8 1008: MOVL BYTE: FF DST: R0 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 100A Prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 End: PC: 100A Clk: 10
 When BNC is encountered with a PSW Carry flag set, it should not branch to the FALSE label and it should not set R0 to 0x0000. It should execute the BRA DONE instruction immediately after the BNC, as the PC should not have changed. 	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 1 End: PC: 100C Clk: 12 Option: g Start: PC: 100C PSW: 60E1 Brkpt: 0000 Clk: 12 100C: BNCBLO OFF: 0002 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R7 (PC): 100E prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 1 End: PC: 100E Clk: 14 Option: g Start: PC: 100E PSW: 60E1 Brkpt: 0000 Clk: 14 100E: BRA OFF: FFF6 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R5 (LR): 0000 R7 (PC): 1006 Clk: 14 End: PC: 1006 Clk: 16

6. BN

Purpose: Checks for successful implementation of BN instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BN when the PSW's Negative flag is both set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bn.txt
Time of assembly: Wed 31 Jul 2024 10:43:47
                                                R4
                                        eau
                                LR
                                                R5
                                        equ
 3
                                SP
                                                R6
                                        eau
                                PC
                                                R7
                                        equ
                                        org #1000
 5
                        MAIN
       1000
                4DA4
                                setcc
                                        n
       1002
                3002
                                bn
                                        TRUE
       1004
                3C00
                                bra
                                        DONE
                        DONE
 10
       1006
                3FFF
                                        DONE
 11
12
       1008
                67F8
                                movl
                                        #FF,R0
                                                        ; loop
 13
       100A
                4DC4
                                clrcc
       100C
                3001
                                        FALSE
                                bn
               3FFB
16
                                        DONE
 17
                        FALSE
       1010
                67F8
                                movl
                                        #FF,R0
19
       1012
               3FF9
                                bra
                                        DONE
                        end MAIN
Successful completion of assembly - 2P
```

Expected Results: Actual Results: prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: End: PC: 1002 Clk: 4 Option: g Start: PC: 1002 PSW: 60E4 Brkpt: 0000 Clk: 4 1002: BN OFF: 0004 R0: 0000 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1008 When BN is encountered with a PSW Negative flag set, it should branch to the prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 TRUE label and set R0 to 0x00FF. End: PC: 1008 Clk: 6 It should not execute the BRA DONE Option: g Start: PC: 1008 PSW: 60E4 Brkpt: 0000 Clk: 6 End: PC: 1008 Clk: 8 instruction immediately after the BN, as the PC should have changed. Option: g Start: PC: 1008 PSW: 60E4 Brkpt: 0000 Clk: 8 1008: MOVL BYTE: FF DST: R0 R0: 00FF R1: 0000 0000 R3: 0000 R4 (BP): R5 (LR): 0000 (SP): 0000 (PC): 100A prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c:

- When BN is encountered with a PSW Negative flag cleared, it should not branch to the FALSE label and it should not set R0 to 0x0000.
- It should execute the BRA DONE instruction immediately after the BN, as the PC should not have changed.

```
orev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c:
End: PC: 100C Clk: 12
Start: PC: 100C PSW: 60E0 Brkpt: 0000 Clk: 12
100C: BN OFF: 0002
      00FF
R0:
R1:
      0000
      0000
R2:
      0000
R3:
R4 (BP):
R5 (LR):
R6 (SP):
R7 (PC):
prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0
End: PC: 100E Clk: 14
Option: g
Start: PC: 100E PSW: 60E0 Brkpt: 0000 Clk: 14
100E: BRA OFF: FFF6
R0:
      00FF
      0000
      0000
R3:
      0000
R4 (BP):
R5 (LR):
R6 (SP):
            0000
            0000
            0000
             1006
```

7. BGE

Purpose: Checks for successful implementation of BGE instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BGE when the PSW's Negative and oVerflow flags are set and cleared

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bge.txt
Time of assembly: Wed 31 Jul 2024 10:51:52
                                ВP
                                                 R4
 1
                                         eau
                                 LR
  2
                                         equ
                                                 R5
                                 SP
                                                 R6
 3
                                         eau
                                PC
                                                 R7
  4
                                         equ
                                         org #1000
 5
                        MAIN
  6
                4DB4
        1000
                                 setcc
                                         nv
        1002
                3402
                                         TRUE
  8
                                 bge
        1004
                3C00
                                         DONE
                                 bra
 10
                        DONE
 11
        1006
                3FFF
                                         DONE
                                 bra
                        TRUE
 12
        1008
                67F8
                                movl
                                         #FF,R0
 13
                                                          ; loop
        100A
                4DD0
 14
                                 clrcc
 15
        100C
                3401
                                         FALSE
                                 bge
        100E
                3FFB
                                         DONE
 16
                                 bra
 17
                        FALSE
        1010
                6000
                                 movl
                                         #00,R0
 18
 19
        1012
                3FF9
                                 bra
                                         DONE
 20
                        end MAIN
Successful completion of assembly - 2P
```

Expected Results:	Actual Results:
 When BGE is encountered with a PSW Negative flag set and oVerflow flag set, it should branch to the TRUE label and set R0 to 0x00FF. It should not execute the BRA DONE instruction immediately after the BGE, as the PC should have changed. 	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 End: PC: 100C Clk: 12 Option: g Start: PC: 100C PSW: 60E4 Brkpt: 0000 Clk: 12 100C: BGE
 When BGE is encountered with a PSW Negative flag set and oVerflow flag cleared, it should not branch to the FALSE label and it should not set R0 to 0x0000. It should execute the BRA DONE instruction immediately after the BGE, as the PC should not have changed. 	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 End: PC: 100C Clk: 12 Option: g Start: PC: 100C PSW: 60E4 Brkpt: 0000 Clk: 12 100C: BGE OFF: 0002 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R7 (PC): 100E prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 End: PC: 100E Clk: 14 Option: g Start: PC: 100E PSW: 60E4 Brkpt: 0000 Clk: 14 100E: BRA OFF: FFF6 R0: 00FF R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 R6 (SP): 0000 R7 (PC): 1006 PTev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0

8. BLT

Purpose: Checks for successful implementation of BLT instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BLT when the PSW's Negative flag and oVerflow flag are set and cleared.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: beqbz.txt
Time of assembly: Wed 31 Jul 2024 09:55:13
                                 BP
                                 LR
                                         equ
                                                 R5
  3
                                 SP
                                         equ
                                                 R6
  4
                                PC
                                         equ
                                                 R7
                                         org #1000
                        MAIN
  6
        1000
                4DA2
                                 setcc
                                         EQUAL
                2002
  8
        1002
                                beq
  9
        1004
                3C00
                                 bra
                                         DONE
                        DONE
 10
                3FFF
        1006
                                         DONE
 11
                                bra
                        EOUAL
 12
        1008
                67F8
                                         #FF,R0
 13
                                mov1
                                                         ; loop
 14
        100A
                4DC2
                                 clrcc
                                         UNEQUAL
 15
        100C
                2001
                                 beq
        100E
                3FFB
                                         DONE
 16
                                bra
 17
                        UNEQUAL
                67F8
 18
        1010
                                movl
                                         #FF,R0
 19
        1012
                3FF9
                                bra
                                        DONE
                        end MAIN
Successful completion of assembly - 2P
```

Expected Results: Actual Results: prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 End: PC: 1002 Clk: 4 Option: g Start: PC: 1002 PSW: 60E4 Brkpt: 0000 Clk: 4 1002: BLT OFF: 0004 R0: 0000 R1: 0000 R2: 0000 R3: 0000 R4 (BP): 0000 R5 (LR): 0000 When BLT is encountered with a PSW R7 (PC): Negative flag set and oVerflow flag 1008 prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 cleared, it should branch to the TRUE End: PC: 1008 Clk: 6 label and set R0 to 0x00FF. Option: g Start: PC: 1008 PSW: 60E4 Brkpt: 0000 Clk: 6 End: PC: 1008 Clk: 8 It should not execute the BRA DONE instruction immediately after the BLT, as Option: g Start: PC: 1008 PSW: 60E4 Brkpt: 0000 Clk: 8 1008: MOVL BYTE: FF DST: R0 the PC should have changed. 00FF 0000 R0: R1: R2: R3: 0000 0000 (BP): (LR): R6 (SP): R7 (PC): prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 1 z: 0 c: 0 End: PC: 100A Clk: 10

- When BLT is encountered with a PSW Negative flag set and oVerlow flag set, it should not branch to the FALSE label and it should not set R0 to 0x0000.
- It should execute the BRA DONE instruction immediately after the BGE, as the PC should not have changed.

```
prev: 3 flt: 0 curr: 7 v: 1 slp: 0 n: 1 z: 0 c: 0
End: PC: 100C Clk: 12
Option: g
Start: PC: 100C PSW: 60F4 Brkpt: 0000 Clk: 12
100C: BLT
     00FF
   (BP):
   (LR):
           0000
   (SP):
           0000
prev: 3 flt: 0 curr: 7 v: 1 slp: 0 n: 1 z: 0 c: 0
End: PC: 100E Clk: 14
Option: g
Start: PC: 100E PSW: 60F4 Brkpt: 0000 Clk: 14
100E: BRA OFF: FFF6
    00FF
R0:
R1:
     0000
R3:
   (LR):
   (SP): 0000
         1006
   (PC):
prev: 3 flt: 0 curr: 7 v: 1 slp: 0 n: 1 z: 0 c: 0
End: PC: 1006 Clk: 16
```

9. BRA always branches

Purpose: Checks for successful implementation of BRA instruction.

Configuration: The following .xme file is loaded into the emulator. It uses the BRA instruction to continuously branch to the label DONE, creating a loop.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: bl.txt
Time of assembly: Tue 30 Jul 2024 23:15:04
                                                 R4
                                BP
                                         eau
                                 LR
                                         equ
                                                 R5
                                 SP
                                                 R6
 3
                                         equ
                                 PC
  4
                                         equ
                                                 R7
                                         org #1000
  5
                        MAIN
  6
 7
        1000
                0001
                                bl
                                         LOOP
        1002
                                         DONE
 8
                3C02
                                 bra
                        LOOP
                                         #FF,R0
        1004
                67F8
 10
                                mov1
                                                         ; loop
 11
        1006
                4C2F
                                         LR,PC
                                 mov
                        DONE
 12
 13
        1008
                3FFF
                                         DONE
14
                        end MAIN
Successful completion of assembly - 2P
```

Expected Results:	Actual Results:
•	

```
Option: g
Start: PC: 1002 PSW: 60E0 Brkpt: 0000 Clk: 12
1002: BRA OFF: 0004
R0: 00FF
R1: 0000
R2: 0000
R3: 0000
R4 (BP): 0000
R7 (CP): 1008
prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0
End: PC: 1008 Clk: 14

Option: g
Start: PC: 1008 PSW: 60E0 Brkpt: 0000 Clk: 14
End: PC: 1008 Clk: 16

Option: g
Start: PC: 1008 PSW: 60E0 Brkpt: 0000 Clk: 14
End: PC: 1008 Clk: 16

Option: g
Start: PC: 1008 PSW: 60E0 Brkpt: 0000 Clk: 16
1008: BRA OFF: FFFE
R1: 0000
R2: 0000
R3: 0000
R4 (BP): 0000
R3: 0000
R4 (BP): 0000
R5 (LR): 1002
R6 (SP): 0000
R7 (CP): 1008
prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0
End: PC: 1008 Clk: 18
```