ECED3403 – Lab 4

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1. Testing

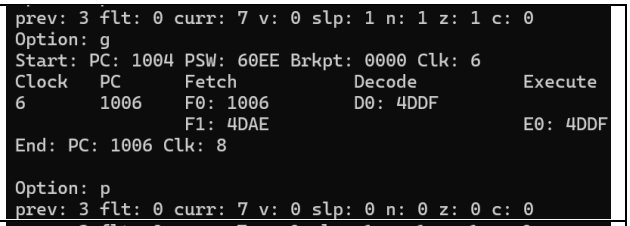
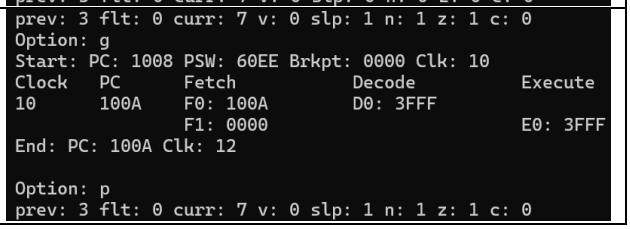
1. SETCC and CLRCC can successfully set or clear flags

Purpose: Checks for successful implementation of SETCC and CLRCC instructions.

Configuration: SETCC and CLRCC are used in an assembly code where each of them will set or clear all flags. They will also set or clear two flags at once to demonstrate that are not restricted to setting or clearing all flags at once.

```
X-Makina Assembler - Version XM-23P Single Pass+ Assembler - Release 24.04.17
Input file name: SETCCCLRCC.txt
Time of assembly: Wed 3 Jul 2024 15:35:36
  1                                   org #1000
  2                     MAIN
  3     1000    4DBF            setcc vsnzc
  4     1002    4DD1            clrcc vc
  5     1004    4DDF            clrcc vsnzc
  6     1006    4DAE            setcc snz
  7                     DONE
  8     1008    3FFF            bra     DONE            ; loop
  9                     end MAIN
Successful completion of assembly - 1P
```

Expected Results:	**Actual Results:**
At PC 1000, SETCC is used to set all flags. All flags should be set after the instruction.	prev: 3 flt: 0 curr: 7 v: 0 slp: 0 n: 0 z: 0 c: 0 Option: g Start: PC: 1000 PSW: 60E0 Brkpt: 0000 Clk: 2 Clock PC Fetch Decode Execute 2 1002 F0: 1002 D0: 4DBF F1: 4DD1 E0: 4DBF End: PC: 1002 Clk: 4 Option: p prev: 3 flt: 0 curr: 7 v: 1 slp: 1 n: 1 z: 1 c: 1
At PC 1002, CLRCC is used to clear the v and c flags. After the instruction, only slp, n, and z flags should be set.	prev: 3 flt: 0 curr: 7 v: 1 slp: 1 n: 1 z: 1 c: 1 Option: g Start: PC: 1002 PSW: 60FF Brkpt: 0000 Clk: 4 Clock PC Fetch Decode Execute 4 1004 F0: 1004 D0: 4DD1 F1: 4DDF E0: 4DD1 End: PC: 1004 Clk: 6 Option: p prev: 3 flt: 0 curr: 7 v: 0 slp: 1 n: 1 z: 1 c: 0

At PC 1002, CLRCC is used to clear all flags. After the instruction, all flags should be cleared.	
At PC 1002, SETCC is used to set the slp, n, and z flags. After the instruction, only slp, n, and z flags should be set.	

All flags are set and cleared as expected.

Pass/Fail: PASS

2. Stages are displayed as expected

Purpose: Checks for successful implementation of debugging print statements to verify stages occurring at each clock tick.

Configuration: Load any program and check for successful printing of pipeline stages.

Expected Results: The clock ticks and program counter for each two pipeline passes should be printed. The four stages should also be printed. For F0, instruction address should be printed. For F1, instruction bits should be printed. For D0, instruction to be decoded should be printed. For E0, instruction to be executed should be printed.

After discussion with Dr. Hughes, he permitted the third column (which stored instruction bits) to not be required as part of the display.

Actual results:

```
Start: PC: 0FFE PSW: 60EE Brkpt: 0000 Clk: 0
Clock   PC      Fetch           Decode          Execute
0       1000    F0: 1000        D0: 4C40
                F1: 4DBF                        E0: 4C40
2       1002    F0: 1002        D0: 4DBF
                F1: 4DD1                        E0: 4DBF
4       1004    F0: 1004        D0: 4DD1
                F1: 4DDF                        E0: 4DD1
6       1006    F0: 1006        D0: 4DDF
                F1: 4DAE                        E0: 4DDF
8       1008    F0: 1008        D0: 4DAE
                F1: 3FFF                        E0: 4DAE
10      100A    F0: 100A        D0: 3FFF
                F1: 0000                        E0: 3FFF
End: PC: 100A Clk: 12
```

The pipeline stages are displayed as expected.

Pass/Fail: PASS