ECED3403 – Assignment 2

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# Design

## Problem Introduction

This assignment aims to further develop the XM23p emulator that was begun in assignment 1. A three-stage pipeline and register operations will now be added. The three-stage pipeline has three stages, Fetch, Decode, and Execute. Using these stages, the pipeline can process and complete instructions every two clock cycles.

## Design Section

Pseudocode:

MAIN:

CALL initialize\_go

IF CLOCK value is even THEN

CALL F0

CALL D0

ELSE

CALL F1

CALL E0

END MAIN

FUNCTION initialize\_go

SET PC to S9 record value or 0

IMEM is initialized

SET CLOCK to 0

SET ICNTRL to 0

END initialize\_go

FUNCTION F0

SET IMAR to PC

INCREMENT PC by 2

END F0

FUNCTION F1

F

END F1

FUNCTION D0

D

END D0

FUNCTION E1

E

END E1

## Data Dictionary

CLOCK

PC

IMEM

ICNTRL

IMAR