ECED3403 – Assignment 3

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# Design

## Problem Introduction

This assignment aims to further develop the XM23p emulator. The goal of assignment 3 is to design features that allow the emulator to perform four data memory access instructions. These four instructions are LD, LDR, ST, and STR. Accessing data memory involves a fifth stage, E1 (Execute 1), which will occur on even clock ticks. E1 will either write to or read memory, depending on what instruction called it.

## Design Section

**PSEUDOCODE:**

mnemarray = [“BL” | “BEQBZ” | “BNEBZ” | … | “MOVH” | “LDR” | “STR”] \* array \*

reg\_const\_operands = sourceconstantcheck + wordbyte + sourceconstant + destination

sourceconstantcheck = unsigned int

wordbyte = unsigned int

sourceconstant = unsigned int

destination = unsigned int

unsigned int = [0-4294967295]

movx\_operands = bytevalue, destination

bytevalue = unsigned int

destination = unsigned int

instructionaddress = int \* address \*

programcounter = int \* address \*

ictrl = [READ | DONEREAD] \* ready for address save from buffer? \*

READ = 1

DONEREAD = 0

imbr = int \* instruction memory buffer \*

instructionmnem = 1[mnemarray]1

instructionbit = 16[bit]16

nota2 = [TRUE|FALSE]

TRUE = 1

FALSE = 0

arrayplace = int

int = 2147483647