ECED3403 – Lab 4

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# Testing

### SETCC and CLRCC can successfully set or clear flags

**Purpose:** Checks for successful implementation of SETCC and CLRCC instructions.

**Configuration:** SETCC and CLRCC are used in an assembly code where each of them will set or clear all flags. They will also set or clear two flags at once to demonstrate that are not restricted to setting or clearing all flags at once.

A screen shot of a computer

Description automatically generated

|  |  |
| --- | --- |
| **Expected Results:** | **Actual Results:** |
| At PC 1000, SETCC is used to set all flags. All flags should be set after the instruction. |  |
| At PC 1002, CLRCC is used to clear the v and c flags. After the instruction, only slp, n, and z flags should be set. |  |
| At PC 1002, CLRCC is used to clear all flags. After the instruction, all flags should be cleared. |  |
| At PC 1002, SETCC is used to set the slp, n, and z flags. After the instruction, only slp, n, and z flags should be set. |  |

All flags are set and cleared as expected.

**Pass/Fail:** PASS

### Stages are displayed as expected

**Purpose:** Checks for successful implementation of debugging print statements to verify stages occurring at each clock tick.

**Configuration:** Load any program and check for successful printing of pipeline stages.

**Expected Results:** The clock ticks and program counter for each two pipeline passes should be printed. The four stages should also be printed. For F0, instruction address should be printed. For F1, instruction bits should be printed. For D0, instruction to be decoded should be printed. For E0, instruction to be executed should be printed.

After discussion with Dr. Hughes, he permitted the third column (which stored instruction bits) to not be required as part of the display.

**Actual results:**

A screen shot of a computer

Description automatically generated

The pipeline stages are displayed as expected.

**Pass/Fail:** PASS