CT Unit 3: Logic Gates Project **Group:** **Name:**

Introduction

The purpose of the Logic Gates project is for students to become familiar with basic logic gates: symbols, Boolean function representations, and truth tables. In addition, students will learn to use logic simulation tool (*Logisim*) to capture the schematic diagram of logic circuits, run logic simulation of the circuits, and to derive the truth table and Boolean functions from logic circuits.

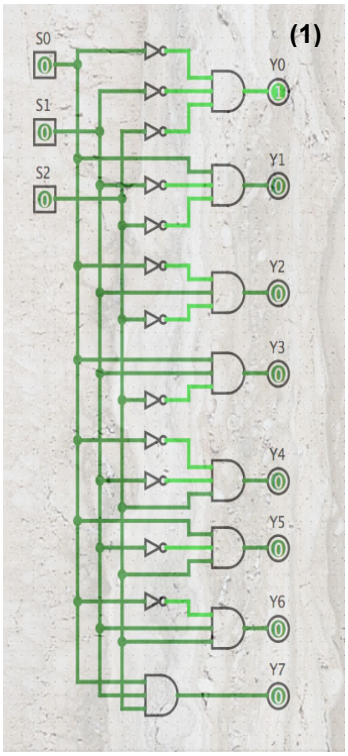
Tasks

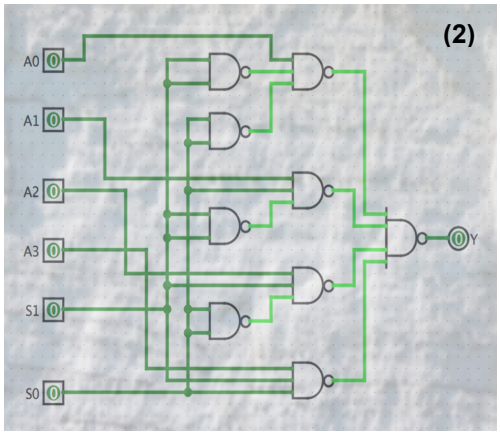
The *Son Doong Cave* in *Vietnam* is the biggest cave in the world. It's over 5.5 miles long, has a jungle and river, and could fit a 40-story skyscraper within its walls. British cavers were the first to explore it in 2009.

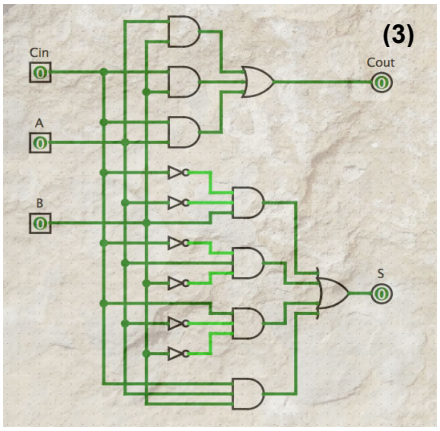
Recently, there is a major archaeological discovery in the cave. A series of geometric symbols organized in various shapes of networks have been discovered on various locations of the cave wall. Unidentified people have painted them in the Paleolithic age.

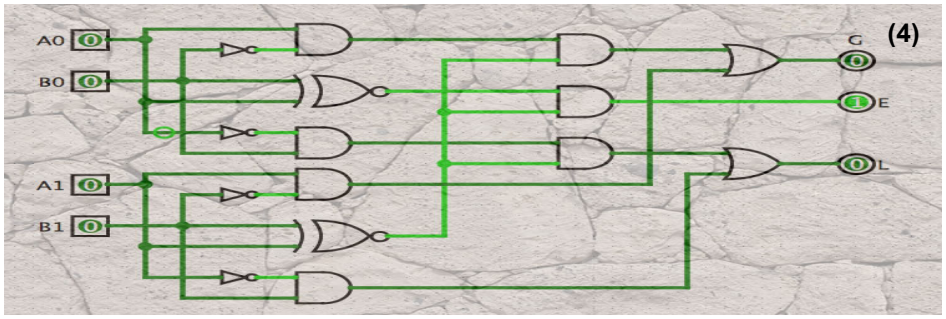
Through publishing the photos on the Internet, computer scientists and engineers around the world quickly recognized those symbols as logic gates, and those networks as logic circuits! How could people in Paleolithic age draw circuit diagrams matching the 21st century computer technology is an unexplained mystery! However, to determine the meanings of these logic circuits is the most pressing issue for today.

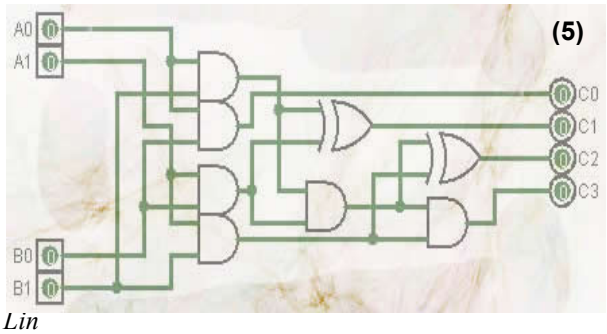
Diagrams

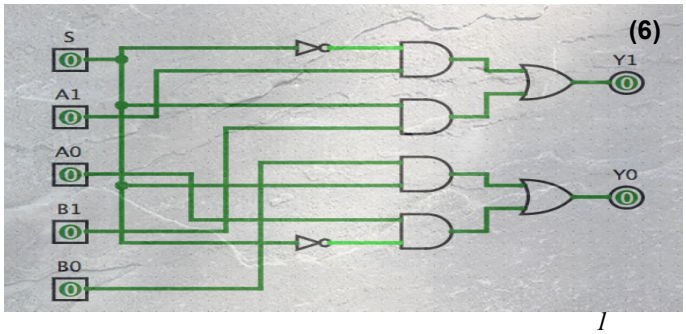










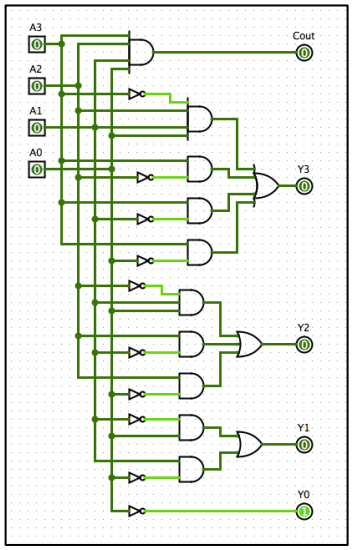


Deliverable

Each group will be assigned a specific diagram, and will have to finish a series of tasks and a word document including the following information:

1. drawing the logic circuit diagram using *Logisim*,
2. furnishing the truth table of the logic circuit,
3. writing the Boolean function of each output variable, and
4. explaining the possible usage of the logic circuits.

Example: Find the truth table, the Boolean functions, and the possible usage of the circuits in the following diagram.



There is an efficient ways to analyze your circuits, find the truth table and Boolean functions: using the logic simulator (*Logisim*). First, follow the following steps:

1) Perform the schematic entry (draw the circuit diagram using *Logisim*).
2) You can find the truth table and Boolean function of the logic circuit by selecting *Project > Analyze Circuit* and then click the *Table* and *Expression* tabs in the *Logicsim*.
3) You will see the Truth Table and Boolean Function as the following:

A3	A2	A1	A0	Cout	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1	0
0	0	1	0	0	0	0	1	1
0	0	1	1	0	0	1	0	0
0	1	0	0	0	0	1	0	1
0	1	0	1	0	0	1	1	0
0	1	1	0	0	0	1	1	1
0	1	1	1	0	1	0	0	0
1	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	1	0
1	0	1	0	0	1	0	1	1
1	0	1	1	0	1	1	0	0
1	1	0	0	0	1	1	0	1
1	1	0	1	0	1	1	1	0
1	1	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	0

Output: Cout — $A3\ A2\ A1\ A0$

Output: Y3 — $\overline{A3}\ A2\ A1\ A0 + A3\ \overline{A2} + A3\ \overline{A1} + A3\ \overline{A0}$

Output: Y2 — $\overline{A2}\ A1\ A0 + A2\ \overline{A1} + A2\ \overline{A0}$

Output: Y1 — $\overline{A1}\ A0 + A1\ \overline{A0}$

Output: Y0 — $\overline{A0}$

In order to identify the functions/usages of the logic circuits, analyze the inputs and outputs of the truth table:

A3	A2	A1	A0	A3-A0	Cout	Y3	Y2	Y1	Y0	Y3-Y0
0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	1	0	0	0	1	0	2
0	0	1	0	2	0	0	0	1	1	3
0	0	1	1	3	0	0	1	0	0	4
0	1	0	0	4	0	0	1	0	1	5
0	1	0	1	5	0	0	1	1	0	6
0	1	1	0	6	0	0	1	1	1	7
0	1	1	1	7	0	1	0	0	0	8
1	0	0	0	8	0	1	0	0	1	9
1	0	0	1	9	0	1	0	1	0	10
1	0	1	0	10	0	1	0	1	1	11
1	0	1	1	11	0	1	1	0	0	12
1	1	0	0	12	0	1	1	0	1	13
1	1	0	1	13	0	1	1	1	0	14
1	1	1	0	14	0	1	1	1	1	15
1	1	1	1	15	1	0	0	0	0	**0**

By reading the decimal values of ***input A3-A0*** and the decimal values of ***output Cout and Y3-Y0***, we notice that ***Y = A + 1***. So, the logic circuit is a **4-bit incrementing circuit**.