			constant_kk_o
			[7:0]
			constant_aaa_o
	instruction_i		[11:0]
	[17:0]		
			mux_i_o_select_o
	carry_i		
			slO_write_or_read_o
·	zero_i		
			slO_enable_o
			mux_register_select_o
			[1:0]
			sRegister_X_adresse_o
			[3:0]
			sRegister_Y_adresse_o
			[3:0]
			sRegister_write_enable_o
		Instruction	
		Instruction Decoder	mux_ALU_select_o
		Decodei	
			sALU_select_o
			[5:0]
			sALU_enable_o
			mux_stack_select_o
			sStack_write_or_read_o
			-Ct-sk smakle s
			sStack_enable_o
			DOlt
			mux_PC_select_o
	reset_i		sPC_enable_o
			or O_criable_o
	clk i		sRAM_write_or_read_o
	_clk_i		31 CAN WITTE OF TEAU O
			sRAM_enable_o
			STATINI_CHADIC_O
			l