PY32C642Data Sheet

32BitARM®Cortex®-M0+Microcontroller

Puya Semiconductor (Shanghai) Co., Ltd

PUYA

PY32C642series

32BitARM®Cortex®-M0+Microcontroller

Product Features

- Kernel
  - — 32BitARM®Cortex®- M0+
  - — Highest24 MHzOperating frequency
- Memory
  - — 24 Kbytes FlashMemory
  - — 3 Kbytes SRAM
- Clock system
  - — internal24 MHz RCOscillator (HSI)
  - — internal32.768 KHz RCOscillator (LSI)
  - — 32.768 KHzLow speed crystal oscillator (LSE
  - — External clock input
- Power Management and Reset
  - — Operating Voltage:1.7 V ~ 5.5 V
  - — Low Power Mode:Sleep/Stop
  - — Power-on/Power-off reset (POR/PDR)
  - — Brownout Detect Reset (BOR)
- General Purpose Input and Output (I/O)
  - — Up to18indivualI/O, both can be used as external interrupt
  - — Drive current8 mA
- 1 x 12BitADC
  - — Support most8External input channels,2Internal channels
  - — $V_{ADC-REF}$internal1.5 V,V_{CC}
- Timer
  - — 1indivual16bit Advanced Control Timer (TIM1)
  - — 1A universal16Bit Timer (TIM14)
  - — 1Low-power timer (LPTIM), support fromstopmold Wake-up
  - — 1Independent watchdog timer (IWDT)
  - — 1indivualSysTick timer
- hardwareCRC-32Modules
- 2Comparator
- onlyUID
- Serial Single Wire Debug (SWD
- Operating temperature: -40 ~ 85 °C
- EncapsulationQFN16,QFN20

Table of contents

1.Introduction

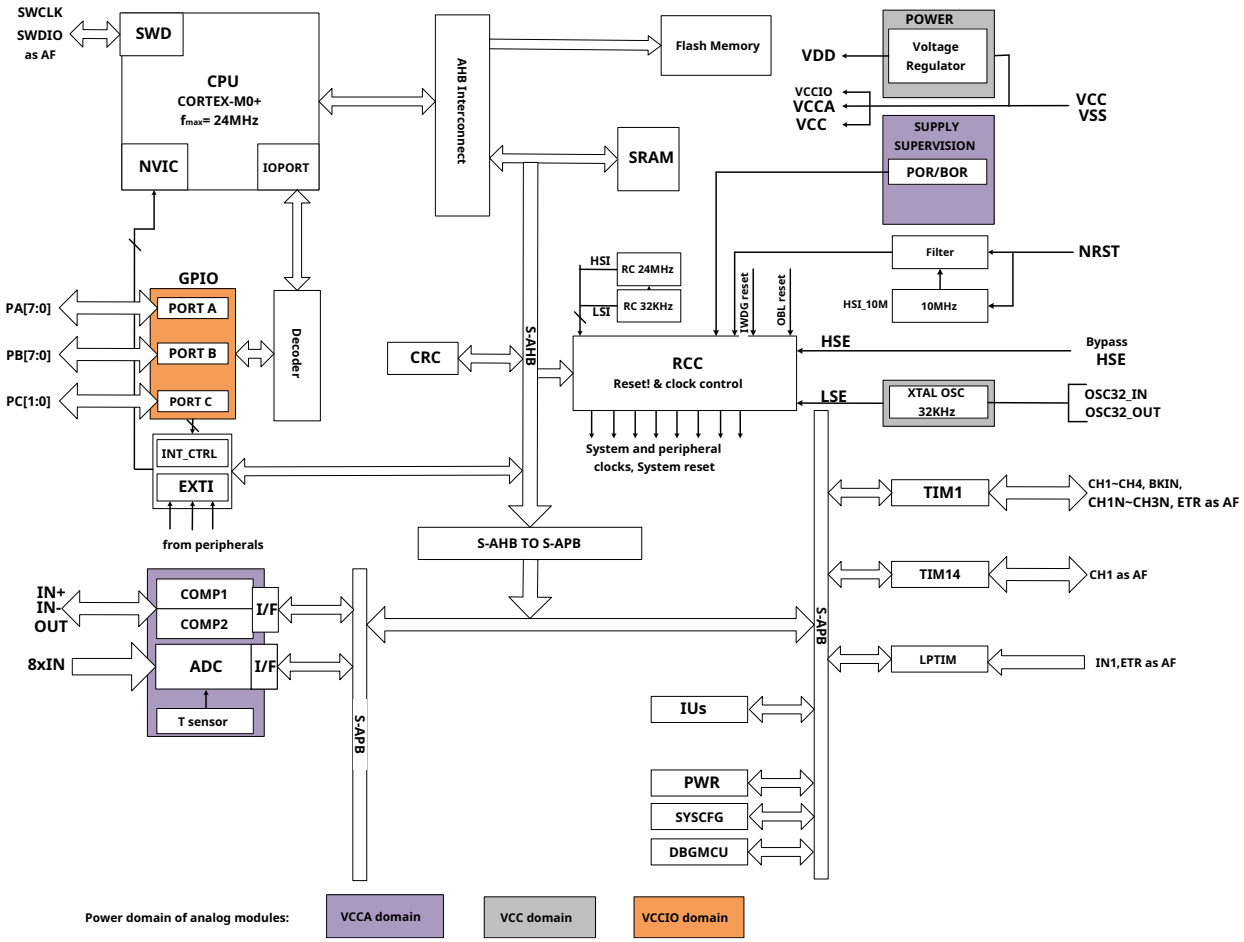
PY32C642Series of microcontrollers using high performance32BitARM®Cortex®-M0+Core, wide voltage operating rangeMCUEmbedtwenty four Kbytes Flashand3 Kbytes SRAMMemory, maximum operating frequency24 MHz. Contains a variety of different packaging types of products.1road12Bit ADC,2indivual16bit timer, and2Road comparator.

PY32C642The operating temperature range of the series microcontrollers is -40°C ~ 85°C, operating voltage range1.7 V ~ 5.5 V. Chip provides sleep/stopLow power working mode can meet different low power applications.

PY32C642The series of microcontrollers are suitable for a variety of application scenarios, such as controllers, handheld devices,PCPeripherals, Games andGPSPlatform, Work Industry applications, etc.

surface1-1 PY32C642Product Series Planning and Features

Peripherals		PY32C642W15U6	PY32C642F15U6
Flash memory (Kbytes)		twenty four	
SRAM (Kbytes)		3	
Timer	Advanced Timing Device	1 (16-bit)	
	General Timing Device	1 (16-bit)	
	Low power consumption Timer	1	
	SysTick	1	
	Watchdog	1	
Universal Port		14	18
ADCNumber of channels (External + Internal)		8+2	
Comparator		2	
Maximum frequency		24 MHz	
Operating voltage		1.7 V ~ 5.5 V	
Encapsulation		QFN16	QFN20



picture1-1Functional modules

2.Functional Overview

2.1. Arm®Cortex®-M0+Kernel

Arm®Cortex®- M0+It is an entry-level design for a wide range of embedded applications32BitArm Cortexprocessor. It provides developers

Membership offers significant benefits, including:

- Simple structure, easy to learn and program
- Ultra-low power consumption, energy-saving operation
- Reduced code density, etc.

Cortex-M0+The processor is32bit core, area and power optimized for high2The processor is streamlined

But the powerful instruction set and extensively optimized design provide high-end processing hardware, including single-cycle multipliers, providing32bit architecture computer

The expected superior performance, better than other8bit and16Bit microcontrollers have higher code density.

Cortex-M0+With a nested vectored interrupt controller (NVIC)Tight coupling.

2.2.Memory

On-chip integrationSRAM.passbyte (8Bit),half-word (16bit) orword (32bits) can be accessedSRAM.

On-chip integrationFlash,Include2It consists of different physical areas:

- Main FlashZone, which contains applications and user data
- Configurable sizeLoad FlashArea for storing customersISP/IAPBootloader
- Informationarea,768 bytes, which includes the following parts:
  - Option bytes
  - UID bytes
  - Factory Configuration bytes
  - USER OTP memory

rightFlash main memoryThe protection includes the following mechanisms:

- write protection (WRP)control to prevent unwanted write operations (due to the program memory pointerPCWrite protection

  The minimum protection unit is4 Kbytes.
- Option byteWrite protection, special unlocking design.

2.3. Bootmodel

Through the configuration bitnBOOT0/ nBOOT1(Stored inOption bytesThere are two different startup modes to choose from, as shown in the following table:

surface2-1 BootConfiguration

Boot mode configuration		Mode	
nBOOT1 bit	**nBOOT0 bit**	**Boot memory size == 0**	**Boot memory size != 0**
X	0	Main flashstart up	Main Flashstart up
0	1	SRAMstart up	SRAMstart up
1	1	N/A	Load Flashstart up

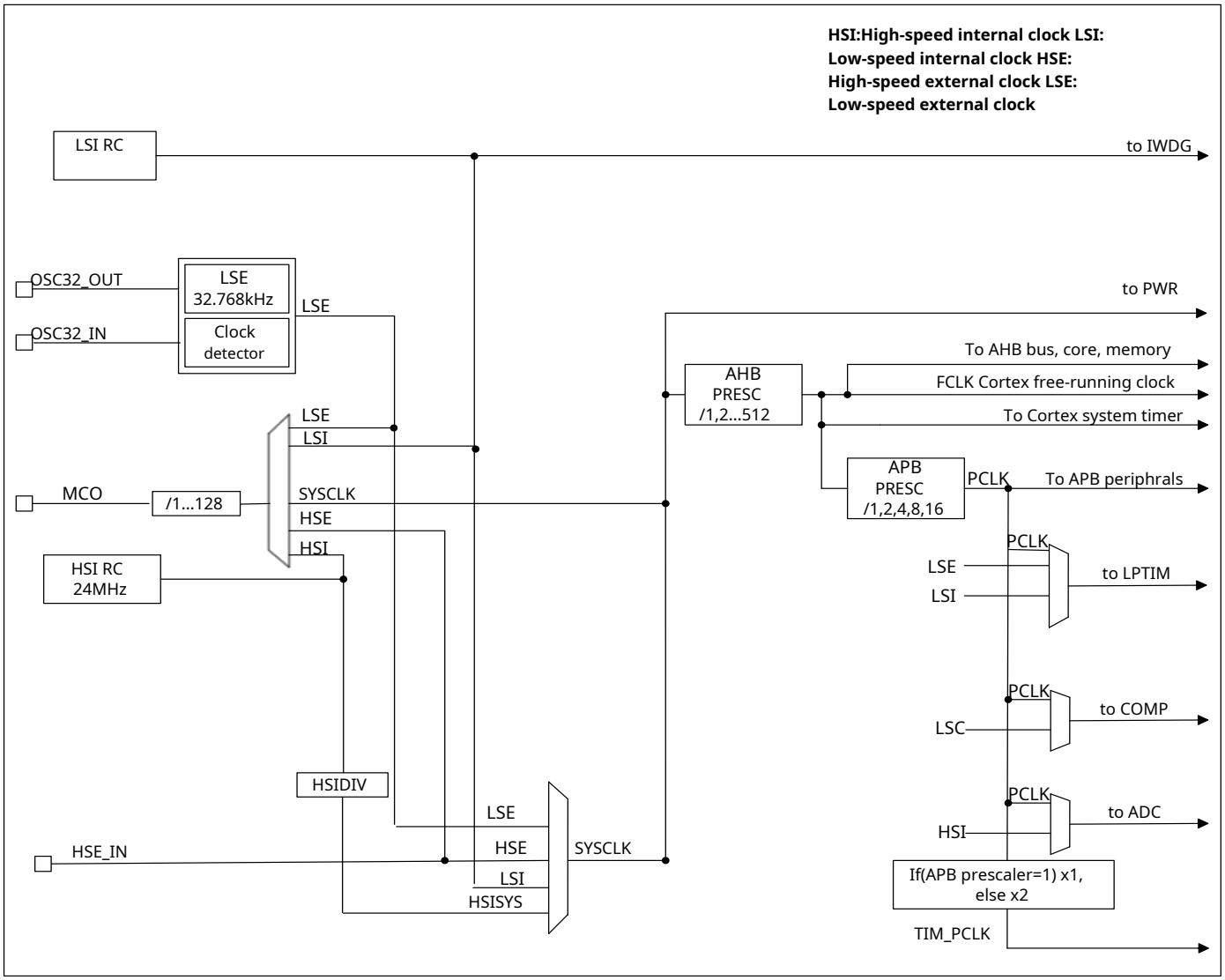
2.4.Clock system

CPUThe default system clock frequency after startup isHSI 24 MHz, you can reconfigure the system clock frequency and system clock after the program is running

The high frequency clocks that can be selected are:

- 24 MHzConfigurable internal high precisionHSIclock.
- one32.768 KHzConfigurable interiorLSIclock.
- 4 MHz ~ 32 MHzExternal input clock
- 32.768 KHz LSEclock.

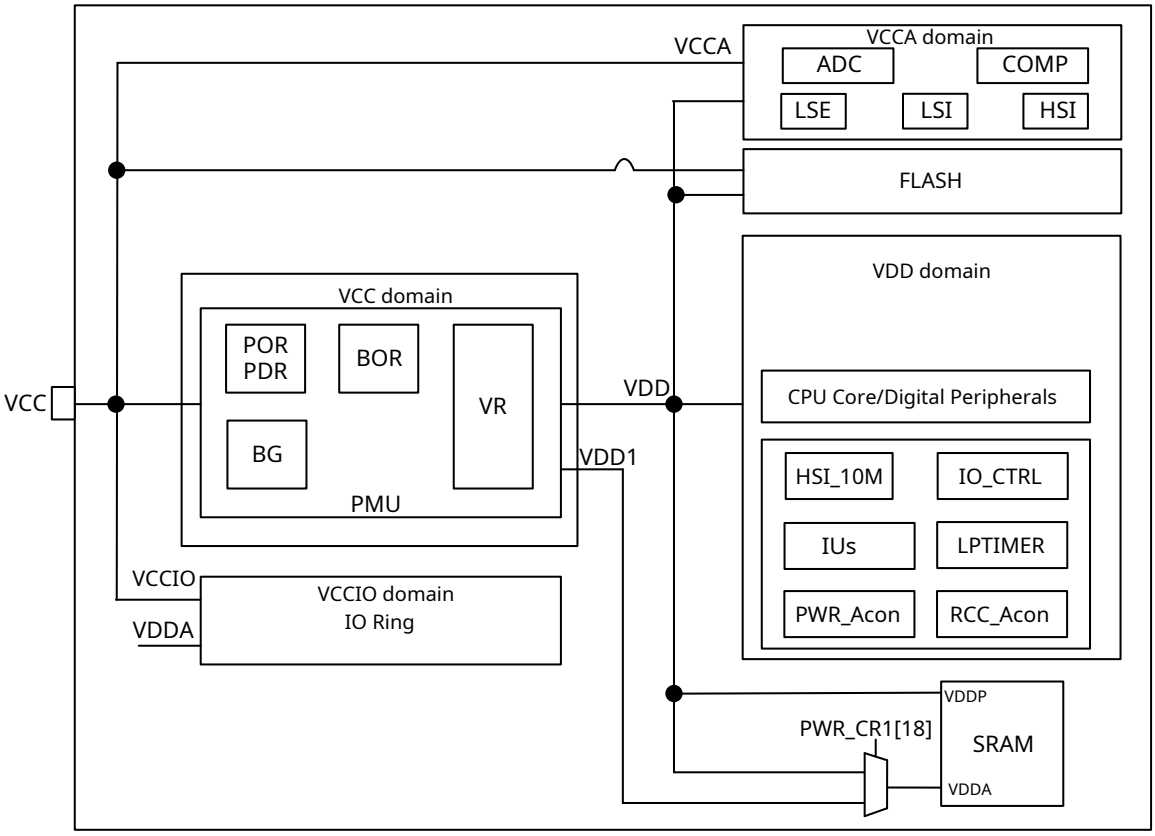
AHBThe clock can be divided based on the system clock.APBThe clock can be based onAHBClock division.AHBandAPBThe maximum clock frequency is 24 MHz.



picture2-1System clock structure diagram

2.5.Power Management

2.5.1.Power supply block diagram



picture2-2Power supply block diagram

surface2-2Power supply block diagram

serial number	power supply	Power Value	describe
1	V_{CC}	1.7 V ~ 5.5 V	The chip is powered by power pins, and its power supply module is: some analog circuits.
2	V_{CCA}	1.7 V ~ 5.5 V	Power for most analog modules comes fromV_{CC}PAD(Separate power supply can also be designed PAD.
3	V_{CCIO}	1.7 V ~ 5.5 V	GiveIOPower supply, fromV_{CC}PAD

2.5.2.Power Monitoring

2.5.2.1.Power-on/power-off reset (POR/PDR)

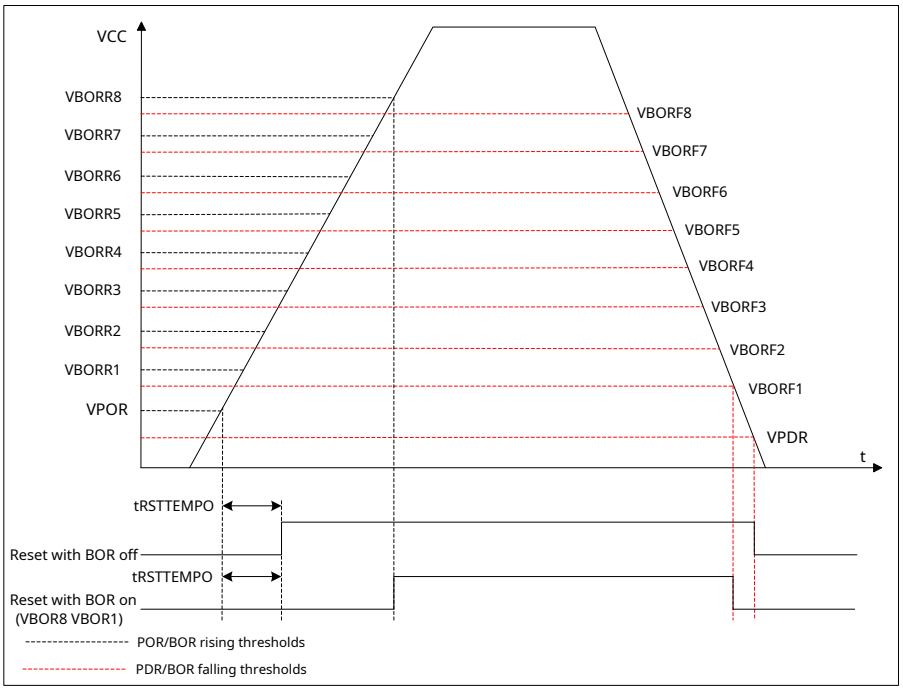
On-chip designPower on reset (POR)/Power down reset (PDR)Module, providing power-on and power-off reset for the chip. The block remains operational in all modes.

2.5.2.2.Brown-out reset (BOR)

Apart fromPOR/PDRIn addition, it also achievedBOR (brown out reset).BOROnly throughoption byteEnable and disable operate.

whenBORWhen opened,BORThe threshold value can beOption byteSelectable, rising and falling detection points can be configured independently

Set.



picture2-3 POR/PDR/BORThreshold

2.5.3.Voltage Regulator

The chip is designed with two voltage regulators:

- MR (Main regulator)Keep working while the chip is in normal operating state.
- LPR (low power regulator)existstopMode provides a lower power consumption option.

2.5.4.Low Power Mode

The chip is outside the normal operating mode.3Low power modes:

- **Sleep mode**:CPUClock Off (NVIC,SysTicketc.), the peripherals can be configured to keep working. (It is recommended to only enable A module that must work, close the module after the module work is completed)
- **Stop mode**: In this modeSRAMand register contents are retained, high-speed clockPLL,HSIandHSEclosure.GPIO, IUs,nRST,LPTIMCan wake upstopmodel.

2.6.Reset

There are two reset functions designed in the chip: power reset and system reset.

2.6.1.Power Reset

A power reset occurs in the following situations:

- Power-on/power-off reset (POR/PDR)
- Brown-out Reset (BOR)

2.6.2.System Reset

When the following events occur, a system reset occurs:

- NRST pinReset
- Independent watchdog reset (IWDG)
- SYSRESETREQSoftware reset
- option byte loadReset (OBL)
- Power Reset (POR/PDR,BOR)

2.7.General purpose input and outputGPIO

EachGPIOcan be configured by software as output (push-pulloropen drain, input (floating,pull-up/down,analog), peripheral multiplexing function, the locking mechanism will freezeI/OPort configuration function.

2.8.Interrupt

PY32C642passCortex-M0+The processor's embedded vectored interrupt controller (NVIC)and an extended interrupt/event controller (EXTI)To handle exceptions.

2.8.1.Interrupt ControllerNVIC

NVICyesCortex-M0+Tight coupling within the processorIP.NVICCan handle externalNMI (Non-maskable interrupts) and Maskable external interrupts, andCortex-M0+Internal exception.NVICProvides flexible priority management.

Processor core andNVICThe tight coupling greatly reduces the interrupt events and the corresponding interrupt service routines (ISR)Delay between starts.ISR The vectors are listed in a vector table, stored inNVICA base address for theISRThe vector address is composed of the vector table base address and Used as offsetISRComposed of serial numbers.

If a high-priority interrupt event occurs and a low-priority interrupt event is waiting for a response, the high-priority interrupt event that arrives later will be Events will be responded to first. Another optimization is called tail chaining (tail-chainingWhen a high priorityISRWhen returning, then start A pending low priorityISR, unnecessary processor context pushes and pops are skipped. This reduces latency and improves power consumption. Source efficiency.

NVICcharacteristic:

- Low latency interrupt processing
- 4Interrupt Priority Level
- support1indivualNMIInterrupt
- support18Maskable external interrupt
- support10indivualCortex-M0+abnormal
- High priority interrupts can interrupt low priority interrupt responses
- Support tail chaining (tail-chainingoptimization
- Hardware interrupt vector retrieval

2.8.2.Extended interruptEXTI

EXTIIncreased flexibility in handling physical line events and in the processor fromstopA wakeup event is generated when the mode is woken up.

EXTIThe controller has multiple channels, including up to18indivualGPIO,2indivualCOMPOutput, andLPTIMWake-up signal.

GPIO,COMPYou can configure the rising edge, falling edge, or both edges to trigger.GPIOThe signal is configured by selecting the signalEXTI0~7 aisle.

EachEXTI lineBoth can be masked independently via registers.

EXTIThe controller can capture pulses that are shorter than the internal clock period.

EXTIRegisters in the controller latch each event, even instopIn this mode, the processor can also recognize the wake-up after waking up from stop mode. The source of the wakeup, or identifying theGPIOand events.

2.9.Analog-to-digital converterADC

The chip has1indivual12PositionSARADCThis module has a total of up to10channels to be measured, including8External channels and2indivual Internal channel. The reference voltage can select the on-chip precise voltage1.5 VorV_{CC}power supply.

The conversion mode of each channel can be set to single, continuous, scan, or discontinuous mode. The conversion results are stored in left-aligned or right-aligned 16bit data register.

simulationwatchdogAllows the application to detect if the input voltage exceeds a user-defined high or low threshold.

ADCIt can run at low frequency and achieve very low power consumption.

At the end of sampling, conversion, and continuous conversion, analogwatchdogAn interrupt request is generated when the conversion voltage exceeds the threshold.

2.10.Comparator(COMP)

Integrated general purpose comparator (general purpose comparators) COMP, and can also be used withtimerUse together.

The comparator can be used as follows:

- Triggered by analog signal, wakes up from low power mode
- Analog Signal Conditioning
- When with fromtimerofPWMWhen output connection isCycle by cycleCurrent control loop

COMPKey Features

- Each comparator has configurable positive or negative input for flexible voltage selection
  - Multi-channelI/O pin
  - power supply$V_{CC}$and the voltage provided by the voltage divider15Score value (1/16,2/16 ... 15/16)
  - Internal reference voltage1.5 V, and the voltage provided by the voltage divider15Score value (1/16,2/16 ... 15/16)
- The output can be connected toI/OortimerThe input is used as a trigger
  - OCREF_CLRevent (cycle by cycleCurrent control)
  - For fastPWM shutdownBrakes

EachCOMPWith interrupt generation capability, used to switch the chip out of low power mode (sleepmode) (viaEXTI)

2.11.Timer

PY32C642The characteristics of different timers are shown in the following table:

surface2-3Timer Characteristics

type	Timer	Bit width	Counting direction	Prescaler	DMA	Capture/Compare Channel	Complementary output
Advanced Timer	TIM1	16Bit	up and down, Center Alignment	1 ~ 65536	support	4	3
General purpose timer	TIM14	16-Bit	superior	1 ~ 65536	-	1	-

2.11.1.Advanced Timer

Advanced Timer(TIM1)Depend on16The 12-bit auto-load counter is driven by a programmable divider. It can be used in various scenarios, including The following are examples: Pulse length measurement of input signals (input capture), or generation of output waveforms (output compare, outputPWM, with dead zone insertion ComplementarityPWM).

TIM1include4Independent channels for:

- Input Capture
- Output Compare
- PWMGenerate (edge or center alignment mode)
- Single pulse mode output

ifTIM1Configured as standard16bit timer, it hasTIMxSame characteristics as the timer. If configured as16BitPWM Generator, it has full modulation capability (0 - 100%).

existMCU debugmodel,TIM1The count can be frozen.

With the same architecturetimerFeatures are shared, soTIM1Can work with other timers via the timer link function to achieve Synchronization or event linking.

2.11.2.General purpose timer

- General purpose timerTIM14Driven by a programmable prescaler16bit auto-load counter.
- TIM14have1Independent channels for input capture/output comparison,PWMOr single pulse mode output.
- existMCU debugmodel,TIM14The count can be frozen.

2.11.3.Low Power Timer

- LPTIMfor16Bit up counter, including31-bit prescaler. Only supports single count.
- LPTIMCan be configured asstopMode wakeup source.
- existMCU debugmodel,LPTIMThe count value can be frozen.

2.11.4. IWDG

The chip integrates aIndependent watchdogAbbreviationIWDG)The module has high security level, precise timing and flexible use Features of use.IUsFind and resolve functional confusion caused by software failures andtimeoutTrigger when value System reset.

- IUsDepend onLSIProvides a clock so that even if the master clockFail, and can also keep working.
- IUsBest suited for needswatchdogAs an independent process outside the main application, and without high timing accuracy constraints use.

- passoption byteThe control can enableIUsHardware mode.
- IUsyesstopThe wake-up source of the mode is to wake up by resetstopmodel.
- existMCU debugmodel,IUsThe count value can be frozen.

2.11.5. SysTick timer

SysTickCounters are specifically designed for real-time operating systems (RTOS), but can also be used as a standard down counter.

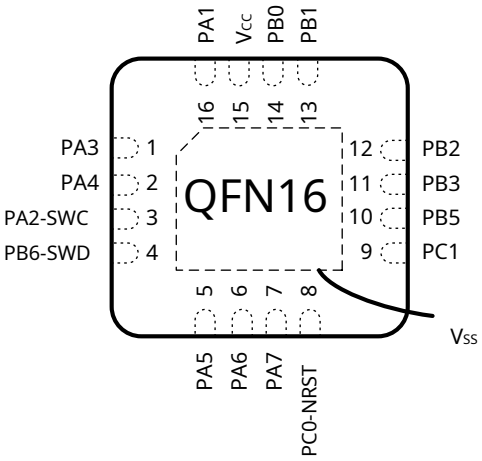
SysTickcharacteristic:

- twenty fourBit count down
- Self-loading capability
- Counter to0An interrupt can be generated when (maskable)

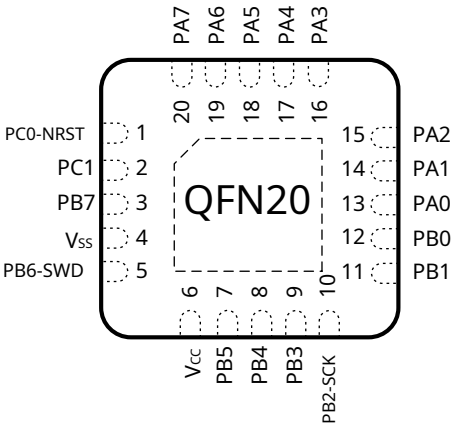
2.12. SWD

ARM SWDThe interface allows serial debugging tools to connect toPY32C642.

3.Pin Configuration



picture3-1 QFN16 Pinout1 PY32C642W15U



picture3-2 QFN20 Pinout1 PY32C642F15U

surface3-1Pin Definition Terms and Symbols

type		symbol	definition
Port Type		S	Supply pin
		G	Ground pin
		I/O	Input/output pin
		NC	No definition
Port Structure		COM	normal5 VPort, supports analog input and output functions
		RST	-
Notes			Unless otherwise stated, all ports are used as analog inputs before and after reset.
Port Function	Multiplexing function		passGPIOx_AFRRegister Select Function
	Additional Features		Functions directly selected or enabled via peripheral registers

surface3-2 QFN16/QFN20Pin Definition

Package Type		Reset	Port Type	Port Structure	Notes	Port Function	
QFN16 W1	QFN20 F1					Multiplexing function	Additional Features
5	18	PA5	I/O	COM		TIM1_CH1 TIM14_CH1	
6	19	PA6	I/O	COM		EVENTOUT	ADC_IN3 External_clock_in
7	20	PA7	I/O	COM		TIM1_CH4 MCO	ADC_IN4
8	1	PC0-NRST	I/O	RST	(1)	SWDIO TIM1_CH1N EVENTOUT	NRST ADC_IN5
9	2	PC1-OSCIN	I/O	COM		-	OSCIN
-	3	PB7-OSCOUT	I/O	COM		TIM14_CH1	OSCOUT
-	4	V_{SS}	S			Ground	
4	5	PB6(SWDIO)	I/O	COM		SWDIO	ADC_IN6
15	6	V_{CC}	S			Digital power supply	
10	7	PB5	I/O	COM		TIM1_CH3 TIM14_CH1	
-	8	PB4	I/O	COM		TIM1_BKIN	
11	9	PB3	I/O	COM		TIM1_ETR CMP1_OUT	
12	10	PB2	I/O	COM		TIM1_CH1N TIM1_CH3	
13	11	PB1	I/O	COM		TIM1_CH2N TIM1_CH4 MCO	ADC_IN0 CMP1_INP CMP1_INM
14	12	PB0	I/O	COM		TIM1_CH2 TIM1_CH3N	ADC_IN7 CMP1_INM
-	13	PA0	I/O	COM		TIM1_CH1	
16	14	PA1	I/O	COM		TIM1_CH2	
3	15	PA2(SWCLK)	I/O	COM		SWCLK TIM1_CH4 CMP2_OUT	
1	16	PA3	I/O	COM		TIM1_CH2	ADC_IN1 CMP2_INP CMP2_INM
2	17	PA4	I/O	COM		TIM1_CH3 TIM14_CH1	ADC_IN2 CMP2_INM

1.choosePC0orNRST/SWDIOis throughoption bytesto configure.

2.After reset (option byteConfiguration0/0,0/1,1/0hour),PB6andPA2twopinConfigured asSWDIOandSWCLK AFFunction, the former

The internal pull-up resistor or the internal pull-down resistor is activated.

3.After reset (option byteConfigured as1/1hour),PC0andPA2twopinConfigured asSWDIOandSWCLK AFfunction, the former internal

pull-up resistor, or the internal pull-down resistor is activated

3.1.portAMultiplexing function mapping

surface3-3portAMultiplexing function mapping

port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	-	TIM1_CH1	-	-	-	-	-
PA1	-	-	TIM1_CH2	-	-	-	-	-
PA2	SWC	-	TIM1_CH4	-	CMP2_OUT	-	-	-
PA3	-	-	TIM1_CH2	-	-	-	-	-
PA4	-	-	TIM1_CH3	-	-	TIM14_CH1	-	-
PA5	-	-	TIM1_CH1	-	-	TIM14_CH1	-	-
PA6	-	-	-	-	-	-	-	EVENTOUT
PA7	-	-	TIM1_CH4	-	MCO	-	-	

3.2.portBMultiplexing function mapping

surface3-4portBMultiplexing function mapping

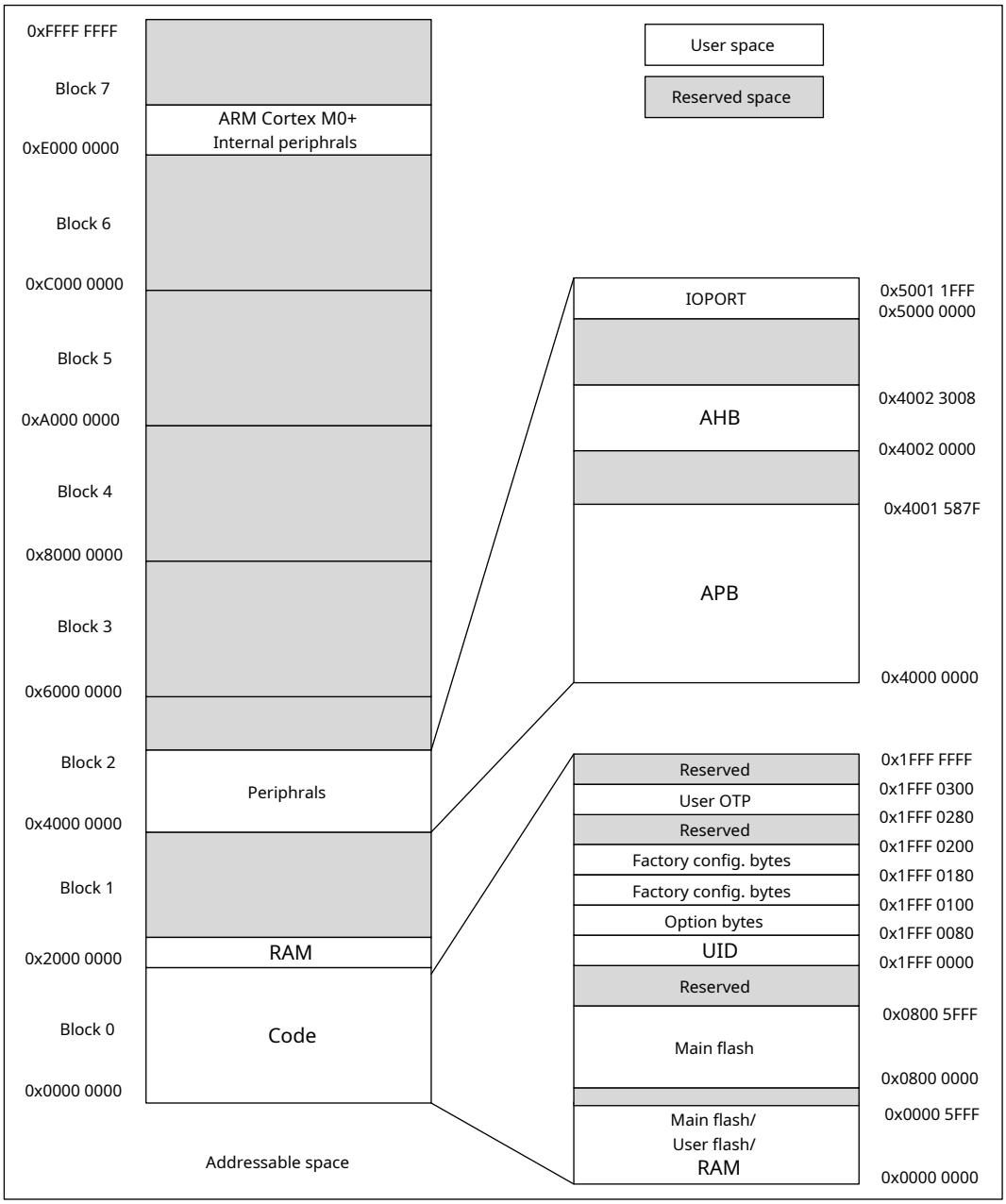
port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	-	TIM1_CH2	TIM1_CH3N	-	-	-	-
PB1	-	-	TIM1_CH2N	TIM1_CH4	MCO	-	-	-
PB2	-	-	TIM1_CH1N	TIM1_CH3	-	-	-	-
PB3	-	-	TIM1_ETR	-	CMP1_OUT	-	-	-
PB4	-	-	TIM1_BKIN	-	-	-	-	-
PB5	-	-	TIM1_CH3	-	-	TIM14_CH1	-	-
PB6	SWD	-	-	-	-	-	-	-
PB7	-	-	-	-	-	TIM14_CH1	-	-

3.3.portCMultiplexing function mapping

surface3-5portCMultiplexing function mapping

port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0-NRST	SWD	-	TIM1_CH1N	-	-	-	-	EVENTOUT
PC1-OSCIN	-	-	-	-	-	-	-	-

4.Memory Map



picture4-1Memory Map

surface4-1Memory address

Type	Boundary Address	Size	Memory Area	Description
SRAM	0x2000 C000-0x3FFF FFFF	-	Reserved	-
	0x2000 0000-0x2000 0BFF	3 KBytes	SRAM	-
Code	0x1FFF 0300-0x1FFF FFFF	-	Reserved	-
	0x1FFF 0280-0x1FFF 02FF	128 Bytes	USER OTP memory	Storing user data
	0x1FFF 0180-0x1FFF 01FF	128 Bytes	Factory Configuration bytes	StorageTrimmingData (including HSI trimmingData), power on and read the check code
	0x1FFF 0100-0x1FFF 017F	128 Bytes	Factory Configuration bytes	Store user usedHSI Trimmingdata,flashErase and write time configuration parameters
	0x1FFF 0080-0x1FFF 00FF	128 Bytes	Option bytes	Chip hardware and softwareoption bytes information
	0x1FFF 0000-0x1FFF 007F	128 Bytes	UID	Unique ID
	0x0800 6000-0x1FFE FFFF	-	Reserved	-
	0x0800 0000-0x0800 5FFF	24 KBytes	Main flash memory	-
	0x0000 6000-0x07FF FFFF	-	Reserved	-
	0x0000 0000-0x0000 5FFF	24 Kbytes	according toBootConfiguration options: 1) Main flash memory 2) Load flash 3) SRAM	-

1.The above space0x1FFF 0E00-0x1FFF 0E7FThe rest are marked asreservedThe space cannot be written and read as0, and produce bornresponse error.

surface4-2Peripheral register addresses

Bus	Boundary Address	Size	Peripheral
	0xE000 0000-0xE00F FFFF	1 Mbytes	M0+
IOPORT	0x5000 1800-0x5FFF FFFF	-	Reserved(1)
	0x5000 1400-0x5000 17FF	-	Reserved(1)
	0x5000 1000-0x5000 13FF	-	Reserved(1)
	0x5000 0C00-0x5000 0FFF	-	Reserved(1)
	0x5000 0800-0x5000 0BFF	1 Kbytes	GPIOC
	0x5000 0400-0x5000 07FF	1 Kbytes	GPIOB
	0x5000 0000-0x5000 03FF	1 Kbytes	GPIOA
AHB	0x4002 3400-0x4FFF FFFF	-	Reserved
	0x4002 300C-0x4002 33FF	1 Kbytes	Reserved
	0x4002 3000-0x4002 3008		CRC
	0x4002 2400-0x4002 2FFF	-	Reserved

Bus	Boundary Address	Size	Peripheral
	0x4002 2000-0x4002 23FF		Flash
	0x4002 1C00-0x4002 1FFF	-	Reserved
	0x4002 1900-0x4002 1BFF	1 Kbytes	Reserved
	0x4002 1800-0x4002 18FF		EXTI(2)
	0x4002 1400-0x4002 17FF	-	Reserved
	0x4002 1080-0x4002 13FF	1 KBytes	Reserved
	0x4002 1000-0x4002 107F		RCC(2)
	0x4002 0C00-0x4002 0FFF	1 KBytes	Reserved
	0x4002 0040-0x4002 03FF	-	Reserved
	0x4002 0000-0x4002 003C		Reserved
APB	0x4001 5C00-0x4001 FFFF	-	Reserved
	0x4001 5880-0x4001 5BFF	1 Kbytes	Reserved
	0x4001 5800-0x4001 587F		DBG
	0x4001 4C00-0x4001 57FF	-	Reserved
	0x4001 4850-0x4001 4BFF	-	Reserved
	0x4001 4800-0x4001 484C		Reserved
	0x4001 4450-0x4001 47FF	-	Reserved
	0x4001 4400-0x4001 404C		Reserved
	0x4001 3C00-0x4001 43FF	-	Reserved
	0x4001 381C-0x4001 3BFF	-	Reserved
	0x4001 3800 - 0x4001 3018		
	0x4001 3400-0x4001 37FF	-	Reserved
	0x4001 3010-0x4001 33FF	-	Reserved
	0x4001 3000-0x4001 300C		
	0x4001 2C50-0x4001 2FFF	1 Kbytes	Reserved
	0x4001 2C00-0x4001 2C4C		TIM1
	0x4001 2800-0x4001 2BFF	-	Reserved
	0x4001 270C-0x4001 27FF	1 Kbytes	Reserved
	0x4001 2400-0x4001 2708		ADC
	0x4001 0400-0x4001 23FF	-	Reserved
	0x4001 0220-0x4001 03FF	1 KBytes	Reserved
	0x4001 0200-0x4001 021F		COMP1/2
	0x4001 0000-0x4001 01FF		SYSCFG

Bus	Boundary Address	Size	Peripheral
	0x4000 B400-0x4000 FFFF	-	Reserved
	0x4000 B000-0x4000 B3FF	-	Reserved
	0x4000 8400-0x4000 AFFF	-	Reserved
	0x4000 7C28-0x4000 7FFF	1 KBytes	Reserved
	0x4000 7C00-0x4000 7C24		LPTIM
	0x4000 7400 - 0x4000 7BFF	-	Reserved
	0x4000 7018 - 0x4000 73FF	1 KBytes	Reserved
	0x4000 7000 - 0x4000 7014		PWR(3)
	0x4000 5800-0x4000 6FFF	-	Reserved
	0x4000 5434 - 0x4000 57FF	-	Reserved
	0x4000 5400 - 0x4000 5430		
	0x4000 4800-0x4000 53FF	-	Reserved
	0x4000 441C-0x4000 47FF	-	Reserved
	0x4000 4400 - 0x4000 4418		Reserved
	0x4000 3C00-0x4000 43FF	-	Reserved
	0x4000 3810-0x4000 3BFF	-	Reserved
	0x4000 3800-0x4000 380C		Reserved
	0x4000 3400-0x4000 37FF	-	Reserved
	0x4000 3014-0x4000 33FF	1 Kbytes	Reserved
	0x4000 3000-0x4000 0010		IUs
	0x4000 2C0C-0x4000 2FFF	-	Reserved
	0x4000 2C00-0x4000 2C08		Reserved
	0x4000 2830-0x4000 2BFF	-	Reserved
	0x4000 2800-0x4000 282C		Reserved
	0x4000 2420-0x4000 27FF	-	Reserved
	0x4000 2400-0x4000 241C		Reserved
	0x4000 2054-0x4000 23FF	1 Kbytes	Reserved
	0x4000 2000-0x4000 0050		TIM14
	0x4000 1800-0x4000 1FFF	-	Reserved
	0x4000 1400-0x4000 17FF	-	Reserved
	0x4000 1030-0x4000 13FF	-	Reserved
	0x4000 1000-0x4000 102C		Reserved
	0x4000 0800-0x4000 0FFF	-	Reserved

Bus	Boundary Address	Size	Peripheral
	0x4000 0450-0x4000 07FF	-	Reserved
	0x4000 0400-0x4000 044C		Reserved
	0x4000 0000-0x4000 03FF	-	Reserved

1.Table aboveAHBMarked asReservedThe address space cannot be written, and the read back is0, and produceshardfault;APBMarked asReserved

The address space cannot be written, and the read back is0, will not producehardfault.

2.Not only support32It supports word access, half-word access, and byte access.

3.Not only support32Bit word access and half-word access are also supported.

5.Electrical Characteristics

5.1.Test conditions

Unless otherwise specified, all voltages are inV_{SS}As a benchmark.

5.1.1.Minimum and Maximum Values

Unless otherwise specified, the ambient temperatureT_A= 25°C andT_A= $T_{A(max)}$Chip mass production test screening under the worst

Minimum and maximum values are specified over ambient temperature, supply voltage, and clock frequency.

Data based on electrical characteristic results, design simulations, and/or process parameters noted below the table; not tested in production. Minimum and Maximum Values refer to sample tests and are averaged plus or minus three times the standard deviation.

5.1.2.Typical Value

Unless otherwise stated, typical data are based onT_A= 25°C andV_{CC}= 3.3 VThese data are for design guidance only and have not been tested.

TypicalADCThe precision value is obtained by sampling a standard batch and testing it at all temperature ranges.95%Small chip error is equal to the given value.

5.2.Absolute Maximum Ratings

If the voltage applied to the chip exceeds the absolute maximum value given in the following table, it may cause permanent damage to the chip.

The withstand strength rating does not mean that the device will function properly under this condition. Working at the maximum value for a long time may affect Affects the reliability of the chip.

surface5-1Voltage characteristics(1)

symbol	describe	Minimum	Maximum	unit
V_{CC}	External main power supply	- 0.3	6.25	V
V_{IN}	otherPinInput voltage	- 0.3	V_{CC}+0.3	V

1.power supplyV_{CC}HediV_{SS}The pin must always be connected to an external power supply system within the allowed range.

surface5-2Current characteristics

symbol	describe	Maximum	unit
I_{VCC}	Flow InV_{CC}pinTotal current (supply current)(1)	80	mA
I_{VSS}	OutflowV_{SS}pinTotal current (outflow current)(1)	80	mA
$I_{IO(PIN)}$	allIOOutput Sink Current	20	mA
	allIOThe source current	- 20	

1.power supplyV_{CC}HediV_{SS}The pin must always be connected to an external power supply system within the allowed range.

surface5-3Temperature characteristics

symbol	describe	Numeric	unit
T_{STG}	Storage temperature range	-65 ~ +150	°C
T_O	Operating temperature range	-40 ~ +85	°C

5.3.Working conditions

5.3.1.General working conditions

surface5-4General working conditions

symbol	parameter	condition	Minimum	Maximum	unit
f_{HCLK}	internalAHBClock frequency	-	0	twenty four	MHz
f_{PCLK}	internalAPBClock frequency	-	0	twenty four	MHz
V_{CC}	Standard operating voltage	-	1.7	5.5	V
V_{IN}	IOInput voltage	-	- 0.3	V_{CC}+0.3	V
T_A	Ambient temperature	-	- 40	85	°C
T_J	Junction temperature	-	- 40	90	°C

5.3.2.Power on and off working conditions

surface5-5Power-on and power-off operating conditions

symbol	parameter	condition	Minimum	Maximum	unit
t_{VCC}	V_{CC}Ascent rate	-	0	∞	μs/V
	V_{CC}Descent rate	-	20	∞	

5.3.3.Embedded reset module features

surface5-6Embedded reset module features

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
$V_{POR/PDR}$	Power-on/power-off reset threshold	Rising edge	1.5	1.6	1.7	V
		Falling edge	1.45	1.55	1.65	V
$V_{PDRhyst}$ (1)	PDRHysteresis	-	-	50	-	mV
V_{BOR}	BORThreshold voltage	BOR_LEV[2:0]=000 (Rising edge)	1.7	1.8	1.9	V
		BOR_LEV[2:0]=000 (Falling edge)	1.6	1.7	1.8	V
		BOR_LEV[2:0]=001 (Rising edge)	1.9	2	2.1	V
		BOR_LEV[2:0]=001 (Falling edge)	1.8	1.9	2	V
		BOR_LEV[2:0]=010 (Rising edge)	2.1	2.2	2.3	V
		BOR_LEV[2:0]=010 (Falling edge)	2	2.1	2.2	V

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
		BOR_LEV[2:0]=011 (Rising edge)	2.3	2.4	2.5	V
		BOR_LEV[2:0]=011 (Falling edge)	2.2	2.3	2.4	V
		BOR_LEV[2:0]=100 (Rising edge)	2.5	2.6	2.7	V
		BOR_LEV[2:0]=100 (Falling edge)	2.4	2.5	2.6	V
		BOR_LEV[2:0]=101 (Rising edge)	2.7	2.8	2.9	V
		BOR_LEV[2:0]=101 (Falling edge)	2.6	2.7	2.8	V
		BOR_LEV[2:0]=110 (Rising edge)	2.9	3	3.1	V
		BOR_LEV[2:0]=110 (Falling edge)	2.8	2.9	3	V
		BOR_LEV[2:0]=111 (Rising edge)	3.1	3.2	3.3	V
		BOR_LEV[2:0]=111 (Falling edge)	3	3.1	3.2	V
V_{BOR_hyst}	BORHysteresis	-	-	100	-	mV

1.Guaranteed by design, not tested in production.

2.The data is based on assessment results and is not tested in production.

5.3.4.Working current characteristics

surface5-7Run mode current

symbol	condition						Typical Value(1)	Maximum	unit
	System clock	frequency	Code	run	Peripheral clock	FLASH sleep			
I_{DD}(run)	HSI	24 MHz	While(1)	Flash	ON	DISABLE	1.1	-	mA
					OFF	DISABLE	0.9	-	
	LSI	32.768 KHz			ON	DISABLE	160.4	-	μA
					OFF	DISABLE	159.6	-	
	LSI	32.768 KHz			ON	ENABLE	108.3	-	μA
					OFF	ENABLE	107.7	-	

1.The data is based on assessment results and is not tested in production.

surface5-8 sleepMode Current

symbol	condition				Typical Value(1)	Maximum	unit
	System clock	frequency	Peripheral clock	FLASH sleep			
I_{DD}(sleep)	HSI	24 MHz	ON	DISABLE	0.8	-	mA
			OFF	DISABLE	0.5	-	
	LSI	32.768 KHz	ON	DISABLE	159.3	-	μA
			OFF	DISABLE	158.9	-	
	LSI	32.768 KHz	ON	ENABLE	85.3	-	μA
			OFF	ENABLE	84.8	-	

1.The data is based on assessment results and is not tested in production.

surface5-9 stopMode Current

symbol	condition				Typical Value(1)	Maximum	unit
	Vcc	MR/LPR	LSI	Peripheral clock			
IDD(stop)	1.7~5.5 V	MR	-	-	75.3	-	μA
		LPR	ON	IWDG+LPTIM	1.7	-	
				IUs	1.7	-	
				LPTIM	1.7	-	
			OFF	No	1.5	-	

1.The data is based on assessment results and is not tested in production.

5.3.5.Low power mode wake-up time

surface5-10Low power mode wake-up time

symbol	parameter(1)		condition	Typical Value(2)	Maximum	one Bit
TWUSLEEP	SleepWake-up time		-	0.6	-	μs
TWUSTOP	StopCall Wake up time	MRpowered by	FlashIn the execution program,HSI(24 MHz)As a system clock	6.4	-	
		LPRpowered by	FlashIn the execution program,HSIAs the system clock (24 M)	10.6	-	

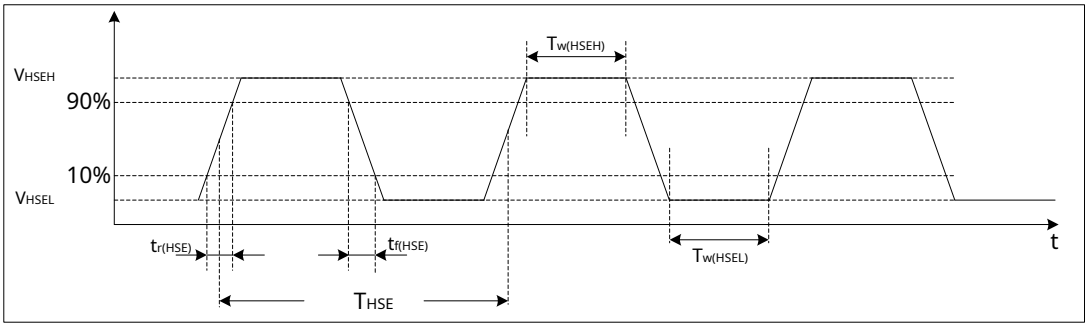
1.The wake-up time is measured from the wake-up time to the time the first instruction is read by the user program.

2.The data is based on assessment results and is not tested in production.

5.3.6.External Clock Source Characteristics

5.3.6.1.External high speed clock

existHSEExternal clock input mode (RCC_CRofHSEENSet), the correspondingIOAs external clock input port.



picture5-1External high-speed clock timing diagram

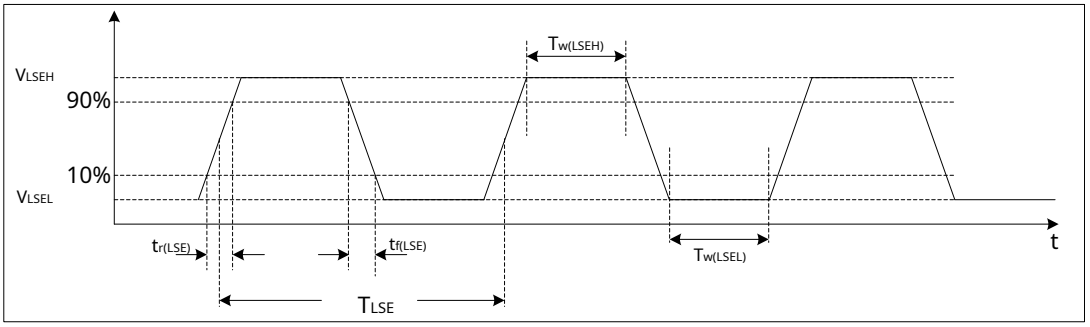
surface5-11External high-speed clock characteristics

symbol	parameter(1)	Minimum	Typical Value	Maximum	unit
f_{HSE_ext}	User external clock frequency	0	4	32	MHz
V_{HSEH}	Input pin high level voltage	0.7*V_{CC}	-	V_{CC}	V
V_{HSEL}	Input pin low level voltage	Vss	-	0.3*V_{CC}	V
$t_{W(HSEH)}$ $t_{W(HSEL)}$	Enter the high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Input rise/fall time	-	-	20	ns

1.Guaranteed by design, not tested in production.

5.3.6.2.External low speed clock

existLSEofbypassmodel(RCC_BDCRofLSEBYPThe low-speed oscillator circuit in the chip stops working.IO As standardGPIOuse.



picture5-2External low-speed clock timing diagram

surface5-12External low speed clock characteristics

symbol	parameter(1)	Minimum	Typical Value	Maximum	unit
f_{LSE_ext}	User external clock frequency	-	32.768	1000	KHz
V_{LSEH}	Input pin high level voltage	0.7*V_{CC}	-	-	V
V_{LSEL}	Input pin low level voltage	-	-	0.3*V_{CC}	V
$t_{W(LSEH)}$ $t_{W(LSEL)}$	Enter the high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	Input rise/fall time	-	-	50	ns

1.Guaranteed by design, not tested in production.

5.3.6.3.External low speed crystal

Can be connected via external32.768 KHzIn the application, the crystal and load capacitors should be as close to the pins as possible.

This can minimize output distortion and startup stabilization time.

surface5-13External Low Speed Crystal Characteristics

symbol	parameter	condition(1)	Minimum	Typical Value	Maximum	unit
I_{DD}	LSEPower consumption	LSE_DRIVER[1:0] = 00	-	100	-	nA
		LSE_DRIVER[1:0] = 01	-	700	-	
		LSE_DRIVER[1:0] = 10	-	1200	-	
		LSE_DRIVER[1:0] = 11	-	1600	-	
$t_{SU(LSE)}$ (3) (4)	Startup time	-	-	3	-	s

1.Crystal/ceramic resonator characteristics are based on the manufacturer's data sheet.

2.Guaranteed by design, not tested in production.

3. $t_{SU(LSE)}$is the start-up time from enabling (by software) until the clock oscillation reaches stability, measured for a standard crystal/resonator. resonance

The device may vary greatly

4.The data is based on assessment results and is not tested in production.

5.3.7.Internal high frequency clock sourceHSIcharacteristic

surface5-14Internal high frequency clock source characteristics

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
f_{HSI}	HSIfrequency	T_A= 25°C, V_{CC}= 3.3 V	23.83(2)	twenty four	24.17(2)	MHz
$\Delta_{Temp(HSI)}$	HSIFrequency temperature drift 24 MHz	V_{CC}= 2.0V ~ 5.5 VT_A= -40 °C ~ 85 °C	- 2(2)	-	2(2)	%
		V_{CC}= 1.7 V ~ 5.5 VT_A = 0 °C ~ 85 °C	- 2(2)	-	2(2)	
		V_{CC}= 1.7 V ~ 5.5 VT_A = -40 °C ~ 85 °C	- 4(2)	-	2(2)	
f_{TRIM} (1)	HSIFine-tuning accuracy	-	-	0.1	-	%
D_{HSI}(1)	Duty Cycle	-	45	-	55	%
$t_{Stab(HSI)}$	HSIStabilization time	-	-	2	4(1)	μs
$I_{DD(HSI)}$ (2)	HSIPower consumption	24 MHz	-	193	-	μA

1.Guaranteed by design, not tested in production.

2.The data is based on assessment results and is not tested in production.

5.3.8.Internal low frequency clock sourceLSIcharacteristic

surface5-15Internal low frequency clock characteristics

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
f_{LSI}	LSIfrequency	T_A= 25°C, V_{CC}= 3.3 V	31.6	32.6	33.6	KHz
$\Delta_{Temp(LSI)}$	LSIFrequency temperature drift	V_{CC}= 1.7 V ~ 5.5 VT_A = 0°C ~ 85°C	- 10(2)	-	10(2)	%

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
		V_{CC}= 1.7 V ~ 5.5 VT_A= -40 °C ~ 85 °C	- 20(2)	-	20(2)	
f_{TRIM} (1)	LSIFine-tuning accuracy	-	-	0.2	-	%
$t_{Stab(LSI)}$ (1)	LSIStabilization time	-	-	150	-	μs
$I_{DD(LSI)}$ (1)	LSIPower consumption	-	-	210	-	nA

1.Guaranteed by design, not tested in production.

2.The data is based on assessment results and is not tested in production.

5.3.9.Memory characteristics

surface5-16Memory characteristics

symbol	parameter	condition	Typical Value	Maximum(1)	unit
t_{prog}	Page program	-	1.0	1.5	ms
t_{ERASE}	Page/sector/mass erase	-	3.5	5.0	ms
I_{DD}	Page program	-	2.1	2.9	mA
	Page/sector/mass erase	-	2.1	2.9	

1.Guaranteed by design, not tested in production.

surface5-17Memory erase and write cycles and data retention

symbol	parameter	condition	Minimum(1)	unit
N_{END}	Erasing times	T_A= -40 °C ~ 85 °C	100	Kcycle
t_{RET}	Data retention period	10 Kcycle T_A= 55 °C	20	Year

1.The data is based on assessment results and is not tested in production.

5.3.10. EFTcharacteristic

symbol	parameter	condition	grade	Typical Value	unit
EFT to IO	-	IEC61000-4-4	A	2	KV
EFT to Power	-	IEC61000-4-4	A	4	KV

5.3.11. ESD & LUcharacteristic

surface5-18 ESD & LUcharacteristic

symbol	parameter	condition	Typical Value	unit
$V_{ESD(HBM)}$	Static discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	6	KV
$V_{ESD(CDM)}$	Static discharge voltage (charging device model)	ESDA/JEDEC JS-002-2018	1	KV

symbol	parameter	condition	Typical Value	unit
$V_{ESD(MM)}$	Static discharge voltage (machine model)	JESD22-A115C	200	V
LU	StaticLatch-Up	JESD78E	200	mA

5.3.12.Port Features

surface5-19 IOStatic characteristics

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
V_{IH}	Input high level voltage	V_{CC}= 1.7 V ~ 5.5 V	0.7*V_{CC}	-	-	V
V_{IL}	Input low level voltage	V_{CC}= 1.7 V ~ 5.5 V	-	-	0.3*V_{CC}	V
V_{hys}	Schmitt hysteresis voltage	-	-	200	-	mV
I_{lkg}	Input leakage current	-	-	-	1	μA
R_{PU}	Pull-up resistor	-	30	50	70	KΩ
R_{PD}	Pull-down resistor	-	30	50	70	KΩ
C_{IO}	Pin capacitance	-	-	5	- -	pF

1.Guaranteed by design, not tested in production.

surface5-20Output voltage characteristics

symbol	parameter(1)	condition	Minimum	Maximum	unit
V_{OL} (2)	COM IOOutput low level	I_{OL}= 20 mA, V_{CC}≥5.0 V	-	0.4	V
V_{OL}		I_{OL}= 8 mA, V_{CC}≥2.7 V	-	0.4	V
V_{OL} (2)		I_{OL}= 4 mA, V_{CC}= 1.8 V	-	0.5	V
V_{OH} (2)	COM IOOutput high level	I_{OH}= 18 mA, V_{CC}≥5.0 V	V_{CC}–0.6	-	V
V_{OH}		I_{OH}= 8 mA, V_{CC}≥2.7 V	V_{CC}–0.4	-	V
V_{OH} (2)		I_{OH}= 4 mA, V_{CC}= 1.8 V	V_{CC}–0.5	-	V

1. IOFor the type, refer to the terms and symbols defined in the pin definition.

2.The data is based on assessment results and is not tested in production.

5.3.13. NRSTPin Characteristics

surface5-21 NRSTPin Characteristics

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
V_{IH}	Input high level voltage	V_{CC}= 1.7 V ~ 5.5 V	0.7*V_{CC}	-	-	V
V_{IL}	Input low level voltage	V_{CC}= 1.7 V ~ 5.5 V	-	-	0.2*V_{CC}	V
V_{hys}	Schmitt hysteresis voltage	-	-	300	-	mV
I_{lkg}	Input leakage current	-	-	-	1	μA
R_{PU}	Pull-up resistor	-	30	50	70	KΩ

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
R_{PD}	Pull-down resistor	-	30	50	70	KΩ
C_{IO}	Pin capacitance	-	-	5	-	pF

1.Guaranteed by design, not tested in production.

ADCcharacteristic

surface5-22 ADCcharacteristic

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
I_{DD}	Power consumption	@1 MSPS	-	300	-	uA
C_{IN}	Internal sample and hold circuit Allow	-	-	5	-	pF
F_{ADC}	Convert clock frequency	V_{CC}= 1.7 V ~ 2.0 V	1	4	8(2)	MHz
		V_{CC}= 2.0 V ~ 5.5 V	1	8	16(2)	MHz
T_{samp} (1)	-	F_{ADC}=8 MHz	0.438	-	29.94	μs
		V_{CC}= 1.7 V ~ 2.0 V	3.5	-	239.5	1/F_{ADC}
		F_{ADC}=16 MHz	0.219	-	14.97	μs
		V_{CC}= 2.0 V ~ 5.5 V	3.5	-	239.5	1/F_{ADC}
T_{conv} (1)	-	-	-	12*Tclk	-	-
T_{adc}	-	-	-	0.5*Tclk	-	-
DNL(2)	-	-	-	±2	-	LSB
INL(2)	-	-	-	±3	-	LSB
Offset(2)	-	-	-	±2	-	LSB

1.Guaranteed by design, not tested in production.

2.The data is based on assessment results and is not tested in production.

5.3.15.Comparator Characteristics

surface5-23Comparator Characteristics(1)

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
V_{IN}	Input voltage range	-	0	-	V_{CC}-1.5	V
t_{START}	Startup time to reach propagation delay specification	-	-	-	5	μs
t_D	Propagation delay	Output low to high	-	-	200	ns
		Output high to low	-	-	150	
V_{offset}	Offset error	-	-	±5	-	mV
V_{hys}	hysteresis	No hysteresis	-	0	-	mV
I_{DD}	Consumption	-	-	70	-	μA

1.Guaranteed by design, not tested in production.

5.3.16.Temperature Sensor Characteristics

surface5-24Temperature Sensor Characteristics

symbol	parameter	Minimum	Typical Value	Maximum	unit
T_{L}(1)	VTS linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30 °C (±5 °C)	0.74	0.76	0.78	V
t_{START} (1)	Start-up time entering in continuous mode	-	70	120	μs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	μs

1.Guaranteed by design, not tested in production.

2.The data is based on assessment results and is not tested in production.

5.3.17.Built-in reference voltage feature

surface5-25Built-in reference voltage feature

symbol	parameter	Minimum	Typical Value	Maximum	unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$T_{start\_vrefint}$	Start time of internal reference voltage	-	10	15	μs
T_{coeff}	Temperature coefficient	-	-	100(1)	ppm/°C
I_{vcc}	Current consumption from V_{CC}	-	12	20	μA

1.Guaranteed by design, not tested in production.

ADCBuilt-in reference voltage feature

surface5-26Built-in reference voltage feature

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
V_{REF15}	Internal 1.5 V reference voltage	T_A= 25 °C V_{CC}= 3.3 V	1.485	1.5	1.515	V
T_{coeff}	Temperature coefficient cient	T_A= -40 °C ~ 85 °C	-	-	120(1)	ppm/°C
$T_{start\_VREFBUF}$	Start time of internal reference voltage	-	-	10	15	μs

1.Guaranteed by design, not tested in production.

COMPBuilt-in reference voltage characteristics (4BitDAC)

surface5-28Built-in reference voltage feature

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
ΔV_{abs}	Absolute variation	-	-	-	±0.5	LSB
$T_{start\_VREFCMP}$	Start time of internal reference volt-age	-	-	10	15	μs

1.Guaranteed by design, not tested in production.

5.3.20.Timer Characteristics

surface5-27Timer Characteristics

symbol	parameter	condition	Minimum	Maximum	unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 24 MHz	41.667	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 24 MHz	-	12	
Res_{TIM}	Timer resolution	TIM1/14	-	16	bit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 24 MHz	0.041667	2730	μs

surface5-28 LPTIMFeatures (Clock SelectionLSI)

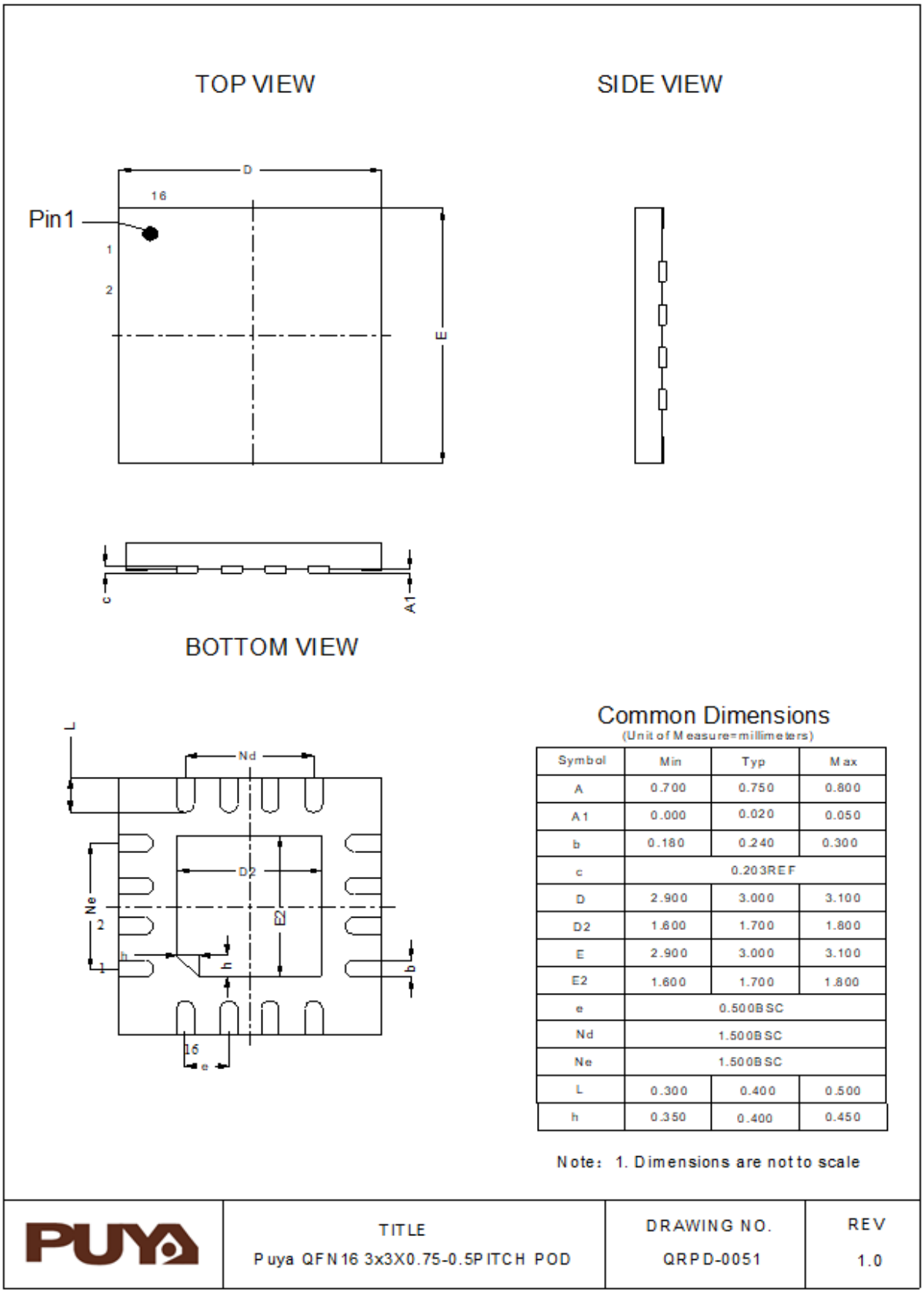
Prescaler	PRESC[2:0]	Minimum overflow value	Maximum overflow value	unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.9456	
/8	3	0.2441	15997.3376	
/16	4	0.4883	32001.2288	
/32	5	0.9766	64002.4576	
/64	6	1.9531	127998.3616	
/128	7	3.9063	256003.2768	

surface5-29 IWDGFeatures (Clock SelectionLSI)

Prescaler	PR[2:0]	Minimum overflow value	Maximum overflow value	unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

6.Packaging information

6.1. QFN16Package size



Common Dimensions

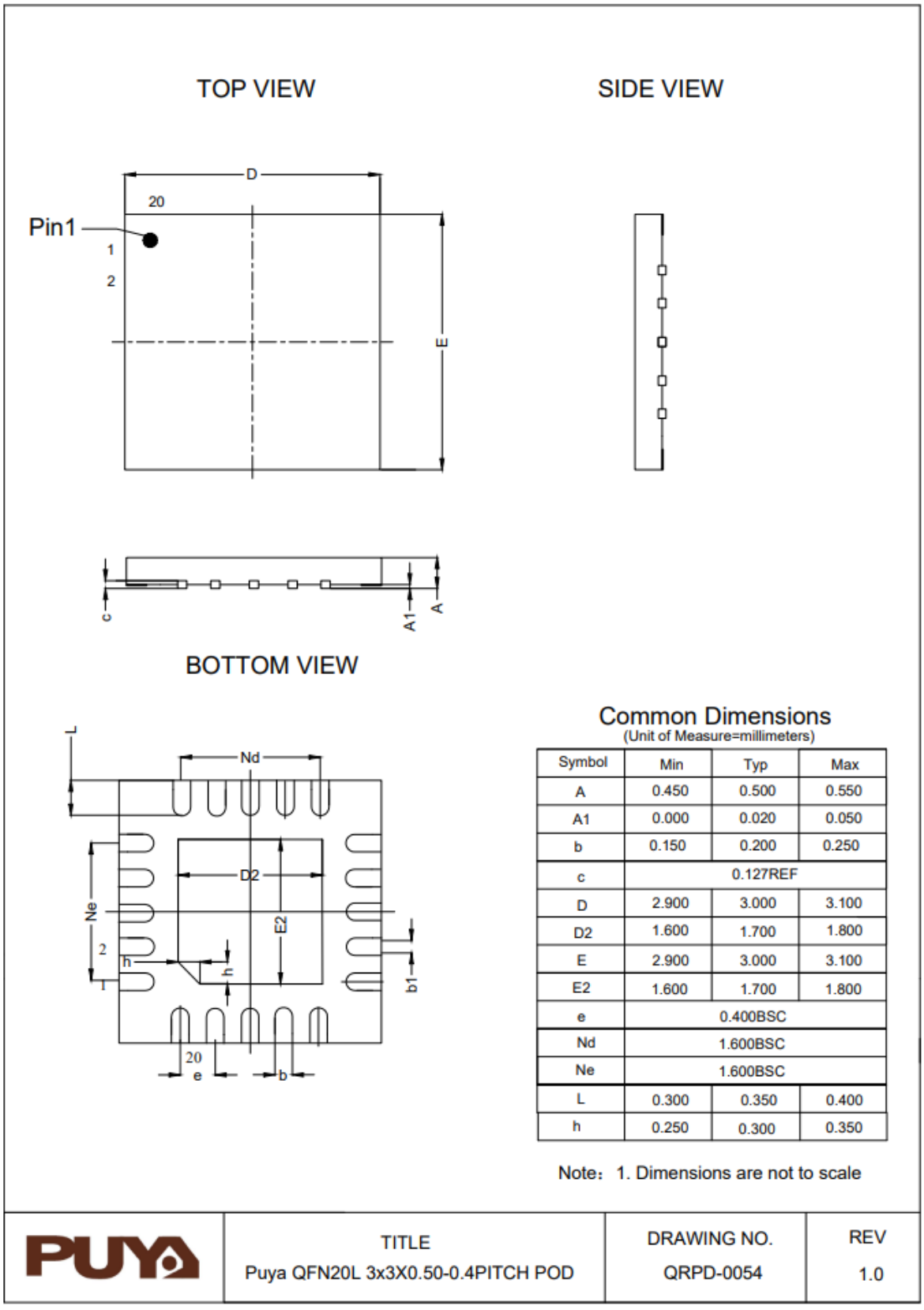
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.180	0.240	0.300
c		0.203REF	
D	2.900	3.000	3.100
D2	1.600	1.700	1.800
E	2.900	3.000	3.100
E2	1.600	1.700	1.800
e		0.500BSC	
Nd		1.500BSC	
Ne		1.500BSC	
L	0.300	0.400	0.500
h	0.350	0.400	0.450

Note: 1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN16 3x3X0.75-0.5PITCH POD	QRPD-0051	1.0

6.2. QFN20Package size



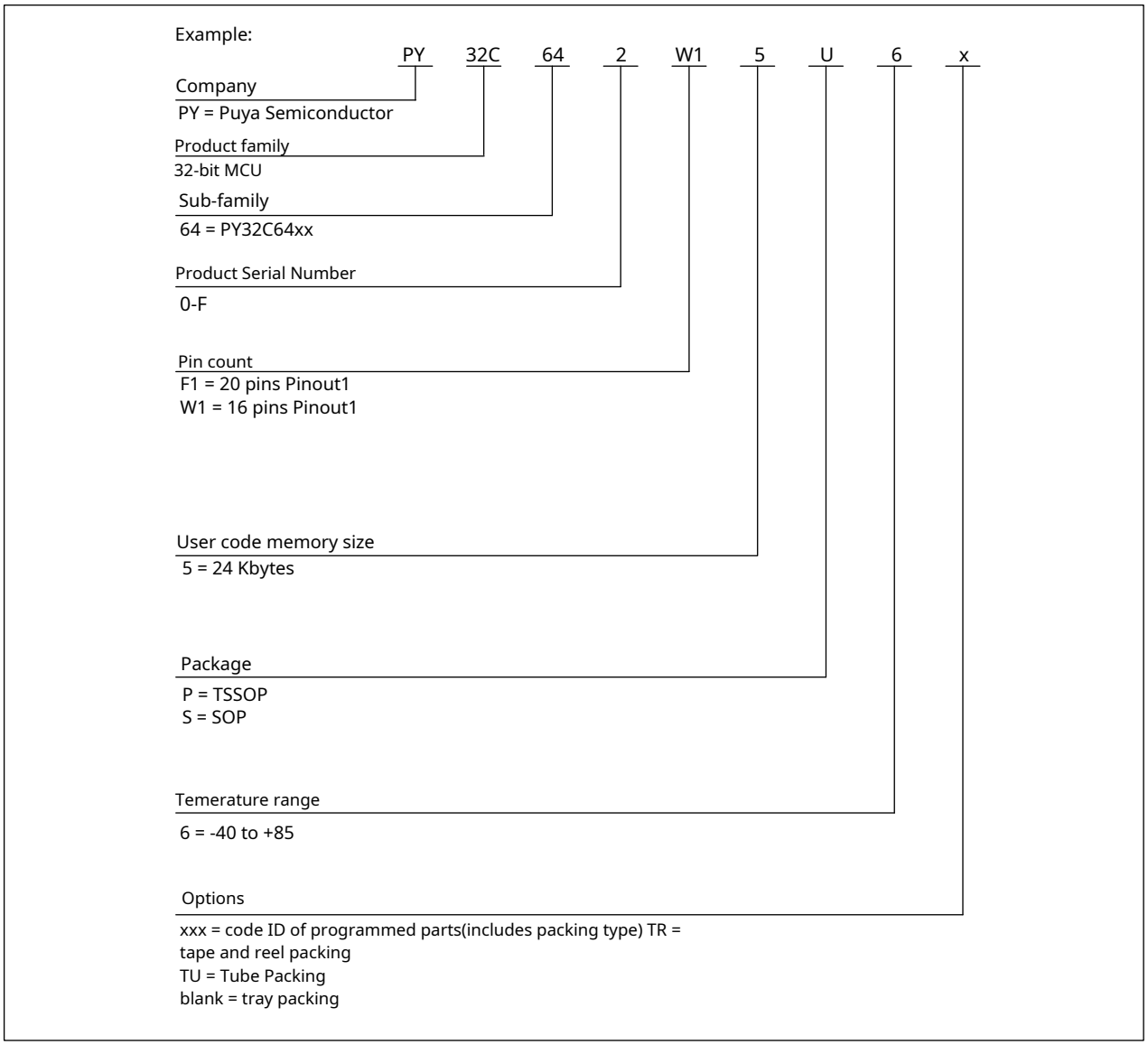
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.450	0.500	0.550
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c		0.127REF	
D	2.900	3.000	3.100
D2	1.600	1.700	1.800
E	2.900	3.000	3.100
E2	1.600	1.700	1.800
e		0.400BSC	
Nd		1.600BSC	
Ne		1.600BSC	
L	0.300	0.350	0.400
h	0.250	0.300	0.350

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN20L 3x3X0.50-0.4PITCH POD	QRPD-0054	1.0

7.Ordering Information



8.Revision History

Version	date	Update Record
V0.1	2023.8.9	First edition

Puya Semiconductor Co., Ltd.

Voice bright