Modeling systems via register machines

for the verification of weak memory models

Elli Anastasiadi [1,2] Samuel Grahn [1]

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firstname.lastname@it.uu.se

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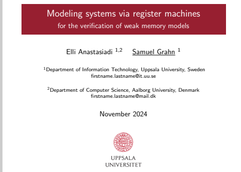
Modeling via Register Machines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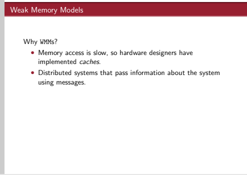
Introduce Elli and Samuel, title

Weak Memory Models

Why `WMMs`?

- Memory access is slow, so hardware designers have implemented *caches*.
- Distributed systems that pass information about the system using messages.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Two situations (next)
The question we want to answer: (next)
(verification problem)
What do we do with undecidability? (next)
Simplify to find a case that is decidable

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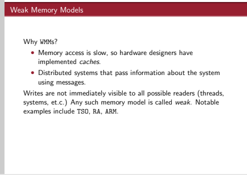
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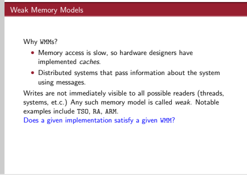
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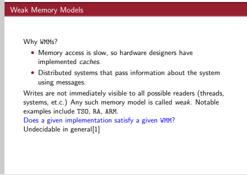

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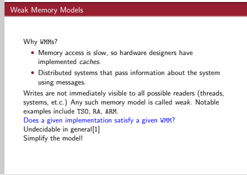
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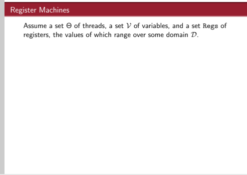
Register Machines

Assume a set Θ of threads, a set $\mathcal{V}$ of variables, and a set $\mathtt{Regs}$ of registers, the values of which range over some domain $\mathcal{D}$.



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Intuitively: FSA with operation labels

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Definition (Operation)

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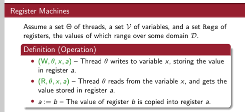
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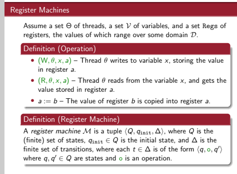
A *register machine* $\mathcal{M}$ is a tuple $\langle Q, q_{\mathtt{init}}, \Delta\rangle$, where Q is the (finite) set of states, $q_{\mathtt{init}} \in Q$ is the initial state, and Δ is the finite set of transitions, where each $t \in \Delta$ is of the form $\langle q, \mathsf{o}, q'\rangle$ where $q, q' \in Q$ are states and o is an operation.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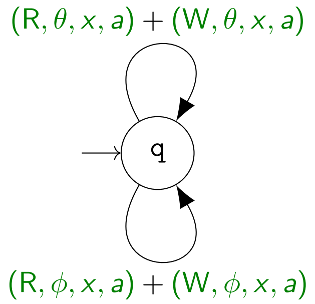
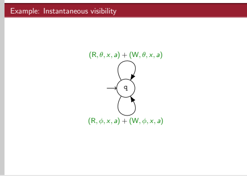
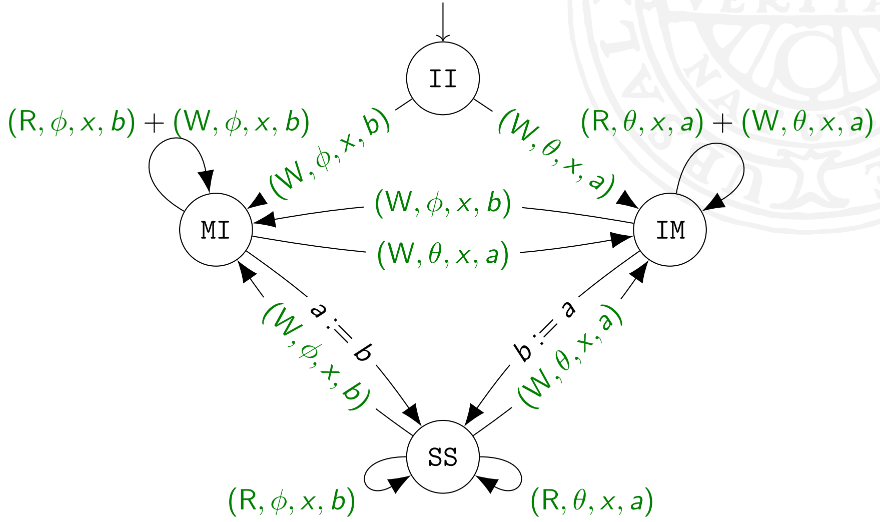
Example: Instantaneous visibility


$$\begin{tikzcd} \arrow[r] & q \arrow[loop above, "(\mathrm{R},\theta,x,a)+(\mathrm{W},\theta,x,a)"] \arrow[loop below, "(\mathrm{R},\phi,x,a)+(\mathrm{W},\phi,x,a)"] \end{tikzcd}$$



Example: Single state, two threads that can read and write from the same register

Example: MSI Protocol


II
MI
IM
SS
$(\mathsf{R}, \phi, x, b) + (\mathsf{W}, \phi, x, b)$
(W, ϕ, x, b)
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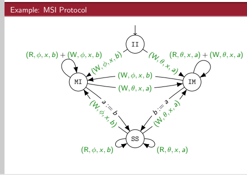
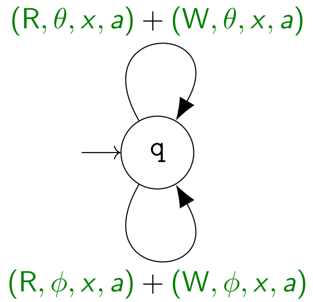


Each thread is in one of three states:
Invalid – Variable not in cache
Modified – Variable owned and controlled
Shared – Read access, shared with others

Modeling via Register Machines
└─Modeling

Thread-local Memory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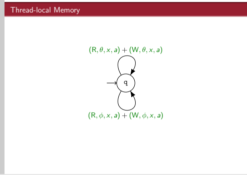
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Previous example: single-state read/write In a real system: effects not immediately visible (e.g. cache)

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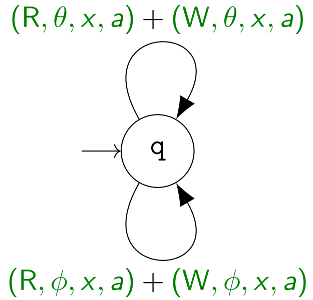
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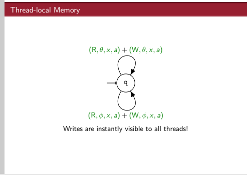
Writes are instantly visible to all threads!



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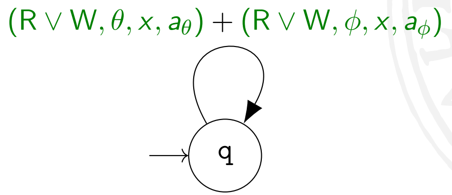
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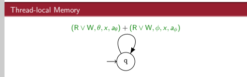

Create thread local registers
(next) Allow copying information between threads
(next) Problem!
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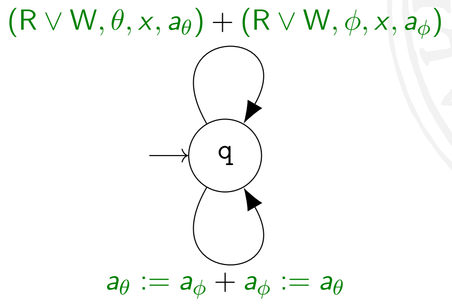
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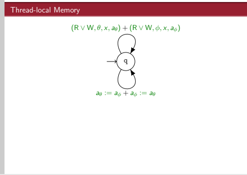

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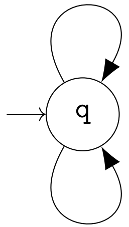
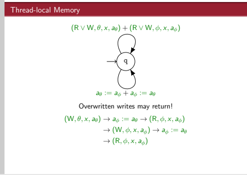


$$a_\theta := a_\phi + a_\phi := a_\theta$$

Overwritten writes may return!

$$\begin{aligned}(\mathsf{W}, \theta, x, a_\theta) &\to a_\phi := a_\theta \to (\mathsf{R}, \phi, x, a_\phi)\\ &\to (\mathsf{W}, \phi, x, a_\phi) \to a_\phi := a_\theta\\ &\to (\mathsf{R}, \phi, x, a_\phi)\end{aligned}$$



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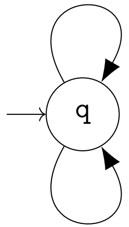

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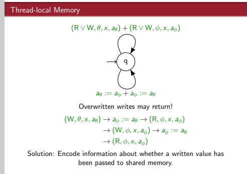
Solution: Encode information about whether a written value has been passed to shared memory.



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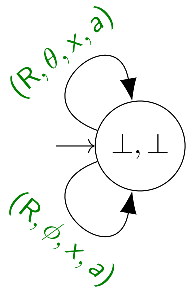

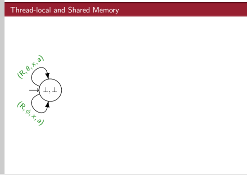

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Both Write and read locally SAY: t is either θ or ϕ

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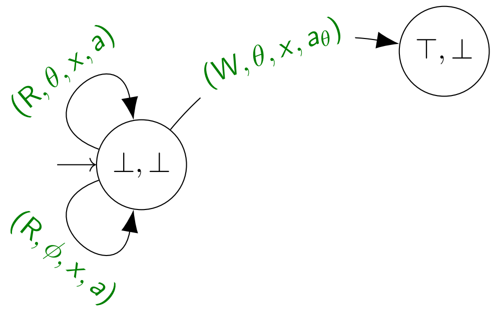

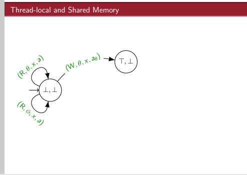

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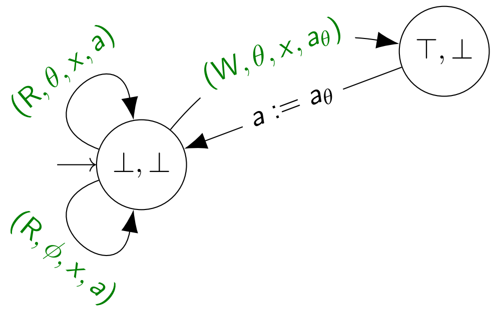

$$\begin{tikzcd}
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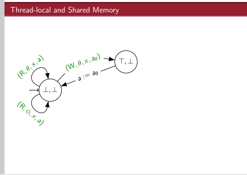
\end{tikzcd}$$



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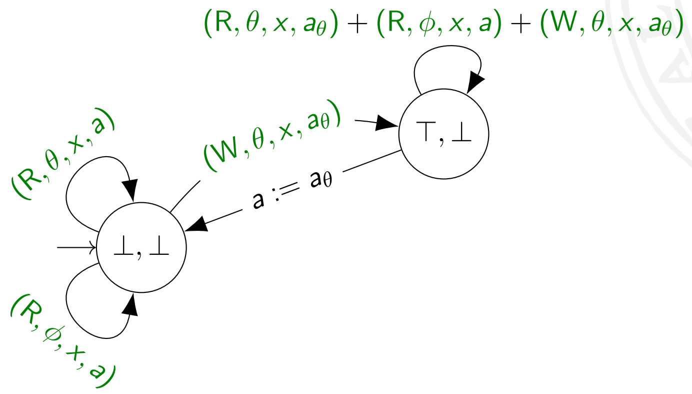

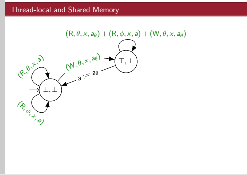

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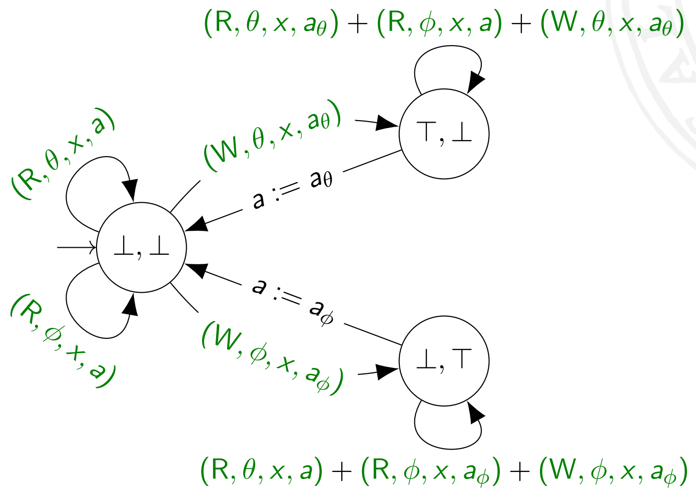
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2024-10-30

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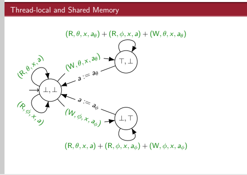
└Modeling
└Thread-local and Shared Memory



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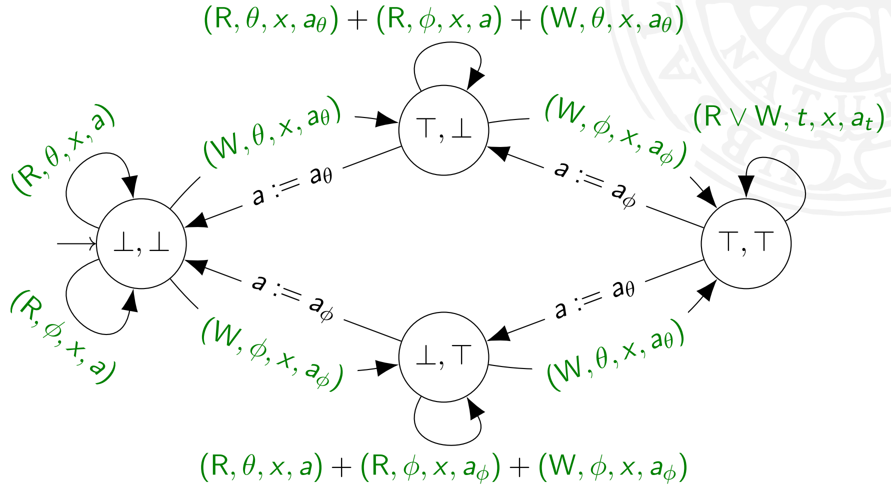
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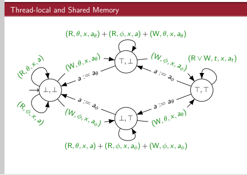
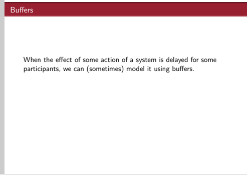
$a := a_\phi$
$a := a_\theta$
(R,ϕ,x,a)
$(\mathsf{W},\phi,x,a_\phi)$
$(\mathsf{W},\theta,x,a_\theta)$
$\bot,\top$
$(\mathsf{R},\theta,x,a)+(\mathsf{R},\phi,x,a_\phi)+(\mathsf{W},\phi,x,a_\phi)$



Initial state, none have written. Introduce a, memory
(next) θ writes. (storing in state)
(next) Copy back.
(next) Reads and writes
(next) Symmetricaly for ϕ
(next) From each of the two (end) states, The *other* thread writes.
Both Write and read locally SAY: t is either θ or ϕ

Buffers

When the effect of some action of a system is delayed for some participants, we can (sometimes) model it using buffers.



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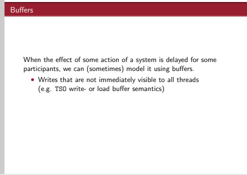
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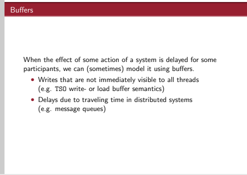
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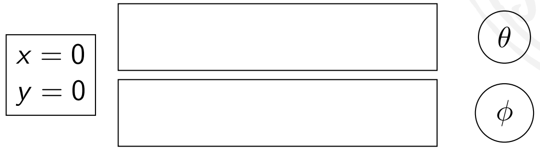
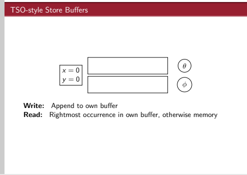
TSO-style Store Buffers

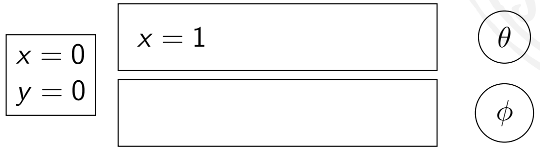


Write: Append to own buffer
Read: Rightmost occurrence in own buffer, otherwise memory



Values in memory, Buffers, one for each thread. DO SOME READS AT EVERY STEP

TSO-style Store Buffers



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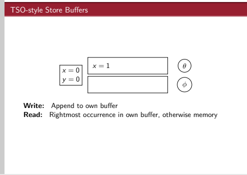

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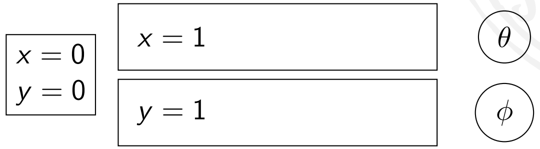

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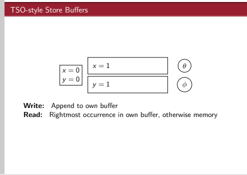

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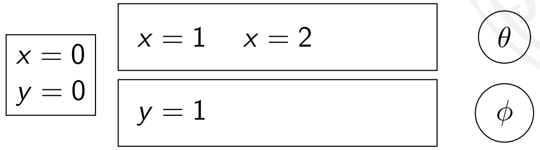

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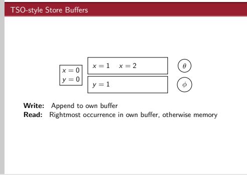

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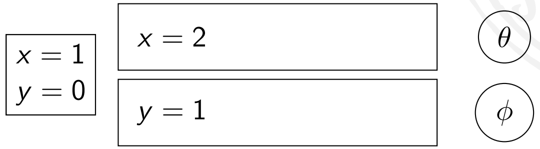

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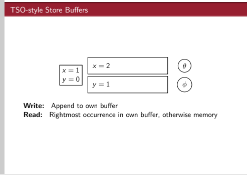
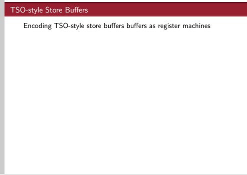


Memory (left) Two threads (right), each with a store buffer (middle)
(Write = append, Read = rightmost)
(next) Say θ writes $x = 1$.
If θ would try to read x, it would read 1. ϕ would read 0.
(next) ϕ writes. (next) θ writes again. The only remaining part is:
(next) Handling buffers: take first message and apply it to memory.

TSO-style Store Buffers

Encoding TSO-style store buffers buffers as register machines


TSO-style Store Buffers

Encoding TSO-style store buffers buffers as register machines

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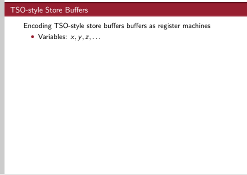
- Variables: $x, y, z, \ldots$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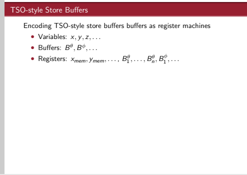
- Variables: $x, y, z, \ldots$
- Buffers: $B^\theta, B^\phi, \ldots$
- Registers: $x_{mem}, y_{mem}, \ldots,\ B^\theta_1, \ldots, B^\theta_n, B^\phi_1, \ldots$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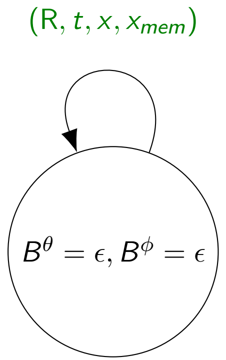
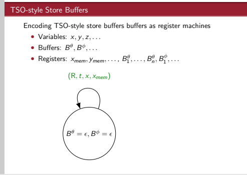

$(\mathrm{R}, t, x, x_{mem})$
$B^\theta = \epsilon, B^\phi = \epsilon$

2024-10-30

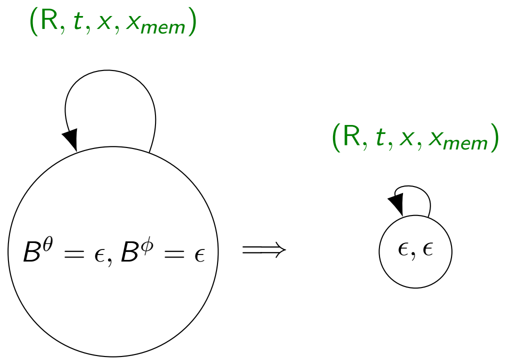
Modeling via Register Machines
└─Modeling
└─TSO-style Store Buffers

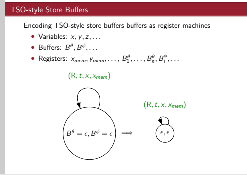


TSO-style Store Buffers

Encoding TSO-style store buffers buffers as register machines

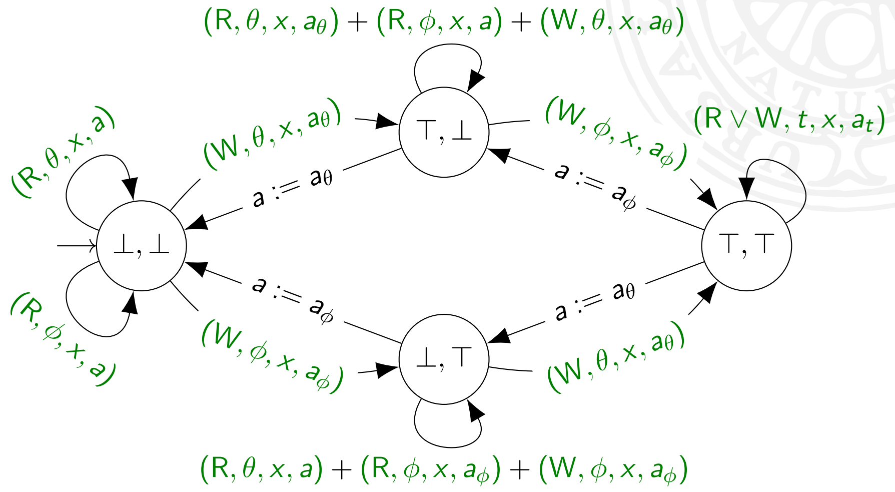
- Variables: $x, y, z, \ldots$
- Buffers: $B^\theta, B^\phi, \ldots$
- Registers: $x_{mem}, y_{mem}, \ldots, B_1^\theta, \ldots, B_n^\theta, B_1^\phi, \ldots$

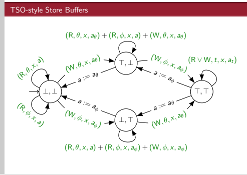

$(\mathrm{R}, t, x, x_{mem})$
$B^\theta = \epsilon, B^\phi = \epsilon$
$\Longrightarrow$
$(\mathrm{R}, t, x, x_{mem})$
ϵ, ϵ



Variables (next)
Buffers = sequence of var names, one for each thread (next)
Registers: one for each variable, and one for each buffer slot (bounded buffers). (next)
We store the buffer contents as part of the state. (next)
But draw it smaller.

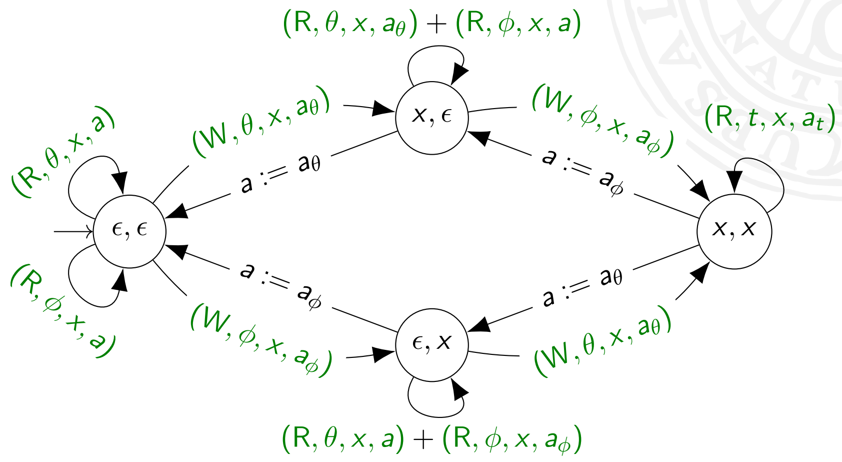
TSO-style Store Buffers

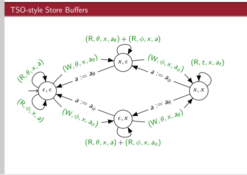

$$\begin{tikzcd}
 & \top,\bot \arrow[loop above, "{(R,\theta,x,a_\theta)+(R,\phi,x,a)+(W,\theta,x,a_\theta)}"] \arrow[dl, "a:=a_\theta"'] \arrow[dr, "{(W,\phi,x,a_\phi)}"] & \\
\bot,\bot \arrow[loop above, "{(R,\theta,x,a)}"] \arrow[loop below, "{(R,\phi,x,a)}"] \arrow[ur, "{(W,\theta,x,a_\theta)}"] \arrow[dr, "{(W,\phi,x,a_\phi)}"'] & & \top,\top \arrow[loop above, "{(R\vee W,t,x,a_t)}"] \arrow[ul, "a:=a_\phi"'] \arrow[dl, "a:=a_\theta"] \\
 & \bot,\top \arrow[loop below, "{(R,\theta,x,a)+(R,\phi,x,a_\phi)+(W,\phi,x,a_\phi)}"] \arrow[ul, "a:=a_\phi"] \arrow[ur, "{(W,\theta,x,a_\theta)}"'] &
\end{tikzcd}$$



We go back and consider the register machine from the context of buffers. Specific instance of the store-buffer: Two threads (i.e. two buffers), one variable, buffer size 1.

TSO-style Store Buffers

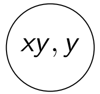


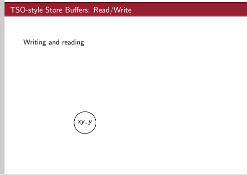


Note, we remove the write loops, as we consider the buffer to be full!
Larger buffers!

TSO-style Store Buffers: Read/Write

Writing and reading





TSO-style Store Buffers: Read/Write

Writing and reading

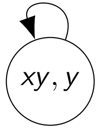
xy, y

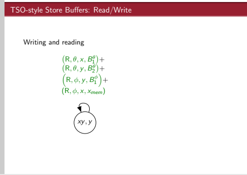
Assume a bound $n > 2$.
From this state, we may read (point out each read) (next)
θ writes (next)
ϕ writes (next)

TSO-style Store Buffers: Read/Write

Writing and reading

$$(\mathsf{R}, \theta, x, B_1^\theta)+$$
$$(\mathsf{R}, \theta, y, B_2^\theta)+$$
$$\left(\mathsf{R}, \phi, y, B_1^\phi\right)+$$
$$(\mathsf{R}, \phi, x, x_{mem})$$





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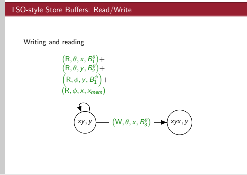
TSO-style Store Buffers: Read/Write

Writing and reading

$$
\begin{array}{l}
(\mathrm{R}, \theta, x, B_1^{\theta})+ \\
(\mathrm{R}, \theta, y, B_2^{\theta})+ \\
\left(\mathrm{R}, \phi, y, B_1^{\phi}\right)+ \\
(\mathrm{R}, \phi, x, x_{mem})
\end{array}
$$

$$\begin{tikzcd}
xy, y \arrow[loop above] \arrow[r, "{(\mathrm{W}, \theta, x, B_3^{\theta})}"] & xyx, y
\end{tikzcd}$$


TSO-style Store Buffers: Read/Write
Writing and reading
$(\mathrm{R}, \theta, x, B_1^{\theta})+$ $(\mathrm{R}, \theta, y, B_2^{\theta})+$ $\left(\mathrm{R}, \phi, y, B_1^{\phi}\right)+$ $(\mathrm{R}, \phi, x, x_{mem})$
xy, y $(\mathrm{W}, \theta, x, B_3^{\theta})$ xyx, y

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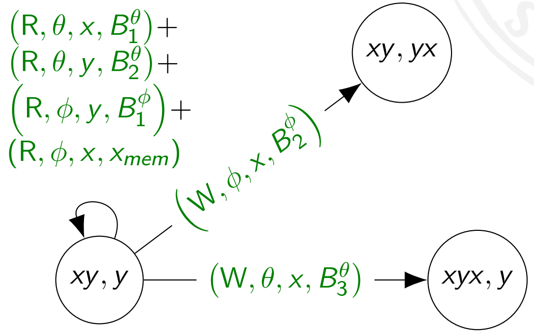
$(\mathrm{R}, \theta, x, B_1^\theta)+$
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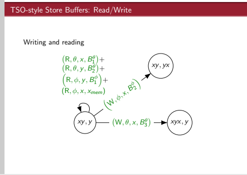
$(\mathrm{R}, \phi, y, B_1^\phi)+$
$(\mathrm{R}, \phi, x, x_{mem})$
xy, yx
$(\mathrm{W}, \phi, x, B_2^\phi)$
xy, y
$(\mathrm{W}, \theta, x, B_3^\theta)$
xyx, y



Assume a bound $n > 2$.
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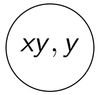
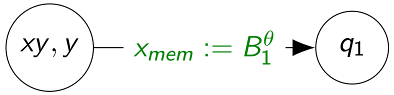
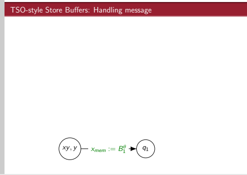
TSO-style Store Buffers: Handling message



Start from the same state.
Handle a message: either from θ or ϕ.
Example: show for θ.
(next) Since first message is x, copy first buffer register to x_{mem}.
DISJOINT sequence of states, not appearing anywhere else! (next) Copy second to first
(next) And so on
(next) Until the final copy
Where we have removed the message from the state.

TSO-style Store Buffers: Handling message





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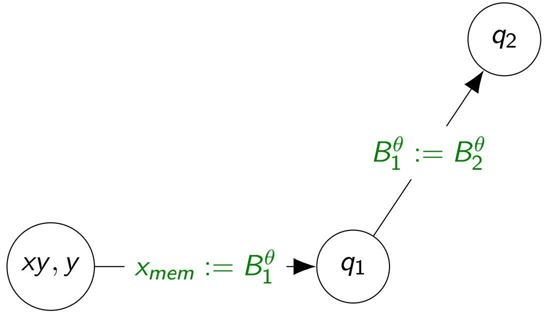

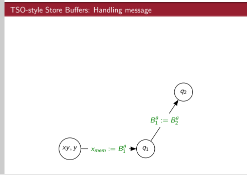

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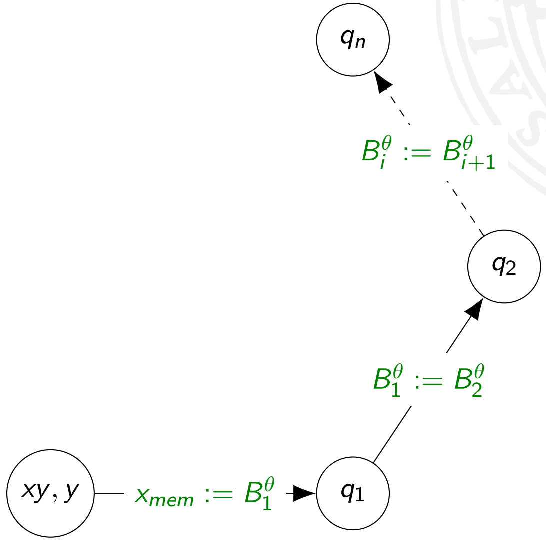
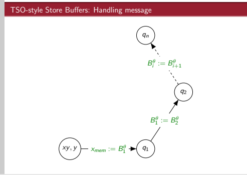

$$\begin{tikzcd} & & q_n \\ & & & q_2 \arrow[ul, dashed, "B_i^\theta := B_{i+1}^\theta"] \\ xy, y \arrow[r, "x_{mem} := B_1^\theta"] & & q_1 \arrow[ur, "B_1^\theta := B_2^\theta"] \end{tikzcd}$$



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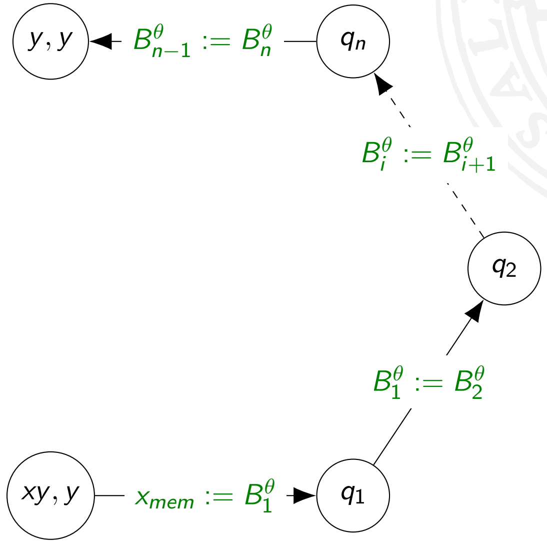
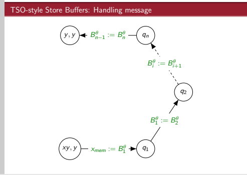
TSO-style Store Buffers: Handling message


y, y
$B^{\theta}_{n-1} := B^{\theta}_{n}$
q_n
$B^{\theta}_{i} := B^{\theta}_{i+1}$
q_2
$B^{\theta}_{1} := B^{\theta}_{2}$
xy, y
$x_{mem} := B^{\theta}_{1}$
q_1

Modeling via Register Machines
└Modeling
└TSO-style Store Buffers: Handling message



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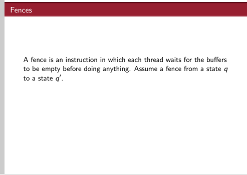
Where we have removed the message from the state.

Fences

A fence is an instruction in which each thread waits for the buffers to be empty before doing anything. Assume a fence from a state q to a state q'.



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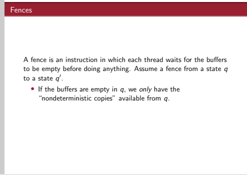
- If the buffers are empty in q, we *only* have the "nondeterministic copies" available from q.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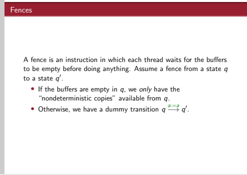
2024-10-30

Modeling via Register Machines
└Modeling
└Fences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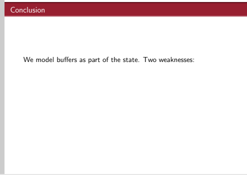
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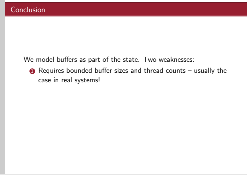

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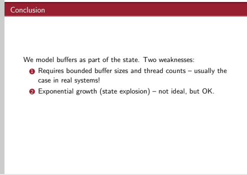
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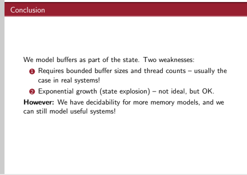
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