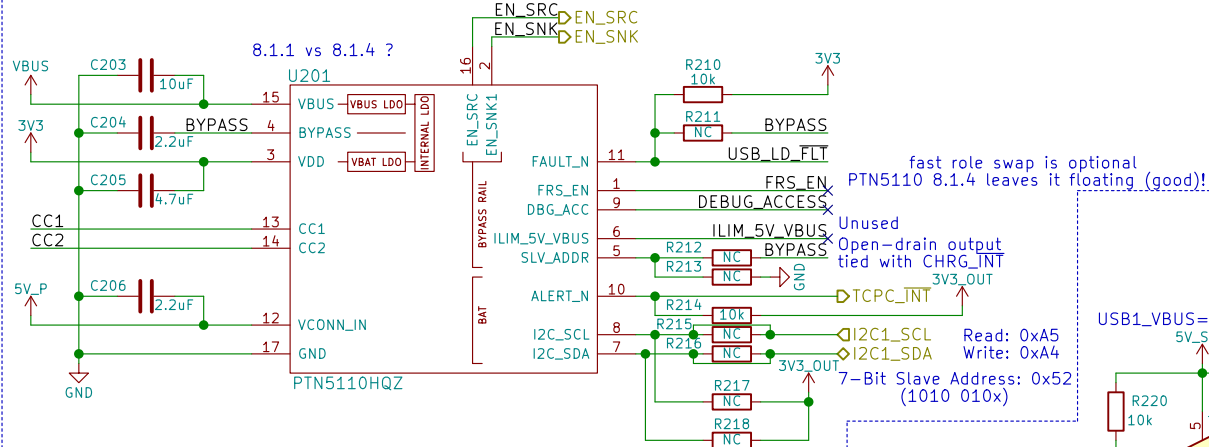


USB-C TCPC - Config Channel (CC) and PD Role Controller

USB-C

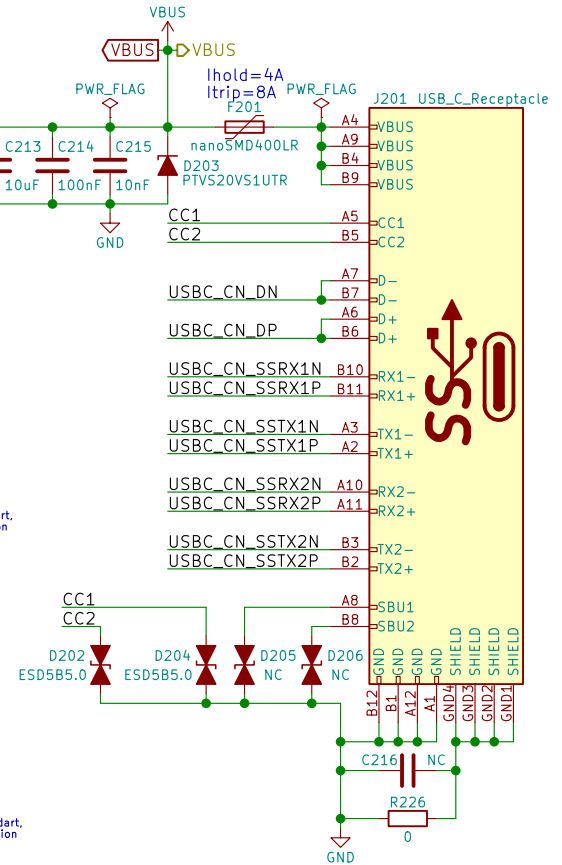
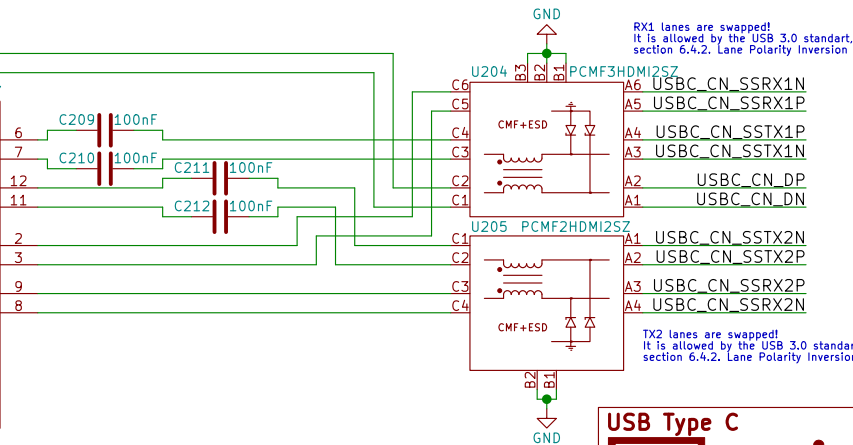
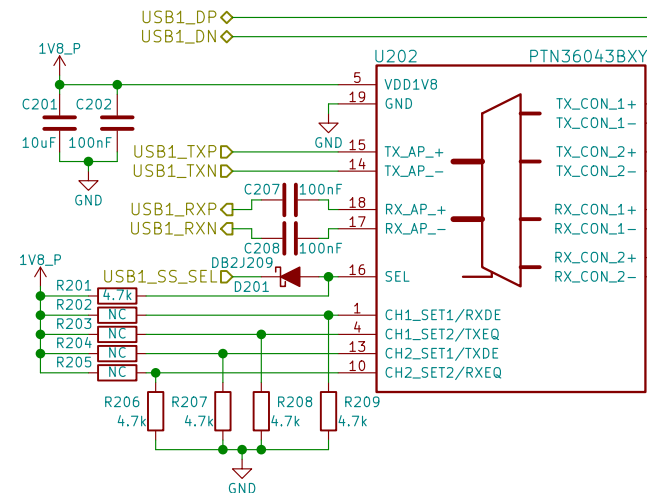


"Under dead battery operation, PTN5110 applies voltage clamps to both CC pins so that the system may receive power as a Sink. To support platforms with buck-boost configuration, PTN5110 asserts EN_SNK1 pin based on validity of VBUS voltage (facilitates 5 V VBUS sinking)."

fast role swap is optional
PTN5110 8.1.4 leaves it floating (good)!

Unused
Open-drain output
tied with CHRG_INT
3V3_OUT
Read: 0xA5
Write: 0xA4
7-Bit Slave Address: 0x52
(1010 010x)

Initialize as the UFP (device)
read CC_STATUS to determine role
use Host Negotiation Protocol (HNP)
to become an DFP (host)
∴ USB ID is effectively unused
⇒ Legacy devices would "wait" for this
⇒ If CC initializes as UFP then no HNP needed



USB Type C

Purism

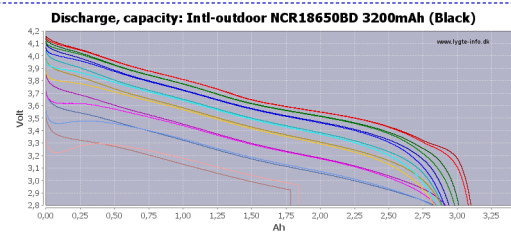
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Sheet: /USB-C/
File: usb-c.sch

Size: A4
KiCad E.D.A. kicad 4.0.7

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christian.schilmoeller@puri.sm

Rev: v0.1.0
Id: 2/24



```
use AUTO_DPDM_EN
to auto-detect IINLIM
```

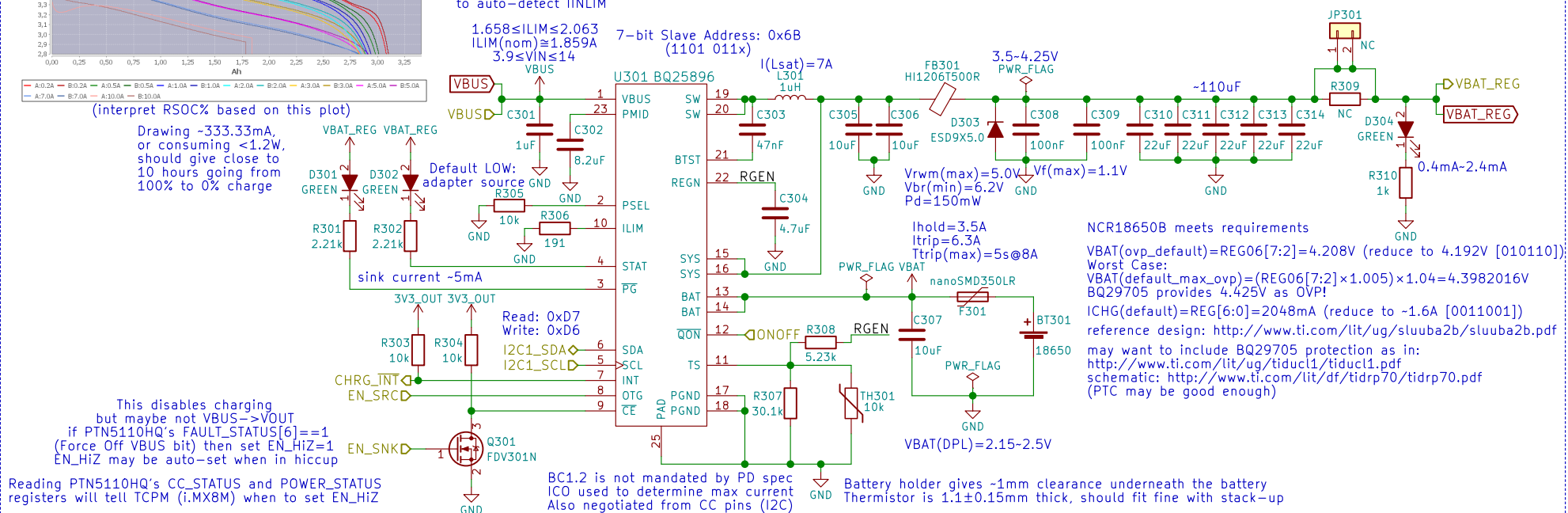
$$1.658 \leq ILIM \leq 2.063$$

$$ILIM(nom) \cong 1.859A$$

$$3.9 < V_{IN} \leq 14$$

7-bit Slave Address: 0x6B
(1101 011x)

Battery Charge Controller



Reading PTN5110HQ's CC_STATUS and POWER_STATUS registers will tell TCPM (i.MX8M) when to set EN_HiZ

Also, reading PTN5110HQ's CC_STATUS and POWER_STATUS registers will tell TPCM (i.MX8M) when to set OTG_CONFIG=1 (this will also happen when PTN5110HQ sets EN_SRC HIGH)

BC1.2 is not mandated by PD spec
ICO used to determine max current
Also negotiated from CC pins (I2C)

Battery holder gives ~1mm clearance underneath the battery
Thermistor is 1.1 ± 0.15 mm thick, should fit fine with stack-up

Battery holder seems to fit up to ~68.88mm long batteries
need to test 18650 protected cells which are ~69.35mm long

NCR18650B meets requirements

VBAT(ovp_default)=REG06[7:2]=4.208V (reduce to 4.192V [010110]);
 Worst Case:
 VBAT(default_max_ovp)=(REG06[7:2]×1.005)×1.04=4.3982016V
 BQ29705 provides 4.425V as OVP!
 ICHG(default)=REG[6:0]=2048mA (reduce to ~1.6A [0011001])
 reference design: <http://www.ti.com/lit/ug/sluuba2b/sluuba2b.pdf>
 may want to include BQ29705 protection as in:
<http://www.ti.com/lit/ug/tiduc11/tiduc11.pdf>
 schematic: <http://www.ti.com/lit/df/tidrp70/tidrp70.pdf>
 (PTC may be good enough)

Battery



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Sheet: /Battery/
File: battery.sch

Size: A4	Date: 2018-06-18
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angus.ainslie@puri.sm
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christian.schilmoeller@puri.sm

Rev: v0.1.0
Id: 3/24

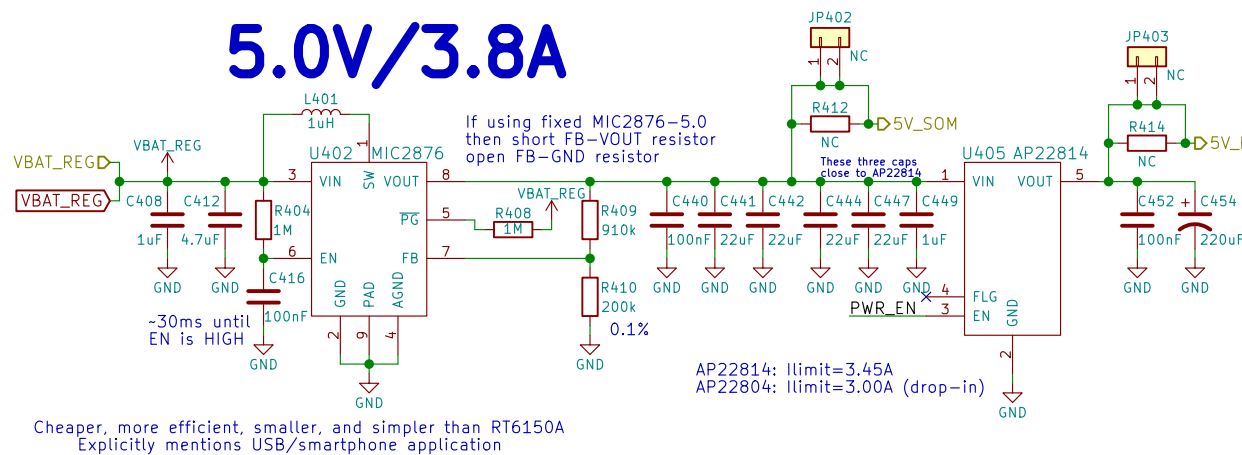
3.3V/3A



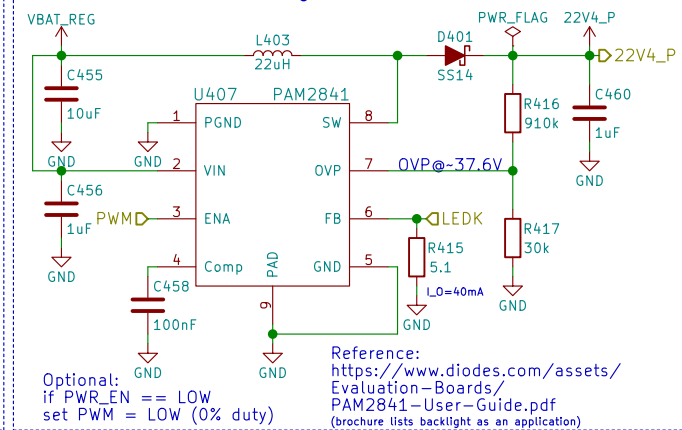
1.8V/600mA



5.0V/3.8A



22.4V/40mA



2.8V/150mA



Power

Power

Purism

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Sheet: /Power/
File: power.sch

Size: A4
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Date: 2018-06-18

Rev: v0.1.0

Id: 4/24

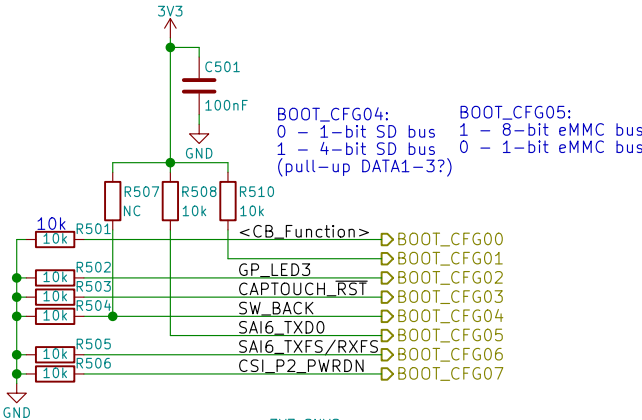
eric.kuzmenko@puri.sm

angus.ainslie@puri.sm

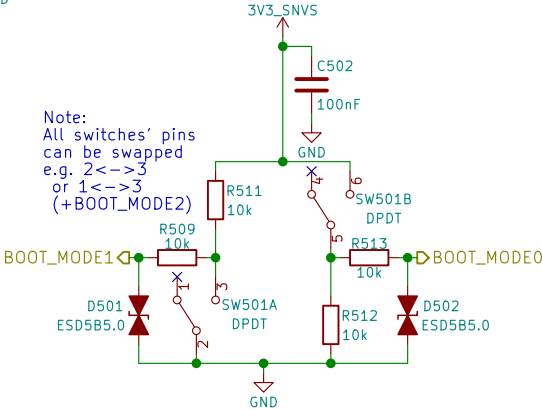
nicole.farber@puri.sm

christian.schilmoeller@puri.sm

Boot Config



BOOT_CFG04: 0 - 1-bit SD bus
1 - 4-bit SD bus (pull-up DATA1-3?)
BOOT_CFG05: 1 - 8-bit eMMC bus
0 - 1-bit eMMC bus



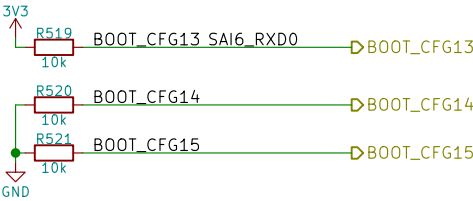
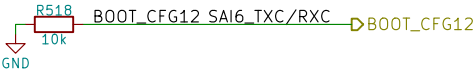
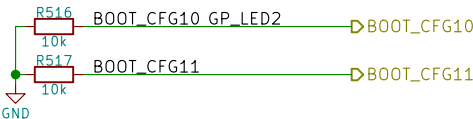
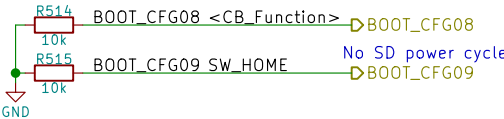
Note:
All switches' pins
can be swapped
e.g. 2<->3
or 1<->3
(+BOOT_MODE2)

2->1: eMMC 2->3: USB (Serial Downloader)	
BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved


Only eMMC

BOOT_CFG[14:12]		Boot device			
001		SD/eSD			
010		MMC/eMMC			
011		NAND			

Fuse	Config	Definition	GPIO ¹	Shipped value	Settings
BOOT_CFG[11:10]	OEM	USDHC port selection	Yes	00	00 - USDHC-1 01 - USDHC-2 10 - USDHC-3 else - reserved



Boot Configuration



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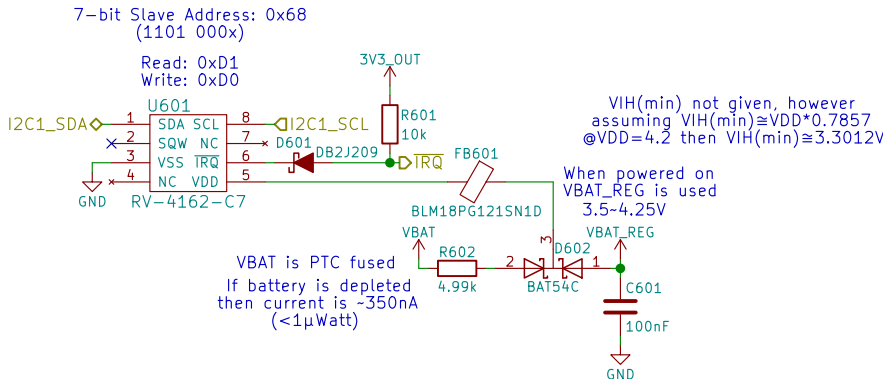
Sheet: /Boot Config/
File: boot.sch

Size: A4
KiCad E.D.A. kicad 4.0.7

eric.kuzmenko@puri.sm
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christian.schilmoeller@puri.sm

Rev: v0.1.0
Id: 5/24

Real-Time Clock



Note:
Datasheet says slave address is 0xD0 with a R/W bit appended, since 0xD must be 4-bits wide the actual 7-bit address is 0x68 (110 1000), and becomes 0xD0 during a write operation (1101 0000)

Reference:
https://github.com/HIO-Project/linux-imx6-nano-imx_3.10.17_1.0.1_ga/blob/8848e94b2f889fe44f6736e2d4c98851a2282275/arch/arm/boot/dts/imx6qdl-mtp.dtsi#L351

RTC



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Sheet: /RTC/

File: rtc.sch

Size: A4	Date: 2018-06-18
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eric.kuzmenko@puri.sm

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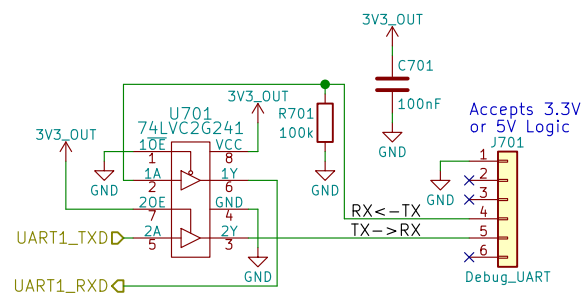
nicole.ferber@puri.sm

christian.schilmoeller@puri.sm

Rev: v0.1.0

Id: 6/24

The diagram shows a 74LVC2G24 inverter (U701) used as a level shifter. The input is UART1_TXDD (3.3V) connected to pin 1A. The output of pin 1Y is connected to RX of the J701 connector. The input of pin 2A is connected to TX of the J701 connector. The output of pin 2Y is connected to TX of the J701 connector. The inverter's VCC is connected to 3V3_OUT and its GND to GND. A 10F capacitor is connected between the input and output. A 100k resistor (R701) is connected between the output and 3V3_OUT. A 100nF capacitor (C701) is connected between the output and GND. The J701 connector is labeled 'Accepts 3.3V or 5V Logic' and 'Debug_UART'.



 Purism

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Id: 7/24

JTAG



JTAG



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Sheet: /JTAG/

File: jtag.sch

Size: A4

Date: 2018-06-18

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Rev: v0.1.0

Id: 8/24

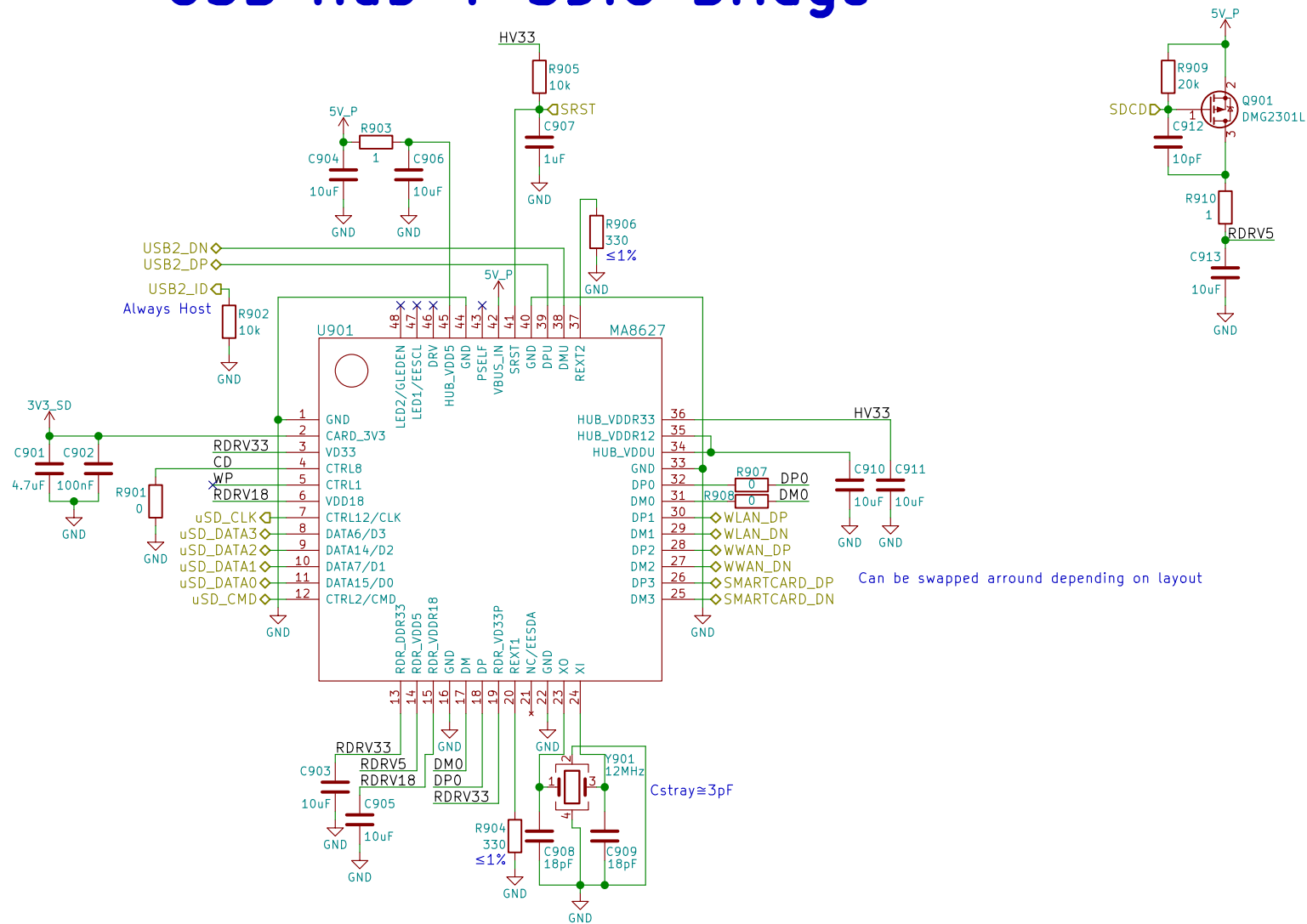
eric.kuzmenko@puri.sm

angus.ainstlie@puri.sm

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christian.schilmoeller@puri.sm

USB Hub + SDIO Bridge



USB Hub + SDIO Bridge



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Sheet: /USB Hub + SDIO Bridge/

File: usb_hub_sdio.sch

Size: A4	Date: 2018-06-18
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Size: A1	Date:
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eric.kuzmenko@puri.sm

angus.ainslie@puri.sm

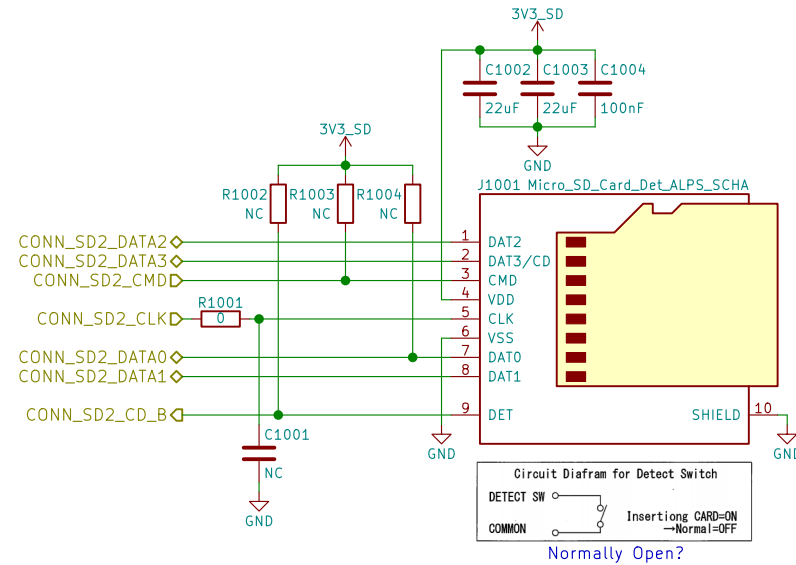
nicole.faerber@puri.sm

christian.schilmoeller@puri.sm

Rev: v0.1.0

Id: 9/24

μSD



uSD Card



Purism

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Sheet: /uSD Card/

File: sd.sch

Size: A4 Date: 2018-06-18

KiCad E.D.A. kicad 4.0.7

eric.kuzmenko@puri.sm

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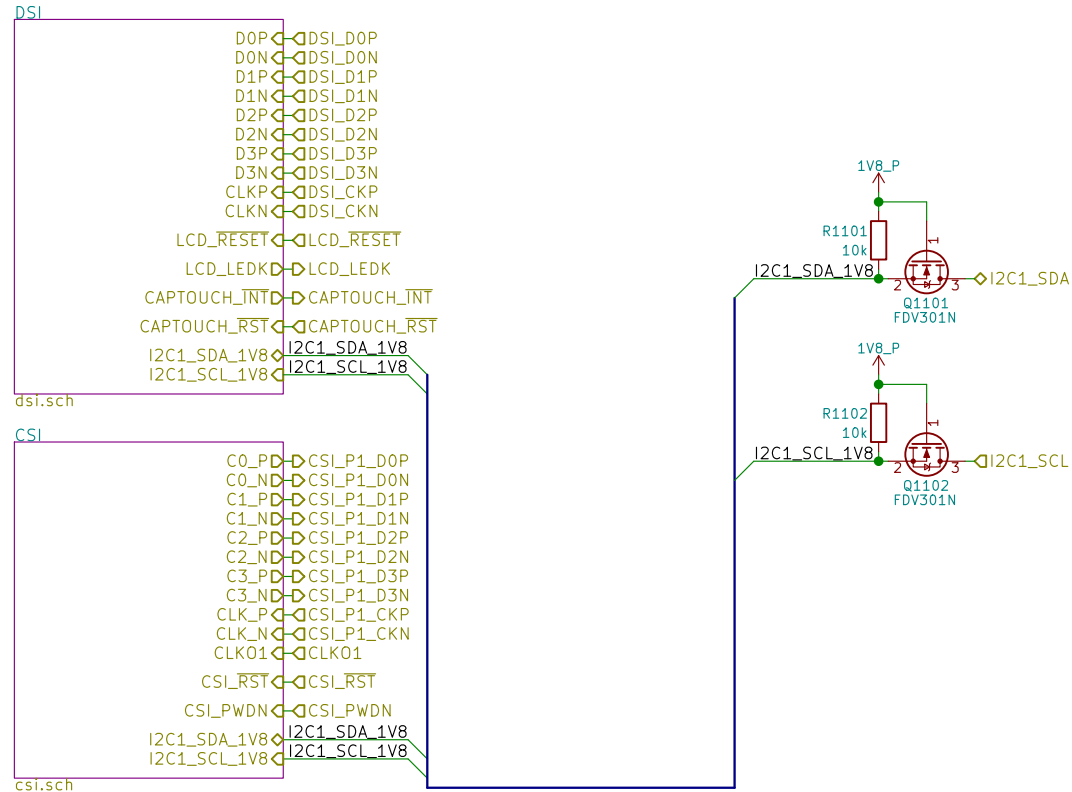
nicole.ferber@puri.sm

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Rev: v0.1.0

Id: 10/24

MIPI



MIPI



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Sheet: /MIPI/

File: mipi.sch

Size: A4 Date: 2018-06-18

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eric.kuzmenko@puri.sm

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nicole.ferber@puri.sm

christian.schilmoeller@puri.sm

Rev: v0.1.0

Id: 11/24

Display & Touch Controller

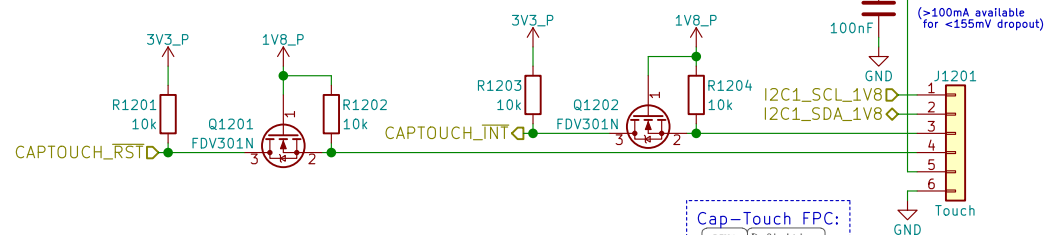
LCD PN:
Shenzhen Jinghong Electronics Co., Ltd.
JH057N00900

Note:
No power-up sequence is
given in the spec sheet

7-bit Slave Address: 0x5D
(1011 101x)

Read: 0xBB
Write: 0xBA

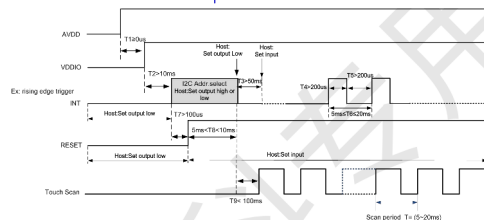
Cap-Touch Controller IC PN:
Goodix GT5688



The upper 7 bits are the address,
and bit 0 is used to select read or write.
GT5688 has two slave device addresses to choose from:

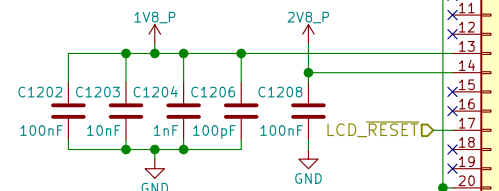
	7-Bit Address	8-Bit Write Address	8-Bit Read Address
INT LOW	0x5D	0xBA	0xBB
INT HIGH	0x14	0x28	0x29

Every time you power on or reset, you need to
use the INT pin to set the I2C address:

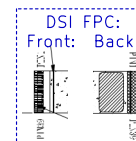
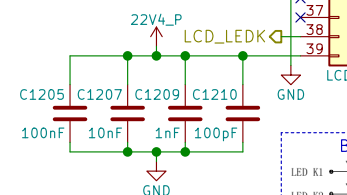


Pin#	Definition
1	SCL
2	SDA
3	INT
4	RESET
5	VID02, S5
6	GND

Front: Back:



100Ω Differential Impedance



Backlight Array:



Display_JH057N00900

DISP1201

5,7 "
RGB
720 x 1440
pixels

FPC6
Touch

FPC39
Display +
Backlight

MIPI DSI

Purism

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Sheet: /MIPI/DSI/

File: dsi.sch

Size: A4 Date: 2018-06-18

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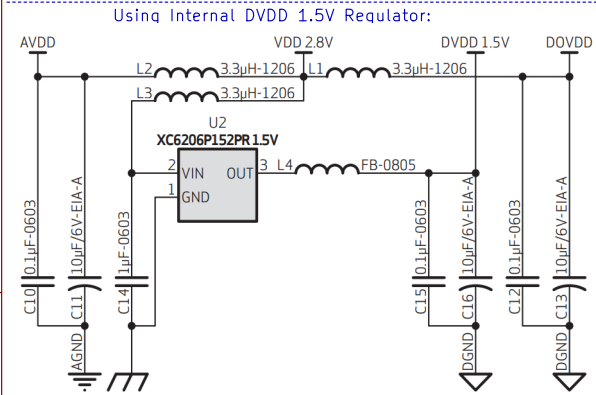
nicole.farber@puri.sm

christian.schilmoeller@puri.sm

Rev: v0.1.0

Id: 12/24

Camera



2.7 POWER UP SEQUENCE

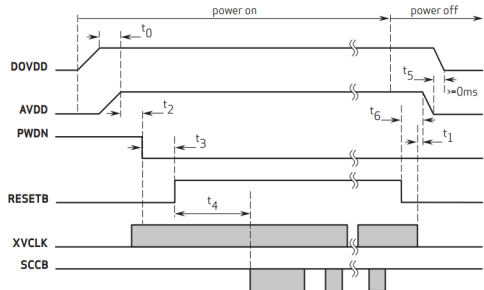
Based on the system power configuration (1.8V or 2.8V for I/O power, using external DVDD or internal DVDD, requiring access to the I2C during power up period or not), the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred. If 2.8V is used for I/O power, due to a high voltage drop at the internal DVDD regulator, there is a potential heat issue. Hence, for a 2.8V power system, OmniVision recommends using an external DVDD source. Due to the higher power down current when using an external DVDD source, OmniVision strongly recommends cutting off all powers, including the external DVDD, when the sensor is not in use in the case of 2.8V I/O and external DVDD.

2.7.1 POWER UP WITH INTERNAL DVDD

For powering up with the internal DVDD and I2C access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. PWDN is active high with an asynchronous design (does not need clock)
3. PWDN pin tied to digital ground if it is not controlled.
4. if PWDN pin is controlled as below, for PWDN to go low, power must first become stable (AVDD to PWDN ≥ 5 ms)
5. RESETB is active low with an asynchronous design
6. master clock XVCLK should provide at least 1 ms before host accesses the sensor's registers
7. host can access I2C bus (if shared) during entire period. 20ms after RESETB goes high, host can access the sensor's registers to initialize sensor

figure 2-3 power up timing with internal DVDD



note $t_0 \geq 0\text{ms}$, delay from DOVDD stable to AVDD stable, it is recommended to power up AVDD shortly after DOVDD has been powered up

$t_1 \geq 0\text{ms}$, delay from XVCLK off to AVDD off

$t_2 \geq 5\text{ms}$, delay from AVDD stable to sensor power up stable, PWDN can be pulled low after this point, XVCLK can be turned on after power on

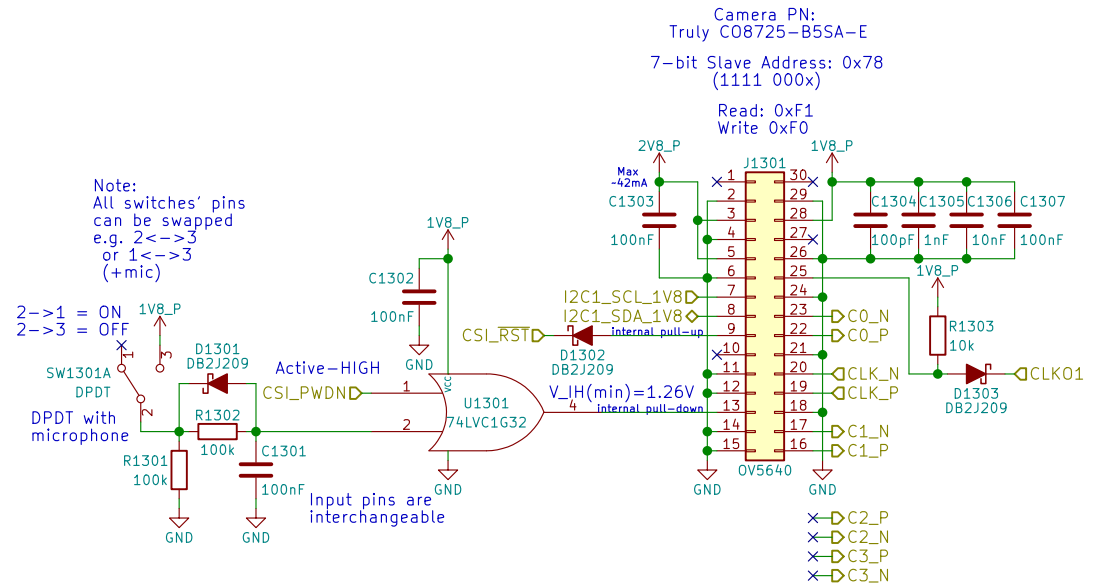
$t_3 \geq 1\text{ms}$, delay from sensor power up stable to RESETB pull up

$t_4 \geq 20\text{ms}$, delay from RESETB pull high to SCCB initialization

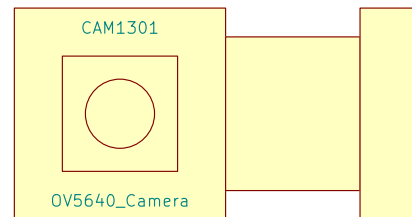
$t_5 \geq 0\text{ms}$, delay from AVDD off to DOVDD off

$t_6 \geq 0\text{ms}$, delay from RESETB pull low to AVDD off

5640 DS 2.2



OV5640 CMOS Image Sensor Datasheet:
https://cdn.sparkfun.com/datasheets/Sensors/LightImaging/OV5640_datasheet.pdf



MIPI CSI



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Sheet: /MIPI/CSI/
File: csi.sch

Size: A4	Date: 2018-06-18
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eric.kuzmenko@puri.sm

angus.ainslie@puri.sm

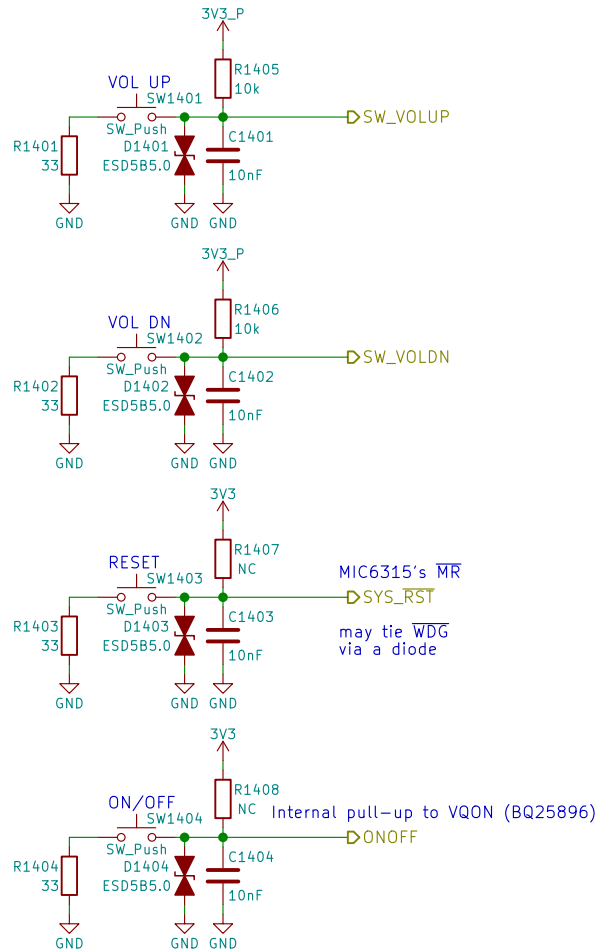
nicole.faerber@puri.sm

christian.schilmoeller@puri.sm

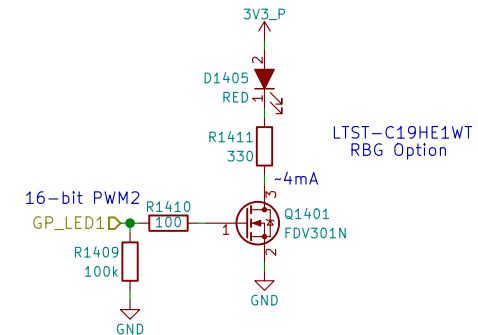
Rev: v0.1.0

Id: 13/24

Buttons & LED



Use PWM2_PWMSAR to set the compare value (duty cycle)
 Use PWM2_PWMCR[15:4] to set the PRESCALER (frequency)
 Use PWM2_PWMPR to set the top of the counter (frequency)



Buttons & LED



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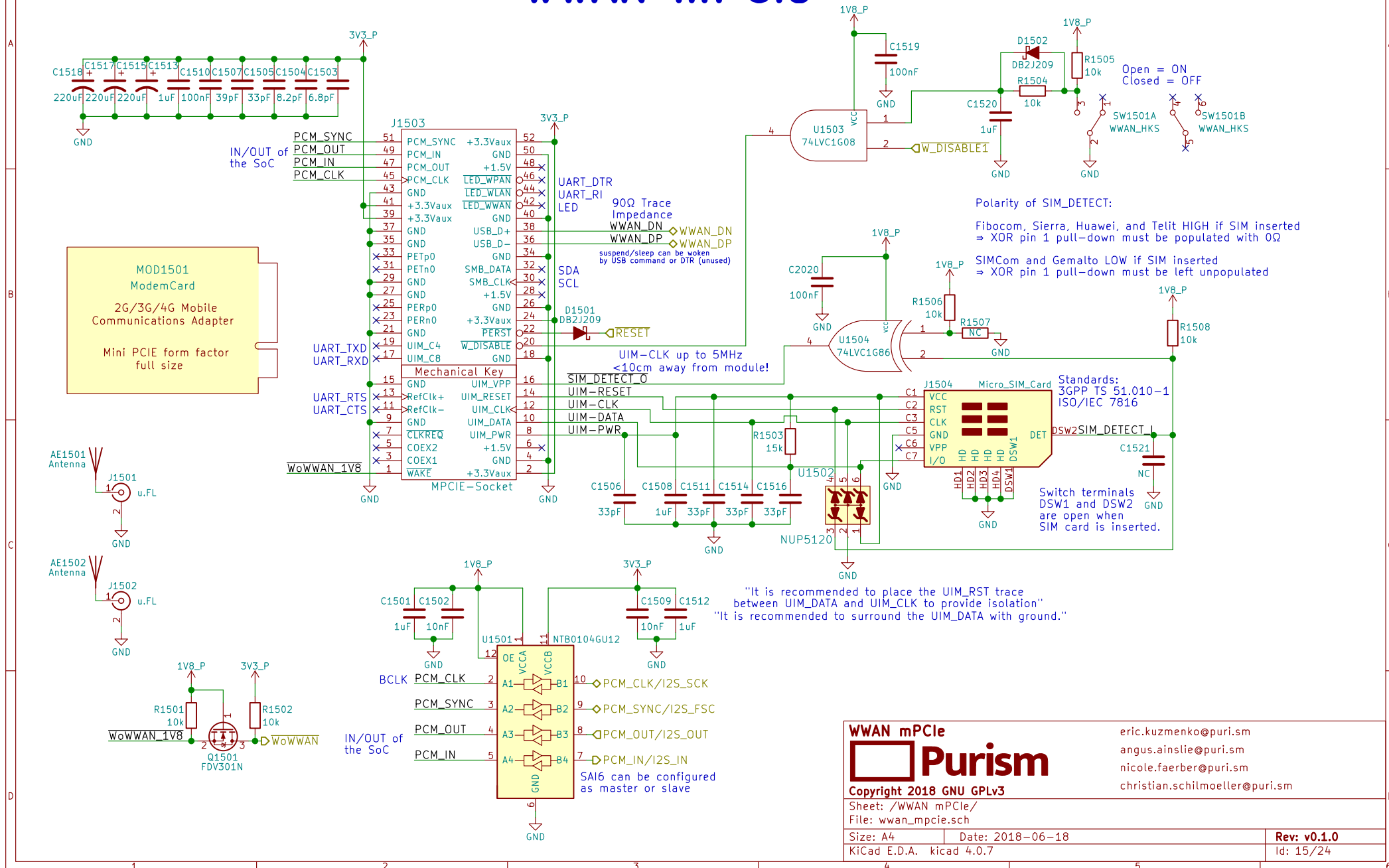
Sheet: /Buttons & LED/
 File: buttons_led.sch

Size: A4 Date: 2018-06-18
 KiCad E.D.A. kicad 4.0.7

eric.kuzmenko@puri.sm
 angus.ainslie@puri.sm
 nicole.ferber@puri.sm
 christian.schilmoeller@puri.sm

Rev: v0.1.0
 Id: 14/24

WWAN mPCIe



Audio

Reference:
http://www.52rd.com/S_txt/2011_3/TXT26685.htm
<http://www.sengpielaudio.com/calculator-transferfactor.htm>
<https://electronics.stackexchange.com/questions/31442/how-can-i-switch-this-audio-jack-using-its-own-mechanical-switches-without-cre>
 (Nt6 does the same)
 +Zener diode to protect against ranges outside of -0.9V to 3.3V

dB specs in datasheet is a unit of power gain (not dBu or VU) with respect to the DAC's unattenuated output

"HP Output - 62.5mW max, 1.02kHz sine into 16Ω load at 3.3 V"
 $\Rightarrow (1V)^2 / (16\Omega) = 62.5mW$
 $\therefore V_{rms} = 1V \Rightarrow V_p(\text{amplitude}) = 1.414V$
 $\therefore I_{rms}(\text{max}) = 62.5mA$

If HP_DET is HIGH for >100ms then HPs are present

S/E button on earbud headsets shorts the mic for key function

Could use FSA8008 to detect mic



$Z(\text{hp}) \geq 16\Omega$

Pin 5 (tip switch) is NC, open when inserted
 If just headphones then HP_DET=HIGH, R(mic)=0
 may add ~220uF cap parallel to Zener

Ext-Mic enabled MIC_SEL=LOW
 Int-Mic enabled MIC_SEL=LOW
 Add TVS next to int-mic? (OpenMoko does this)
 $-37dB = 14.1254mV/Pa$
 $\therefore \text{mic produces } 14.1254mV_{rms} \text{ when exposed to a } 1kHz \text{ tone of } 94dB-SPL \text{ at the capsule (or } 19.98mV \text{ amplitude)}$
 $\Rightarrow 40dB \text{ gain would produce } -2V \text{ amplitude (4Vpp, clipping)}$
 $30dB \text{ gain would produce } -0.632V \text{ amplitude (1.264Vpp)}$
 $38.33dB \text{ gain would yield } 3.3V_{pp}$

LCR Measurements:

Earbud Microphone: @1kHz
 $L_s = 3.844mH$
 $L_p = 15.757H$
 $C_s = 6.583uF$
 $C_p = 1612.8pF$
 $R_s = 1.5465k\Omega$
 $R_p = 1.5478k\Omega$
 $\theta = -0.8deg$

Headset Speaker: @1kHz
 $L_s = 244.4uH$
 $L_p = 141.99mH$
 $C_s = 103.6uF$
 $C_p = 178.77nF$
 $R_s = 36.860\Omega$
 $R_p = 36.860\Omega$
 $\theta = -2.3deg$

Earbud Speaker: @1kHz
 $L_s = 25.2uH$
 $L_p = 311.0mH$
 $C_s = 1.0mF$
 $C_p = 81.95nF$
 $R_s = 17.0300\Omega$
 $R_p = 17.0340\Omega$
 $\theta = 0.5deg$

Audio

Purism

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Sheet: /Audio/
 File: audio.sch

Size: A4 Date: 2018-06-18

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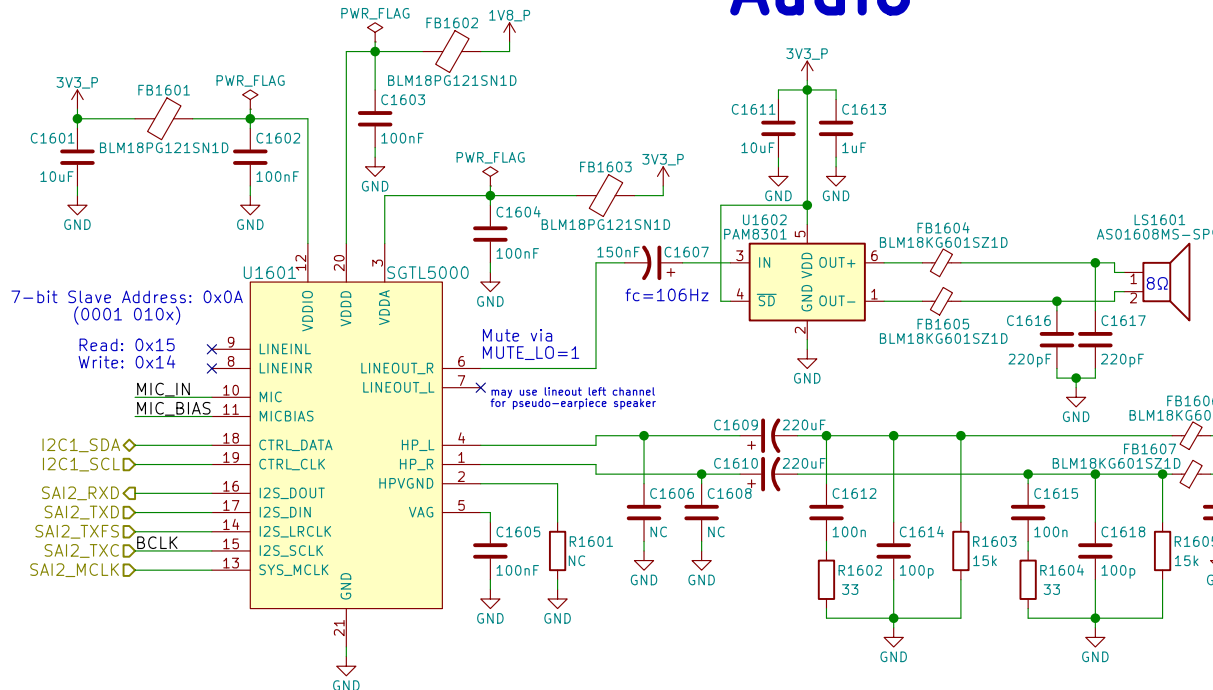
angus.ainslie@puri.sm

nicole.farber@puri.sm

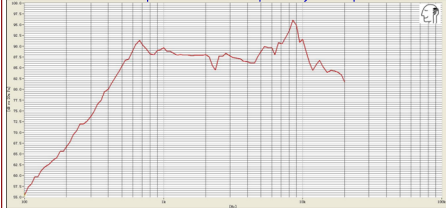
christian.schilmoeller@puri.sm

Rev: v0.1.0

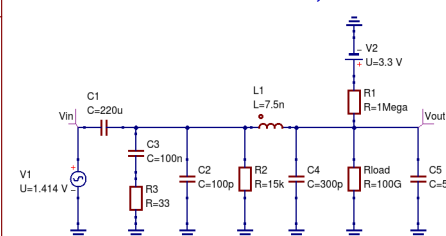
Id: 16/24



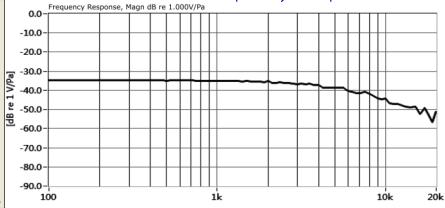
Built-In Speaker's Frequency Response:



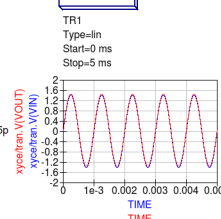
Simulation of HP_DET @ 1kHz output without HP jack inserted:



Built-In Mic's Frequency Response:



transient simulation



RGMII 10/100/1000 Ethernet

Ethernet

Purism

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Sheet: /Ethernet/
File: ethernet.sch

Size: A4 Date: 2018-06-18 Rev: v0.1.0

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Purism

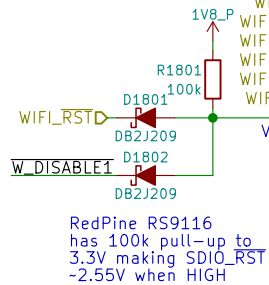
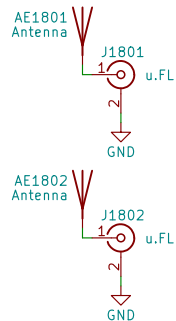
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Rev: v0.1.0
Id: 17/24

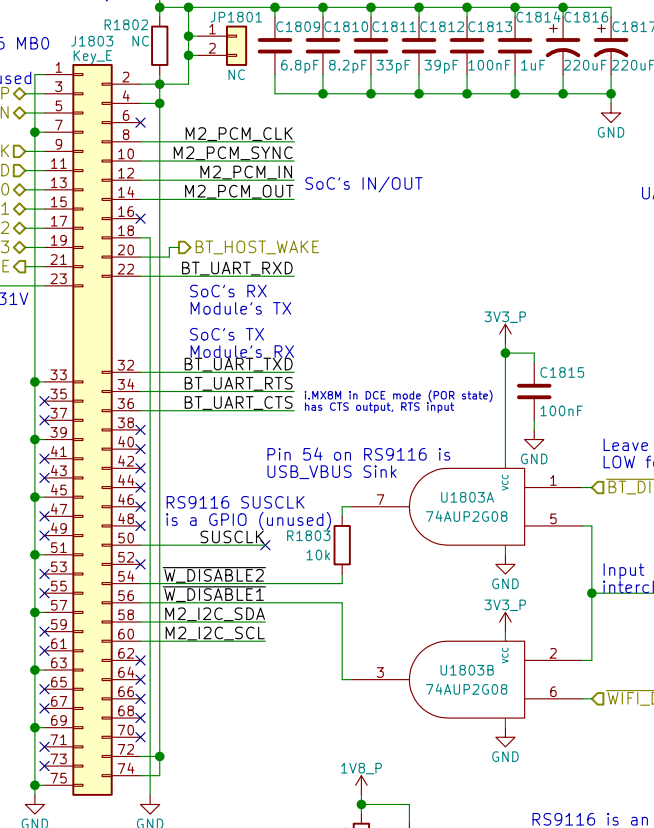
WLAN+BT M.2

RS9116 NC:
RTS, CTS, BT_HOST_WAKE

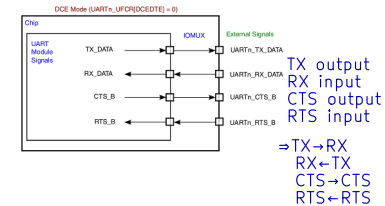
RS9116 datasheet says
no WIFI_WAKE
but the schematic has it



Module: Table 23
Socket: Table 46
3V3_P
M.2 Key E



6.2 M.2 Signal Directions
UARTn_UFCR[DCEDTE]=0 on POR



Leave BT_DISABLE LOW for RS9116

BT_DISABLE

Input pins are interchangeable

WIFI_DISABLE

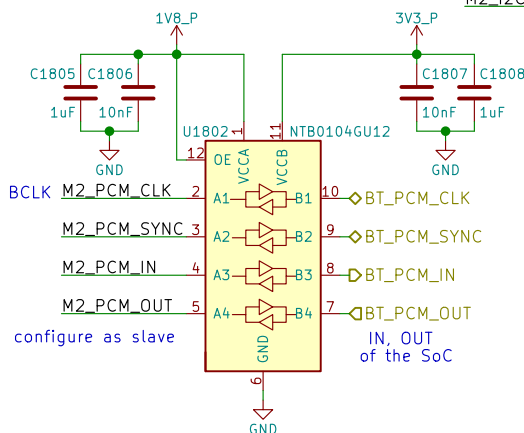
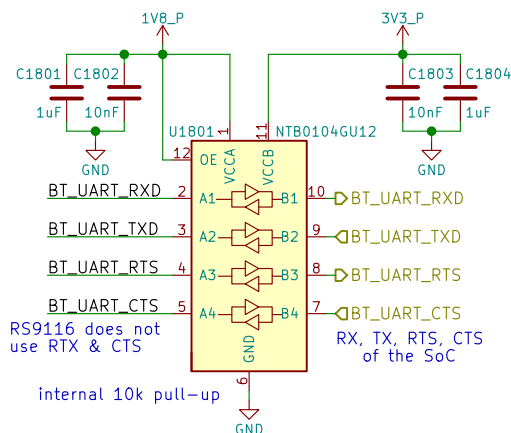
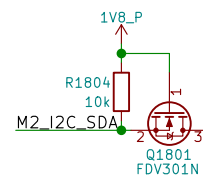
Note:
All switches' pins
can be swapped
e.g. 2<->3
or 1<->3

SW1801A WLAN_HKS

SW1801B WLAN_HKS

Open = ON
Closed = OFF

RS9116 is an I2C master
= its SCL is an output
(ok bc only device on I2C2)



WLAN+BT M.2

Purism

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Sheet: /WLAN+BT M.2/

File: wifi_bt_m2.sch

Size: A4

Date: 2018-06-18

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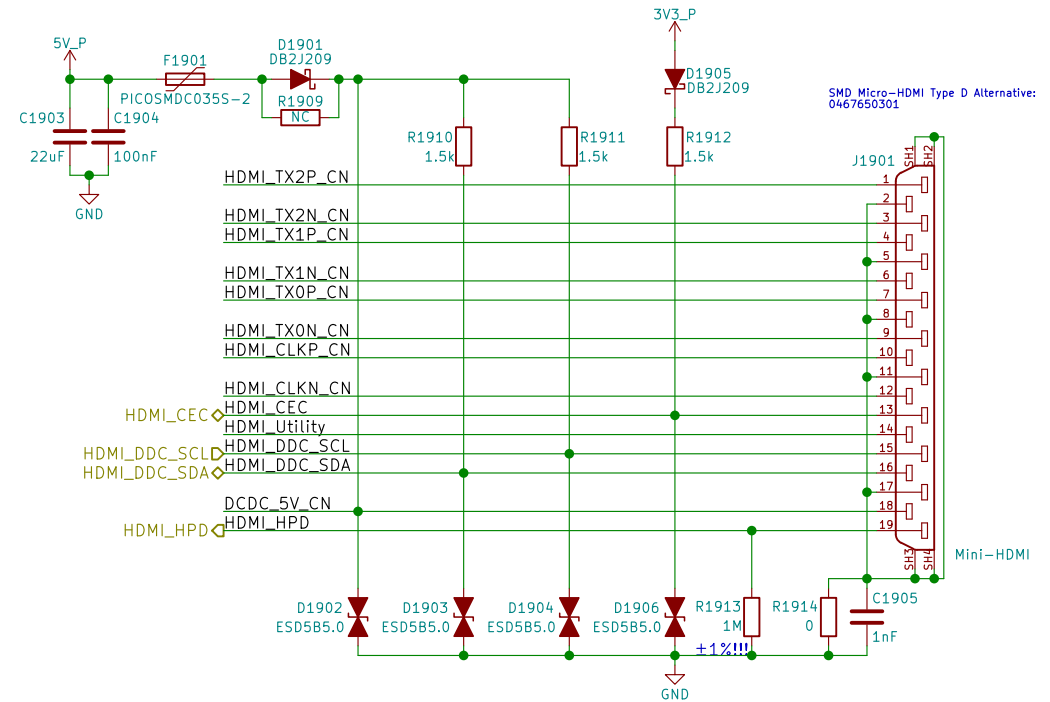
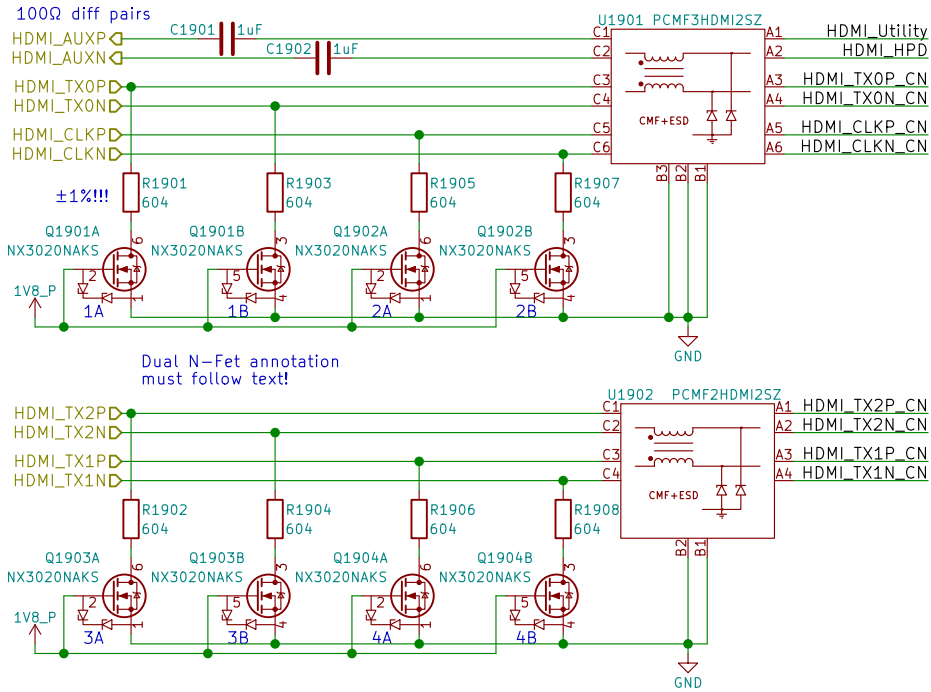
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TUSB1046 can be used for DP over USB-C

HDMI

Layout Note:
May need swap some signals
due to micro-HDMI pinout diff
depending on pin location/routing



HDMI



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Sheet: /HDMI/
File: hdmi.sch

Size: A4
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Date: 2018-06-18

Rev: v0.1.0
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10

B



C

D

10

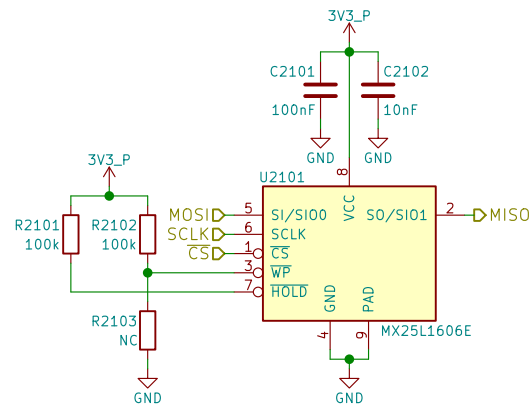


10



Id: 20/24

SPI NOR Flash



SPI NOR Flash



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Sheet: /SPI Flash/

File: flash.sch

Size: A4 Date: 2018-06-18

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Rev: v0.1.0

Id: 21/24

ISO/IEC 7816

Smart Card



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Id: 22/24

GNSS



References:

https://www.u-blox.com/sites/default/files/MAX-M8_HardwareIntegrationManual_L%28UBX-13004876%29.pdf
https://www.u-blox.com/sites/default/files/MAX-8-M8-FW3_HardwareIntegrationManual_L%28UBX-15030059%29.pdf

GNSS



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Sheet: /GNSS/

File: gnss.sch

Size: A4

Date: 2018-06-18

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Rev: v0.1.0

Id: 23/24

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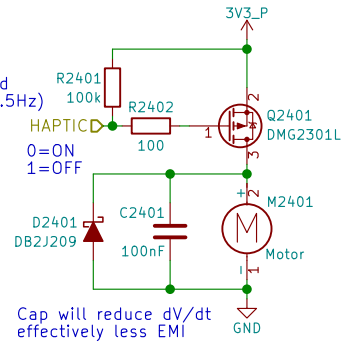
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Haptic Motor

PWM pins occupied:
 GPIO1_I001 - LCD Backlight
 GPIO1_I013 - LED
 GPIO1_I014 - Ethernet (CLKO_25MHz)
 GPIO1_I015 - CSI (CLKO2)

PWM needed?
 Only needs to be toggled
 ON 1 sec, OFF 1 sec (0.5Hz)
 Can MUX as either
 GPIO or PWM2
 swapping with LED



When the motor is off
 both terminals are at GND

Motor will have wire leads
 with a 2-pin Molex or Boom Precision
 connector installed (by request)!
 Metal housing is floating
 (not connected to either pin)
 => could connect housing to GND

Cheaper Motor Connector:
https://lcsc.com/product-detail/1-25T-Connectors_1-25T-1-2AW_C10832.html

Motor Source:
https://www.alibaba.com/product-detail/Coin-motor-vibration-dc-motor-cellphone_1994583657.html?spm=a2700.8443308.0.0.5aa13e5f1wxHgs

Motor Datasheet:
<https://cloud.puri.sm/s/z8JR6DJ4KrJYzoW>

Motor PN:
 BY0820Z021L20

Haptic/Vibration Motor



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Sheet: /Haptic Motor/
 File: haptic.sch

Size: A4 Date: 2018-06-18

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Rev: v0.1.0

Id: 24/24