Battery
I2C1_SDA
I2C1_SCL
CHRG_INT
EN_SRC
EN_SNK
ONOFF
battery.sch
Audio
SAI2_RXD
SAI2_TXD
SAI2_TXFS
SAI2_TXC
SAI2_MCLK
audio.sch
Power
PWR_EN
SD2_RST
POR_B
SWIRE
AVDD_EN
power.sch
Boot Config
BOOT_CFG00 SAI1_RXD0(GPIO4_IO02)
BOOT_CFG01 SAI1_RXD1(GPIO4_IO03)
BOOT_CFG02 SAI1_RXD2(GPIO4_IO04)
BOOT_CFG03 SAI1_RXD3(GPIO4_IO05) CAPTOUCH_RST
BOOT_CFG04 SAI1_RXD4(GPIO4_IO06) SW_BACK
BOOT_CFG05 SAI1_RXD5(GPIO4_IO07) SAI6_TXDO
BOOT_CFG06 SAI1_RXD6(GPIO4_IO08) SAI6_TXFS/RXFS
BOOT_CFG07 SAI1_RXD7(GPIO4_IO09)
BOOT_CFG08 SAI1_TXD0(GPIO4_IO12)
BOOT_CFG09 SAI1_TXD1(GPIO4_IO13) SW_HOME
BOOT_CFG10 SAI1_TXD2(GPIO4_IO14)
BOOT_CFG11 SAI1_TXD3(GPIO4_IO15)
BOOT_CFG12 SAI1_TXD4(GPIO4_IO16) SAI6_TXC/RXC
BOOT_CFG13 SAI1_TXD5(GPIO4_IO17) SAI6_RXDO
BOOT_CFG14 SAI1_TXD6(GPIO4_IO18)
BOOT_CFG15 SAI1_TXD7(GPIO4_IO19)
BOOT_MODE0
BOOT_MODE1
boot.sch
RTC Battery
I2C2_SDA
I2C2_SCL
rtc.sch
UART Debug
UART1_TXD
UART1_RXD
uart.sch
JTAG
JTAG_TMS
JTAG_TCK
JTAG_TDO
JTAG_TDI
POR_B
JTAG_TRST
jtag.sch
uSD Card
CONN_SD2_DATA1
CONN_SD2_DATA0
CONN_SD2_CMD
CONN_SD2_DATA3
CONN_SD2_DATA2
CONN_SD2_CLK
CONN_SD2_CD_B
sd.sch
USB-C
USB1_VBUS
USB1_ID
USB1_SS_SEL
USB1_DP
USB1_DN
USB1_TXP
USB1_TXN
USB1_RXP
USB1_RXN
TCPC_INT
I2C1_SDA
I2C1_SCL
EN_SNK
EN_SRC
usb-c.sch
USB Hub
USB2_DP
USB2_DN
USB2_ID
USB_WWAN_DP
USB_WWAN_DM
USB_WLAN_DP
USB_WLAN_DM
I2C2_SDA
I2C2_SCL
usb_hub.sch
MIPI DSI
D0_P
D0_N
D1_P
D1_N
D2_P
D2_N
D3_P
D3_N
CLK_P
CLK_N
RESX
AVDD_EN
SWIRE
I2C2_SDA
I2C2_SCL
CAPTOUCH_INT
CAPTOUCH_RST
mipi_dsi.sch
Buttons & LED
SW_BACK SAI1_RXD4(GPIO4_IO06) used to be:
SW_VOLDN BTN1 SAI1_TXD3(GPIO4_IO15)
SW_VOLUP BTN2 SAI1_TXD6(GPIO4_IO18)
SW_HOME SAI1_TXD1(GPIO4_IO13)
ONOFF ONOFF
SYS_RST SYS_RST
GP_LED1 GPIO1_IO13 SAI1_RXD1(GPIO4_IO03)
buttons_led.sch
WWAN M.2
CONFIG SAI5_RXC(GPIO3_IO20)
WoWWAN GPIO3_IO08
W_DISABLE1 WWAN_DISABLE GPIO3_IO04
RESET GPIO3_IO09
UART_TX/LED UART3_RXD
UART_RX/DPR UART3_TXD
USB_D+ USB_WWAN_DP
USB_D- USB_WWAN_DM
PCM_CLK/I2S_SCK SAI1_TXD4(GPIO4_IO16) SAI6_TXC/RXC!!!
PCM_SYNC/I2S_FSC SAI1_RXD6(GPIO4_IO08) SAI6_TXFS/RXFS!!!
PCM_IN/I2S_IN SAI1_RXD5(GPIO4_IO07) SAI6_TXDO!!!
PCM_OUT/I2S_OUT SAI1_TXD5(GPIO4_IO17) SAI6_RXDO!!!
wwan_m2.sch

J101A
SD2_RST
SD2_DATA3
SD2_DATA2
SD2_DATA1
SD2_DATA0
SD2_CMD
SD2_CD_B
SD2_CLK
TCPC_INT
USB1_SS_SEL
CAPTOUCH_INT
IMX8M-SOM
GND

J101B
GPIO3_IO09
GPIO3_IO08
PWR_FLAG 3V3_OUT
PWR_FLAG NVCC_SD2
DSI_DP2
DSI_DN2
DSI_DP0
DSI_DN0
DSI_CKN
DSI_CKP
DSI_DP1
DSI_DN1
DSI_DP3
DSI_DN3
+5V
C101 22uF
C102 22uF
C103 0.1uF
C104 0.1uF
C105 22uF
C106 22uF
GND

J101C
BOOT_MODE0
BOOT_MODE1
JTAG_TDI
JTAG_TMS
JTAG_TRST
JTAG_TDO
JTAG_TCK
SAI1_TXC
J102 TEST_1P
DSI_BL_PWM
WDG
PWR_EN
SAI1_RXD1(GPIO4_IO03)
SAI5_RXC(GPIO3_IO20)
SAI1_RXD0(GPIO4_IO02)
GPIO1_IO13
SAI1_RXD4(GPIO4_IO06)
SAI1_RXD3(GPIO4_IO05)
BTN1
SAI2_TXC
SAI1_RXD2(GPIO4_IO04)
SAI2_TXFS
SAI2_RXD
SAI1_RXD6(GPIO4_IO08)
BTN2
SAI2_MCLK
IMX8M-SOM
GND

J101D
3V3_OUT
R102 10k
SAI2_TXD
SAI1_RXD7(GPIO4_IO09)
I2C2_SCL
R103 10k
R104 10k
R101 10k
SAI1_RXD5(GPIO4_IO07)
SAI1_TXD0(GPIO4_IO12)
ONOFF
I2C2_SDA
SAI1_TXD1(GPIO4_IO13)
SYS_RST
I2C1_SCL
I2C1_SDA
SAI1_TXD3(GPIO4_IO15)
SAI1_TXD4(GPIO4_IO16)
SAI1_TXD7(GPIO4_IO19)
UART3_TXD
SAI1_TXD5(GPIO4_IO17)
POR_B
UART1_RXD
SAI1_TXD2(GPIO4_IO14)
SAI1_TXD6(GPIO4_IO18)
UART3_RXD
USB2_DN
USB2_DP
USB1_RXN
USB1_RXP
USB1_TXN
USB1_TXP
UART1_TXD
TODO!!! USB2_VBUS
USB2_VBUS=3.3V??? USB2_ID
USB1_VBUS
USB1_ID
USB1_DN
USB1_DP
IMX8M-SOM
GND

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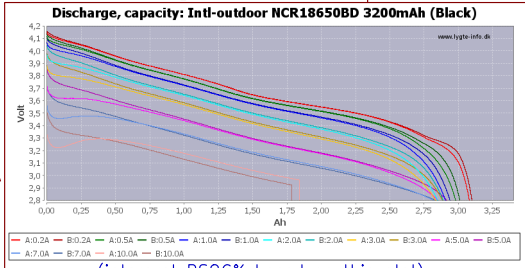
Sheet: /
File: dvk-mx8m-bsb.sch
Title: DVK-MX8M-BSB

Size: A2	Date: 2018-04-19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 1/14



(interpret RSOC% based on this plot)

use AUTO_DPDM_EN
to auto-detect IINLIM

1.658≤ILIM≤2.063
ILIM(nom)≅1.859
3.9≤VIN≤14

U201 BQ25896

I(Lsat)=7A

3.5~4.25V

Default LOW:
adapter source

Open-drain output
tied with TCPC_INT

If enough I/O is available then
separate CHRG_INT & TCPC_INT

This disables charging
but maybe not VBUS->VOUT
if PTN5110HQ's FAULT_STATUS[6]==1
(Force Off VBUS bit) then set EN_HiZ=1
EN_HiZ may be auto-set when in hiccup

Reading PTN5110HQ's CC_STATUS and POWER_STATUS
registers will tell TCPM (i.MX8M) when to set EN_HiZ

Also, reading PTN5110HQ's CC_STATUS and POWER_STATUS
registers will tell TCPM (i.MX8M) when to set OTG_CONFIG=1
(this will also happen when PTN5110HQ sets EN_SRC HIGH)

BC1.2 is not mandated by PD spec
ICO used to determine max current
Also negotiated from CC pins (I2C)

Ihold=3.5A
Itrip=6.3A
Ttrip(max)=5s@8A

VBAT(DPL)=2.15~2.5V

Vrm=5.8V
Vz=6.8

NCR18650BD is recommended

VBAT(nom)=REG06[7:2]
VBAT(default_max_ovp)=(REG06[7:2]×1.005)×1.04=4.3982016V
REG06[7:2]=010111⇒VBAT(max_ovp)=4.3814784
BQ29705 provides 4.425V as OVP!!!

reference design: http://www.ti.com/lit/ug/sluuba2b/sluuba2b.pdf

may want to include BQ29705 protection as in:
http://www.ti.com/lit/ug/tiducl1/tiducl1.pdf
schematic: http://www.ti.com/lit/df/tidrp70/tidrp70.pdf
(PTC may be good enough)

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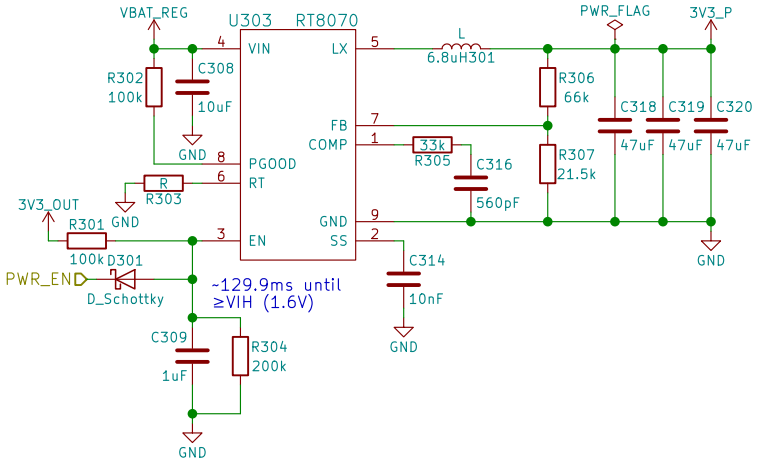
Sheet: /Battery/
File: battery.sch

Title: Battery

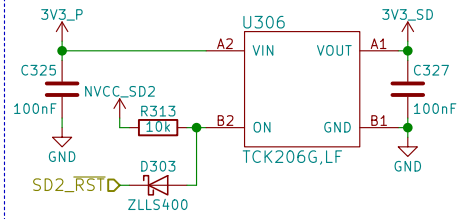
Size: A4	Date: 2018-04-19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 2/14

3.3V/3A

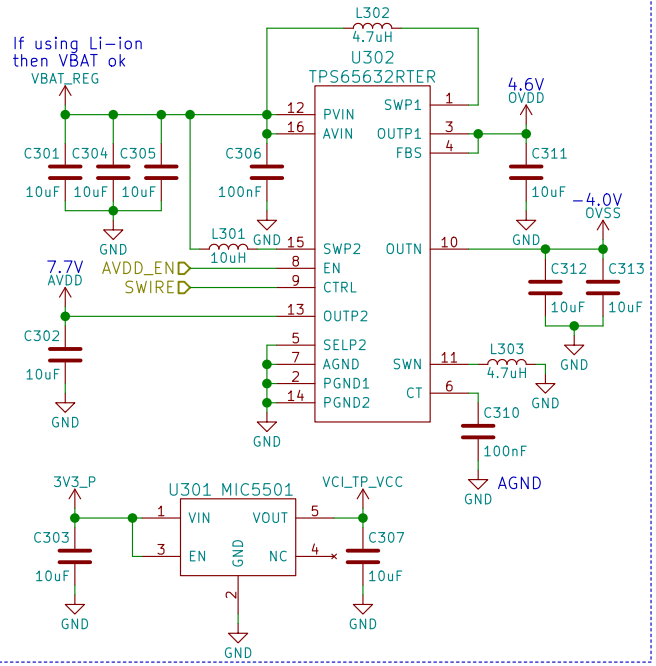
When VBAT can fall below 3.3V use TPS63020 instead!



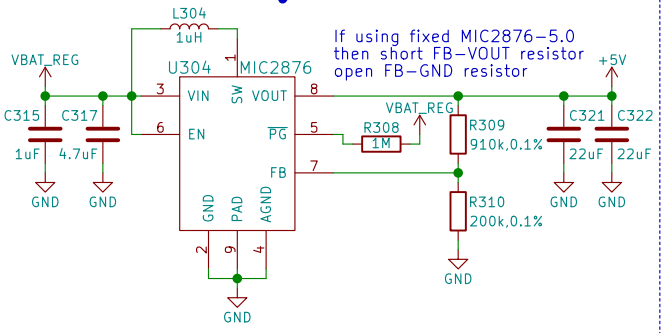
SD POWER



AMOLED POWER

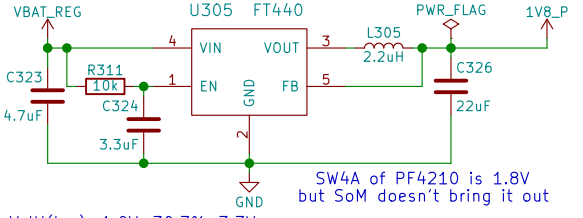


5.0V/3.8A



Cheaper, more efficient, smaller, and simpler than RT6150A
Explicitly mentions USB/smartphone application

1.8V/600mA



SW4A of PF4210 is 1.8V
but SoM doesn't bring it out

$V_{IH}(typ)=1.0V \cong 30.3\% \times 3.3V$
$t(0-30.3\%) \approx 0.361RC$
$\Rightarrow 0.361RC \approx 10ms$
$\therefore R=10k$
$C=2.77uF \cong 3.3uF$

Buck instead of TLV70218 LDO
saving up to ~100mW loss
LM3670MF-1.8 is much more expensive
ST1S12G18R is a drop-in

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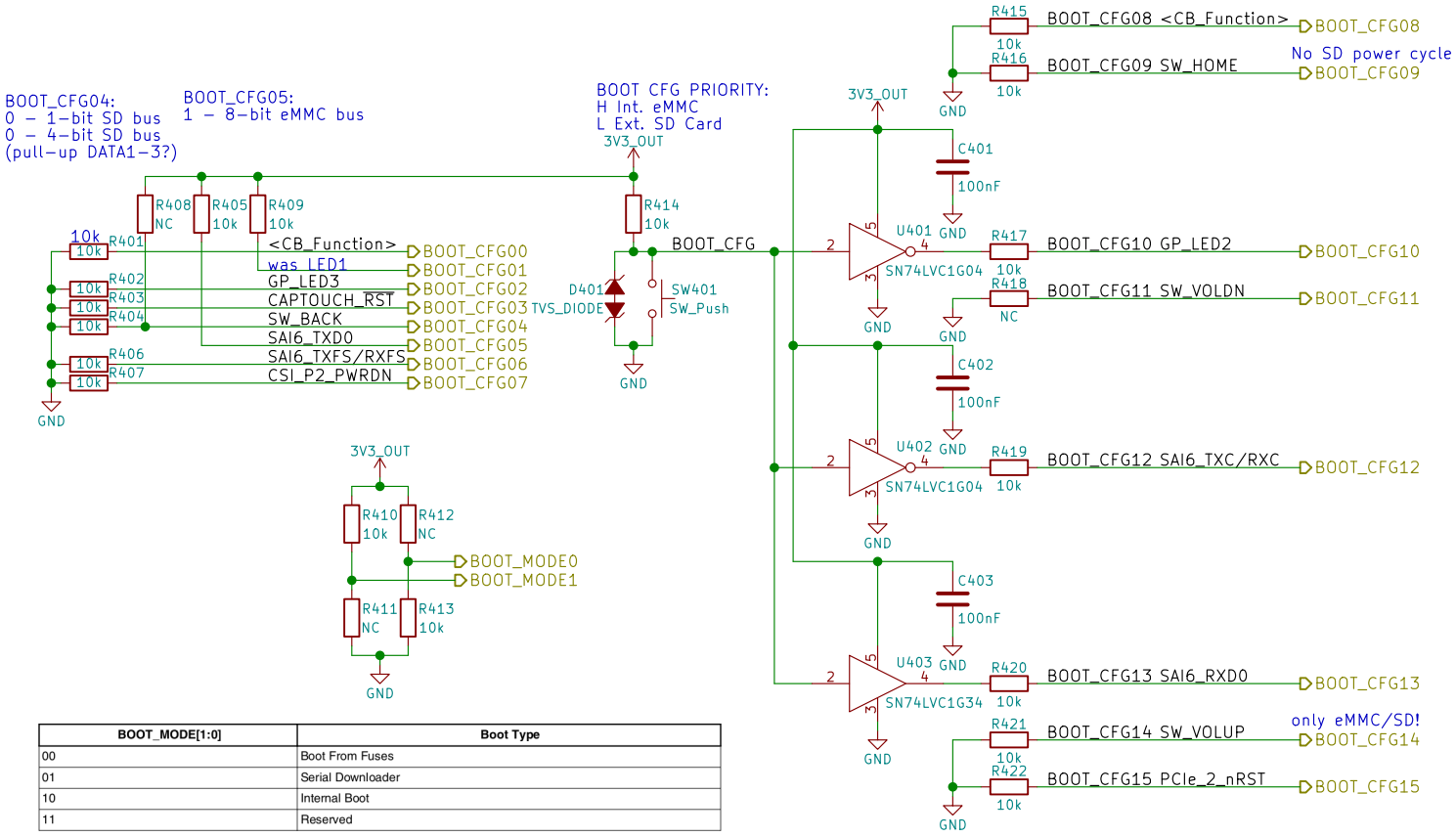
Sheet: /Power/
File: power.sch

Title: Power

Size: A4	Date: 2018-04-19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 3/14

BOOT_CFG[14:12]	Boot device
001	SD/eSD
010	MMC/eMMC
011	NAND

Fuse	Config	Definition	GPIO[1]	Shipped value	Settings
BOOT_CFG[11:10]	OEM	USDHC port selection	Yes	00	00 - USDHC-1 01 - USDHC-2 10 - USDHC-3 else - reserved



BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

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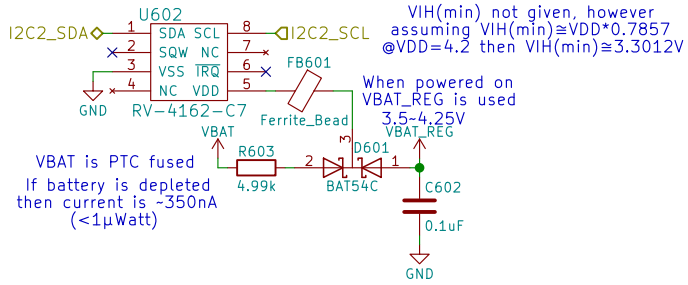
Sheet: /Boot Config/
File: boot.sch

Title: Boot Configuration

Size: A4	Date: 2018–04–19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 4/14



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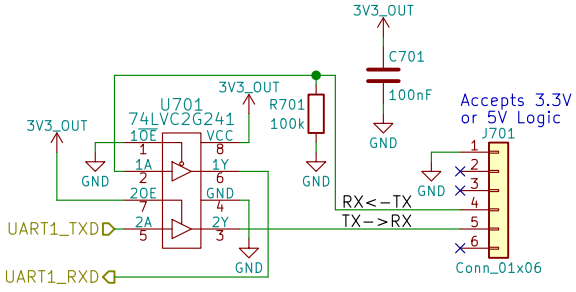
Sheet: /RTC Battery/
File: rtc.sch

Title: RTC Battery

Size: A4	Date: 2018-04-19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 5/14



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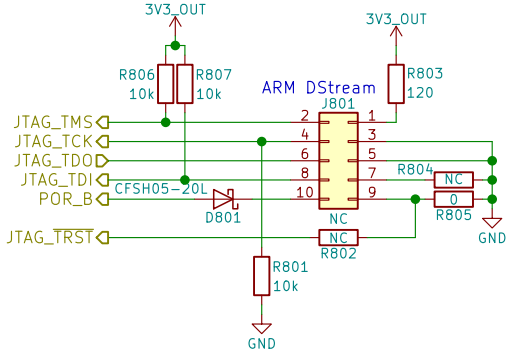
Sheet: /UART Debug/
File: uart.sch

Title: UART Debug

Size: A4	Date: 2018-04-19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 6/14



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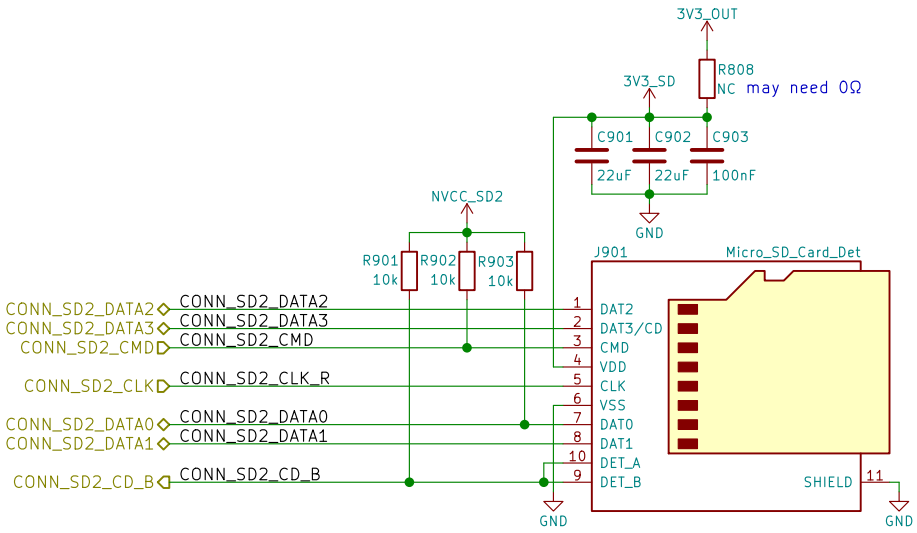
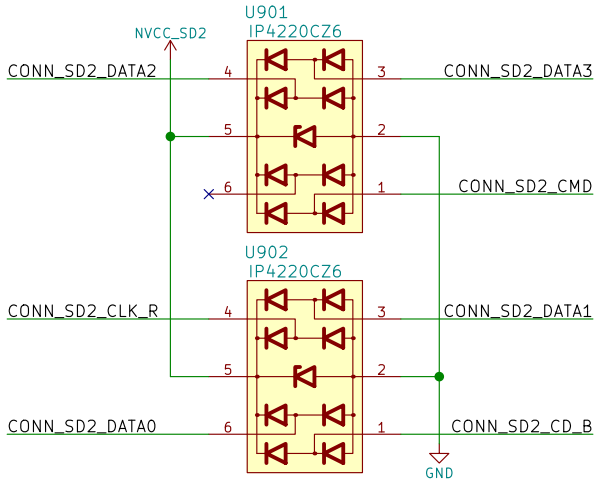
Sheet: /JTAG/
File: jtag.sch

Title: JTAG

Size: A4	Date: 2018-04-19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 7/14





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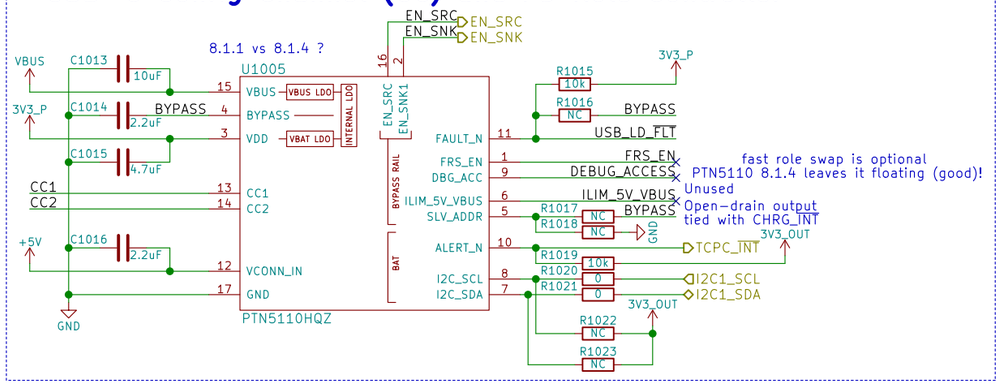
Sheet: /uSD Card/
File: sd.sch

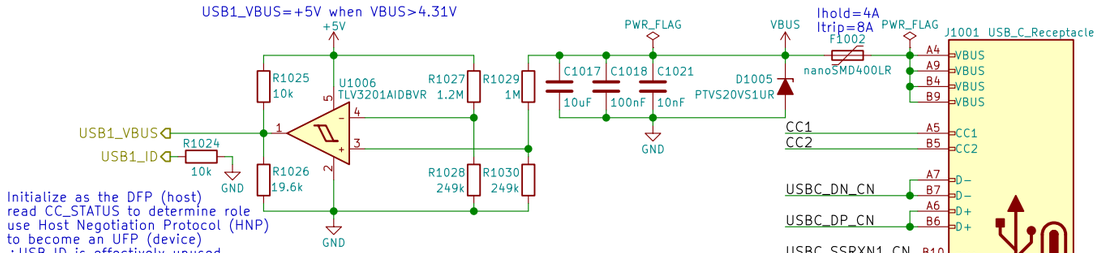
Title: uSD Card

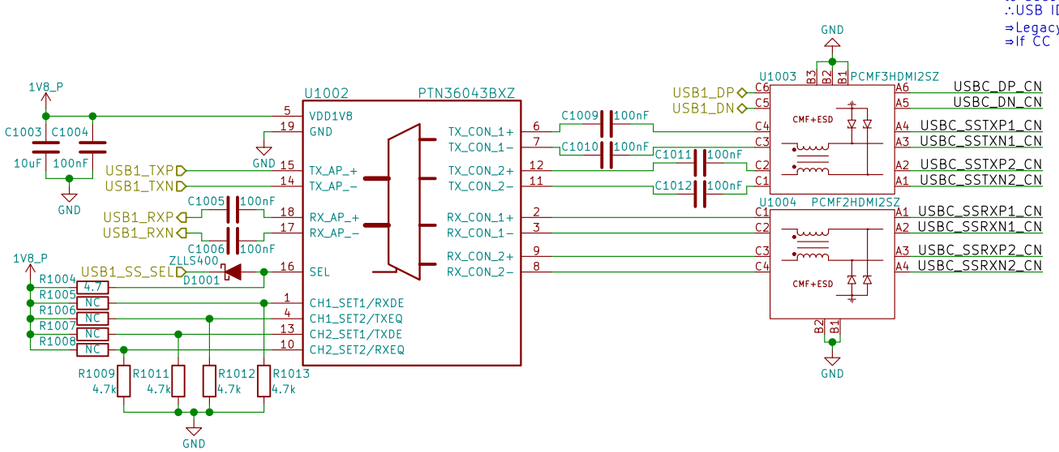
Size: A4	Date: 2018-04-19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 8/14

"Under dead battery operation, PTN5110 applies voltage clamps to both CC pins so that the system may receive power as a Sink. To support platforms with buck-boost configuration, PTN5110 asserts EN_SNK1 pin based on validity of VBUS voltage (facilitates 5 V VBUS sinking)."

USB-C Config Channel (CC) and PD Role Controller







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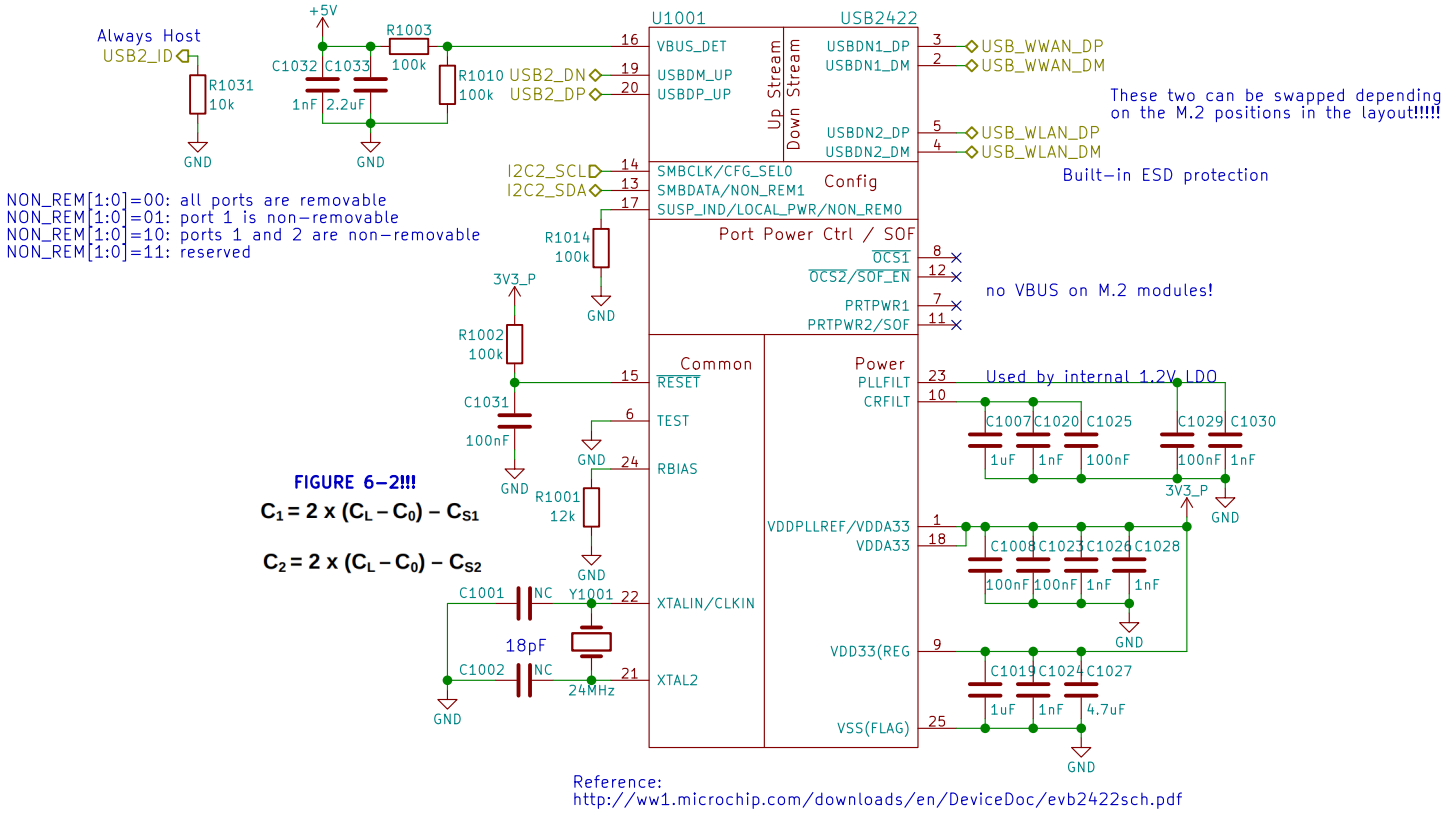
Sheet: /USB-C/		
File: usb-c.sch		
Title: USB Type C		
Size: A3	Date: 2018-04-19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 9/14



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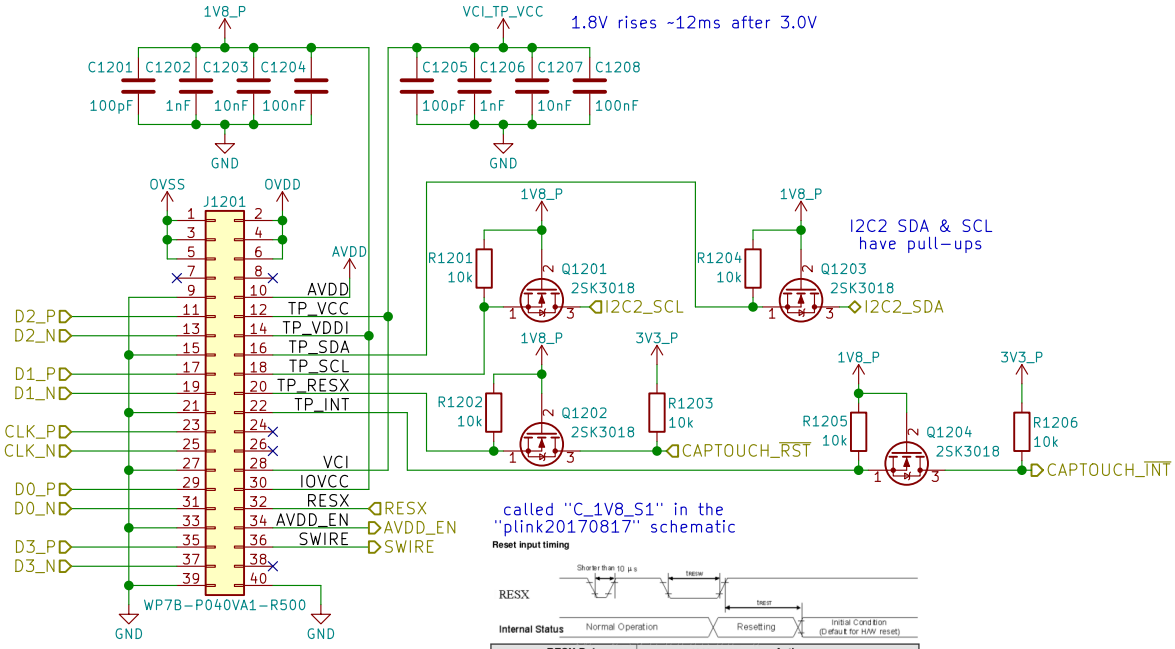
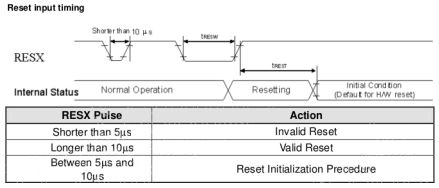
Sheet: /USB Hub/		
File: usb_hub.sch		
Title:		
Size: A4	Date: 2018-04-19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 10/14

Using H546DLB01.1 pin assignment may need
to be changed depending on display used



called "C_1V8_S1" in the
"plink20170817" schematic



RESX Puise	Action
Shorter than 5µs	Invalid Reset
Longer than 10µs	Valid Reset
Between 5µs and 10µs	Reset Initialization Precedure

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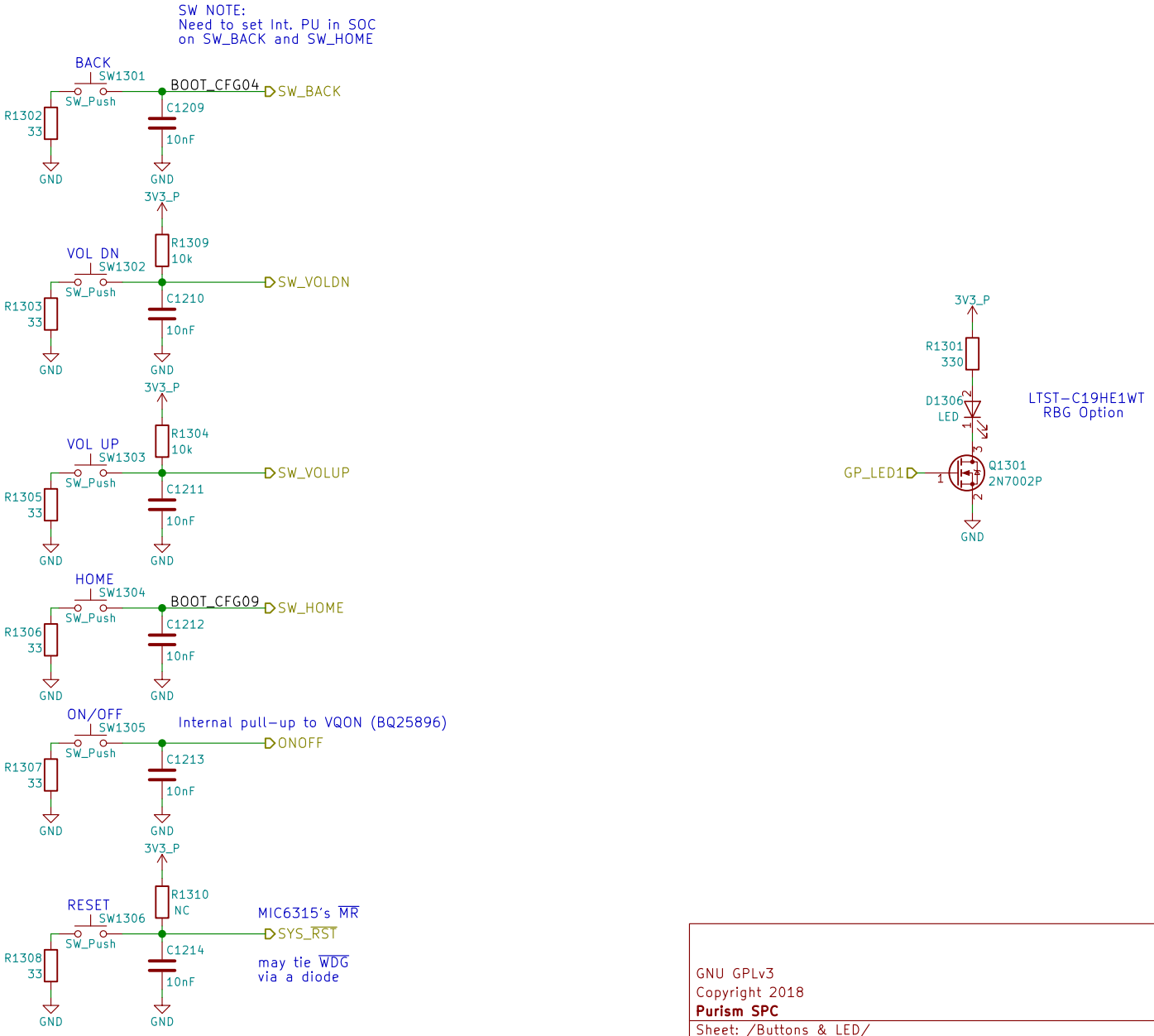
Sheet: /MIPI DSI/
File: mipi_dsi.sch

Title: MIPI DSI

Size: A4	Date: 2018-04-19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 11/14



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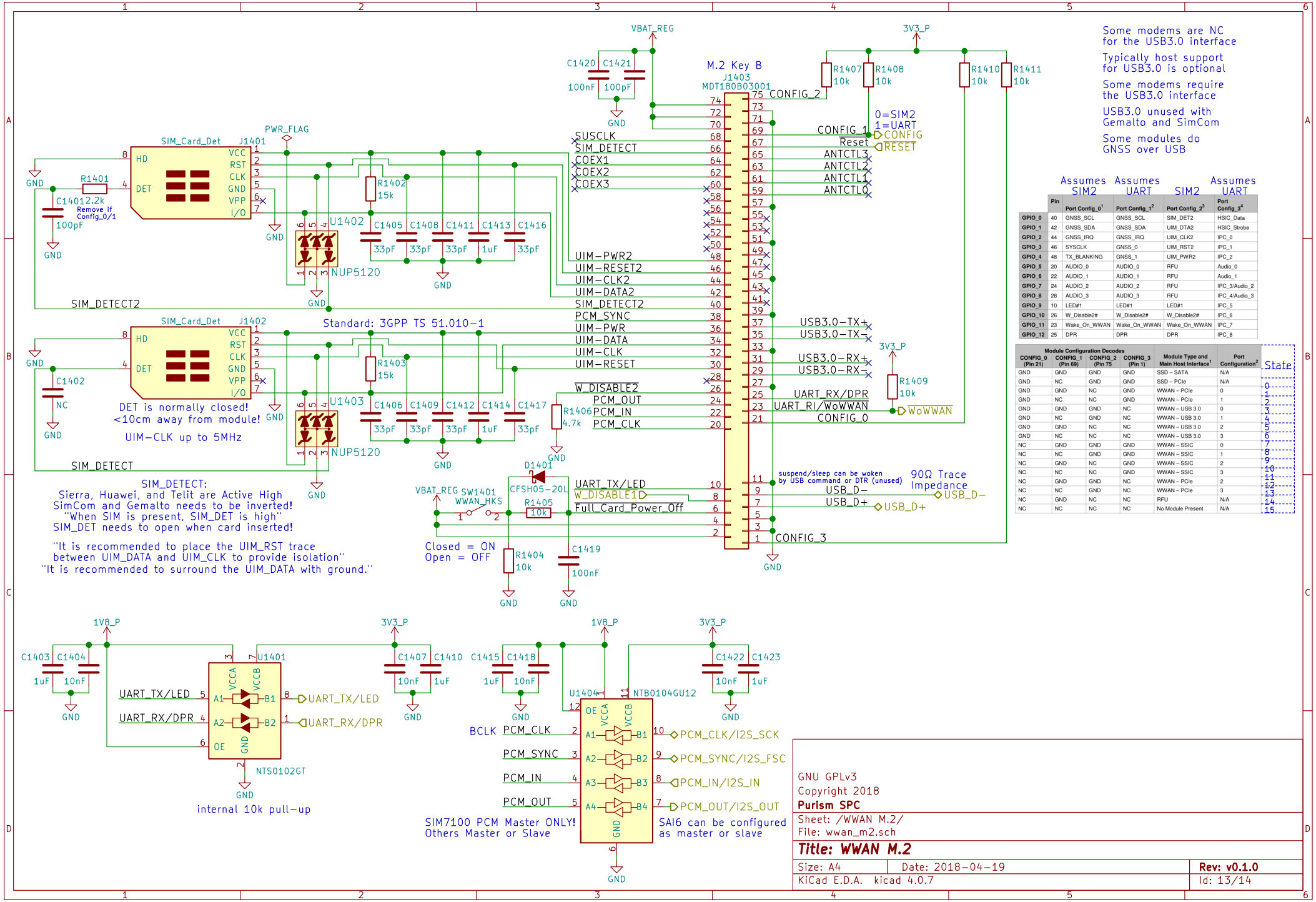
Sheet: /Buttons & LED/
File: buttons_led.sch

Title: Buttons & LED

Size: A4	Date: 2018-04-19	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 12/14



	Pin	Port Config_0[1]	Port Config_1[2]	Port Config_2[3]	Port Config_3[4]
		Assumes SIM2	Assumes UART	SIM2	UART
GPIO_0	40	GNSS_SCL	GNSS_SCL	SIM_DET2	HSIC_Data
GPIO_1	42	GNSS_SDA	GNSS_SDA	UIM_DTA2	HSIC_Strobe
GPIO_2	44	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_0
GPIO_3	46	SYSCLK	GNSS_0	UIM_RST2	IPC_1
GPIO_4	48	TX_BLANKING	GNSS_1	UIM_PWR2	IPC_2
GPIO_5	20	AUDIO_0	AUDIO_0	RFU	Audio_0
GPIO_6	22	AUDIO_1	AUDIO_1	RFU	Audio_1
GPIO_7	24	AUDIO_2	AUDIO_2	RFU	IPC_3/Audio_2
GPIO_8	28	AUDIO_3	AUDIO_3	RFU	IPC_4/Audio_3
GPIO_9	10	LED#1	LED#1	LED#1	IPC_5
GPIO_10	26	W_Disable2#	W_Disable2#	W_Disable2#	IPC_6
GPIO_11	23	Wake_On_WWAN	Wake_On_WWAN	Wake_On_WWAN	IPC_7
GPIO_12	25	DPR	DPR	DPR	IPC_8

Module Configuration Decodes						State
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]	
GND	GND	GND	GND	SSD – SATA	N/A	
GND	NC	GND	GND	SSD – PCIe	N/A	
GND	GND	NC	GND	WWAN – PCIe	0	0
GND	NC	NC	GND	WWAN – PCIe	1	1
GND	GND	GND	NC	WWAN – USB 3.0	0	2
GND	NC	GND	NC	WWAN – USB 3.0	1	3
GND	GND	NC	NC	WWAN – USB 3.0	2	4
GND	NC	NC	NC	WWAN – USB 3.0	3	5
NC	GND	GND	GND	WWAN – SSIC	0	6
NC	NC	GND	GND	WWAN – SSIC	1	7
NC	GND	NC	GND	WWAN – SSIC	2	8
NC	NC	NC	GND	WWAN – SSIC	3	9
NC	GND	GND	NC	WWAN – PCIe	2	10
NC	NC	GND	NC	WWAN – PCIe	3	11
NC	GND	NC	NC	RFU	N/A	12
NC	NC	NC	NC	No Module Present	N/A	13
						14
						15

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Sheet: /WWAN M.2/
File: wwan_m2.sch

Title: WWAN M.2

Size: A4	Date: 2018-04-19	**Rev: v0.1.0**
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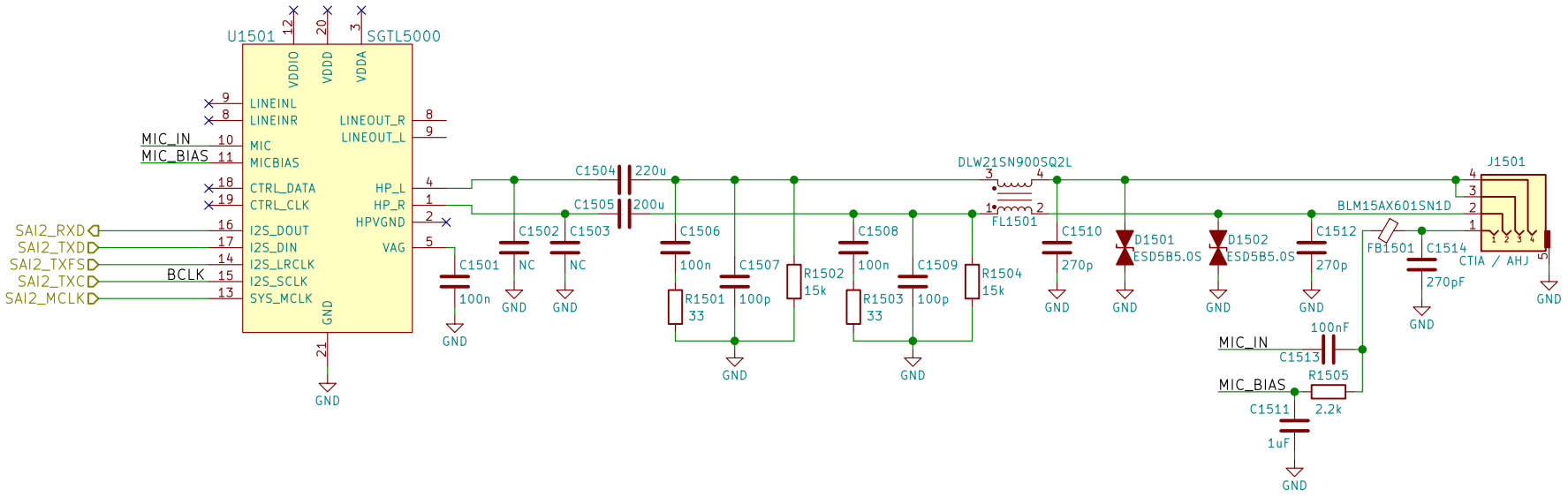

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Sheet: /Audio/
File: audio.sch

Title: Audio

Size: A4	Date: 2018-04-19	**Rev: v0.1.0**
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