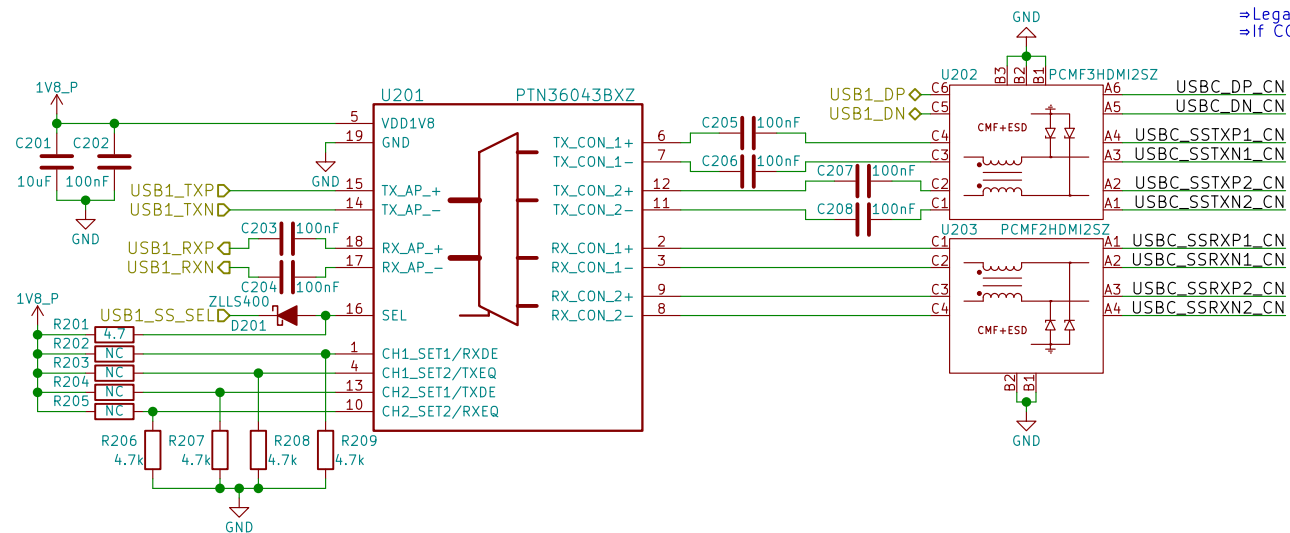
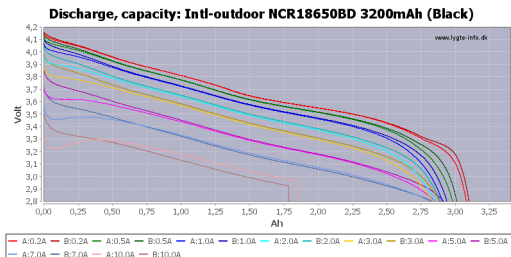


[illegible]

**Title: USB Type C**

Rev: v0.1.0  
Id: 2/17

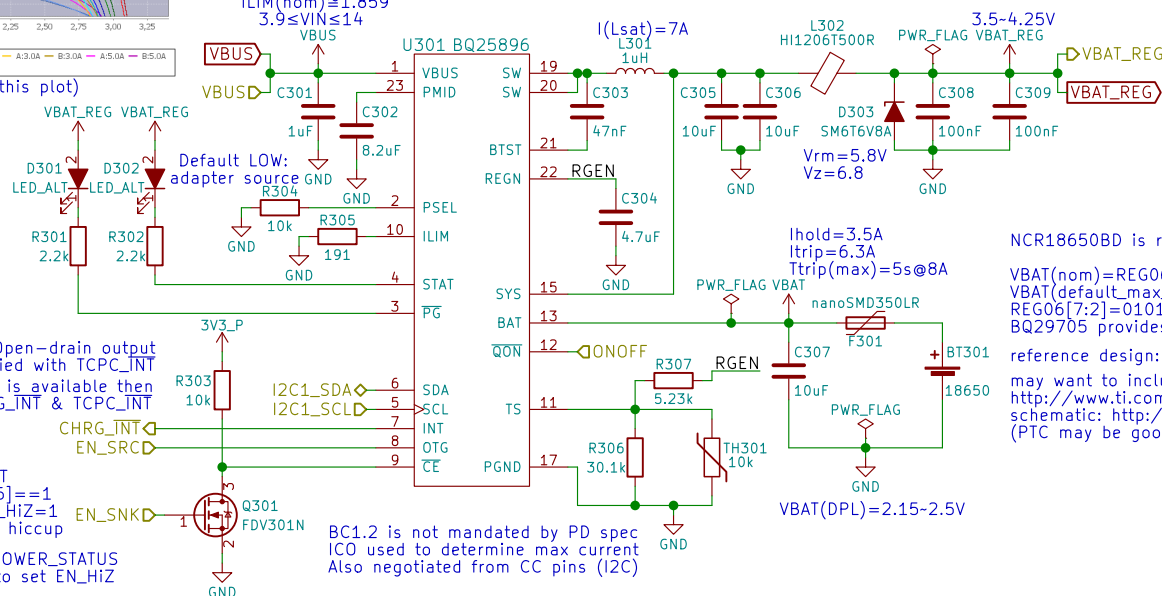


(interpret RSOC% based on this plot)

use AUTO\_DPDM\_EN  
to auto-detect IINLIM

$1.658 \leq I_{LIM} \leq 2.063$   
 $I_{LIM}(nom) \approx 1.859$   
 $3.9 \leq V_{IN} \leq 14$

# Battery Charge Controller



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Purism SPC

Sheet: /Battery/

File: battery.sch

Title: Battery

Size: A4 Date: 2018-05-02

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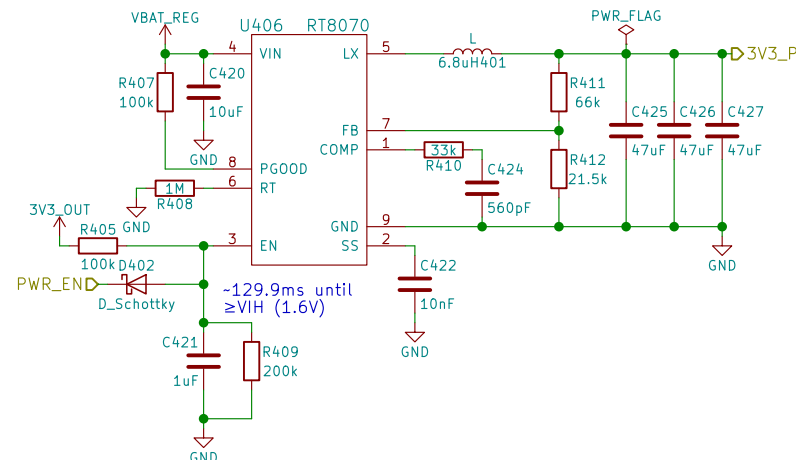
Rev: v0.1.0

Id: 3/17

If using fixed MIC2876-5.0  
then short FB-VOUT resistor  
open FB-GND resistor

Cheaper, more efficient, smaller, and simpler than RT6150A  
Explicitly mentions USB/smartphone application

When VBAT can fall below 3.3V use TPS63020 instead!



The schematic diagram illustrates the power management section of the TMS320C6748. It features two main regulators: the TPS65632RTER (U402) and the MIC5501 (U401).

**TPS65632RTER (U402) Connections:**

- Input:** PVIN (pin 12) is connected to the 7.7V AVDD rail. AVIN (pin 16) is connected to the 4.6V OVDD rail. SWP1 (pin 1) and SWP2 (pin 15) are connected to the 4.7uH inductor L401.
- Output:** OUTP1 (pin 3) is connected to the 4.6V OVDD rail. OUTP2 (pin 13) is connected to the 7.7V AVDD rail. OUTN (pin 10) is connected to the -4.0V OVSS rail.
- Control:** EN (pin 8) is connected to the 7.7V AVDD rail. CTRL (pin 9) is connected to the SWIRED signal. SELP2 (pin 5) is connected to the 7.7V AVDD rail. AGND (pin 7), PGND1 (pin 2), and PGND2 (pin 14) are connected to GND.
- Other:** FBS (pin 4) is connected to the 4.6V OVDD rail. CT (pin 6) is connected to GND via a 100nF capacitor C410.

**MIC5501 (U401) Connections:**

- Input:** VIN (pin 1) is connected to the 3V3\_P rail.
- Output:** VOUT (pin 5) is connected to the VCL\_TP\_VCC rail.
- Control:** EN (pin 3) is connected to the 3V3\_P rail.
- Other:** NC (pin 4) is connected to GND. GND (pin 2) is connected to GND.

**Capacitors:**

- C401, C404, C405: 10uF capacitors connected to the 7.7V AVDD rail.
- C402: 10uF capacitor connected to the 7.7V AVDD rail.
- C403: 10uF capacitor connected to the 3V3\_P rail.
- C407: 100nF capacitor connected to the 7.7V AVDD rail.
- C409: 10uF capacitor connected to the VCL\_TP\_VCC rail.
- C411, C412, C413: 10uF capacitors connected to the 4.6V OVDD rail.
- C410: 100nF capacitor connected to GND.

**Inductors:**

- L401: 4.7uH inductor connected to the 7.7V AVDD rail.
- L404: 4.7uH inductor connected to the 4.6V OVDD rail.

VBAT\_REG

U405 FT440

VIN VOUT

EN FB

GND

GND

PWR\_FLAG

1V8\_P

C418

R406 10k

C419

3.3uF

4.7uF

L405 2.2uH

C423 22uF

SW4A of PF4210 is 1.8V but SoM doesn't bring it out

$V_{IH}(typ) = 1.0V \approx 30.3\% \times 3.3V$   
 $t(0 - 30.3\%) \approx 0.361RC$   
 $\approx 0.361RC \approx 10ms$   
 $\therefore R = 10k$   
 $C = 2.77\mu F \approx 3.3\mu F$

Buck instead of TLV70218 LDO saving up to ~100mW loss

LM3670MF-1.8 is much more expensive

ST1512G18R is a drop-in

### Purism SPC

Sheet: /Power/  
File: power.sch

**Title: Power**

**Title: Power**

**Title: Power**

Size: A4

Date: 2018-05-02

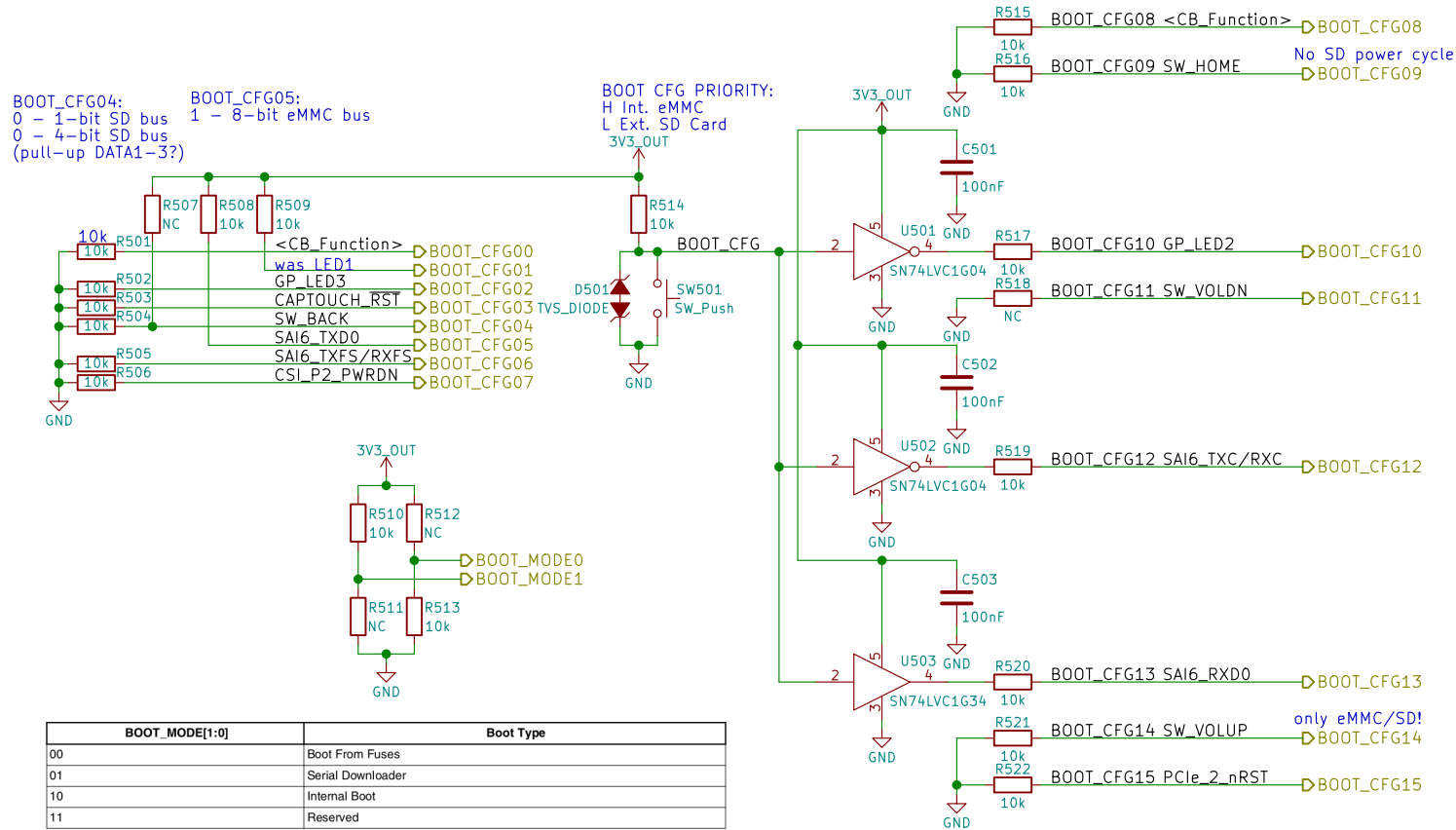
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Rev: v0.1.0

Id: 4/17

BOOT\_CFG04:  
0 - 1-bit SD bus  
0 - 4-bit SD bus  
(pull-up DATA1-3?)

BOOT\_CFG05:  
1 - 8-bit eMMC bus



BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

BOOT_CFG[14:12]		Boot device			
001		SD/eSD			
010		MMC/eMMC			
011		NAND			
Fuse	Config	Definition	GPIO <sup>1</sup>	Shipped value	Settings
BOOT_CFG[11:10]	OEM	USDHC port selection	Yes	00	00 - USDHC-1 01 - USDHC-2 10 - USDHC-3 else - reserved

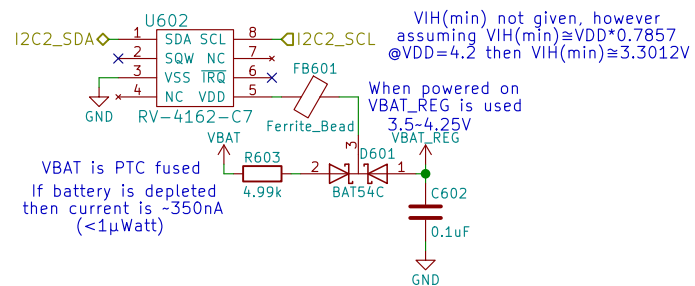
GNU GPLv3  
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**Purism SPC**

Sheet: /Boot Config/  
File: boot.sch

**Title: Boot Configuration**

Size: A4      Date: 2018-05-02  
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**Rev: v0.1.0**  
Id: 5/17



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**Purism SPC**

Sheet: /RTC/  
File: rtc.sch

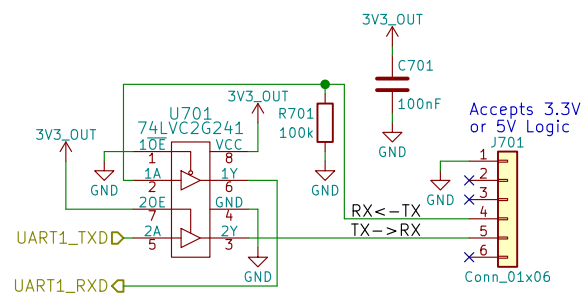
**Title: RTC**

Size: A4 Date: 2018-05-02

KiCad E.D.A. kicad 4.0.7

**Rev: v0.1.0**

Id: 6/17



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**Purism SPC**

Sheet: /UART Debug/  
File: uart.sch

**Title: UART Debug**

Size: A4 Date: 2018-05-02

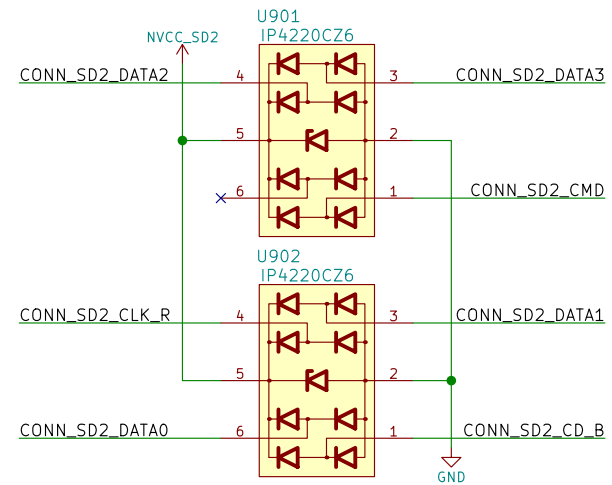
KiCad E.D.A. kicad 4.0.7

**Rev: v0.1.0**

Id: 7/17

Id: 8/17





GNU GPLv3

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**Purism SPC**

Sheet: /uSD Card/

File: sd.sch

**Title: uSD Card**

Size: A4 Date: 2018-05-02

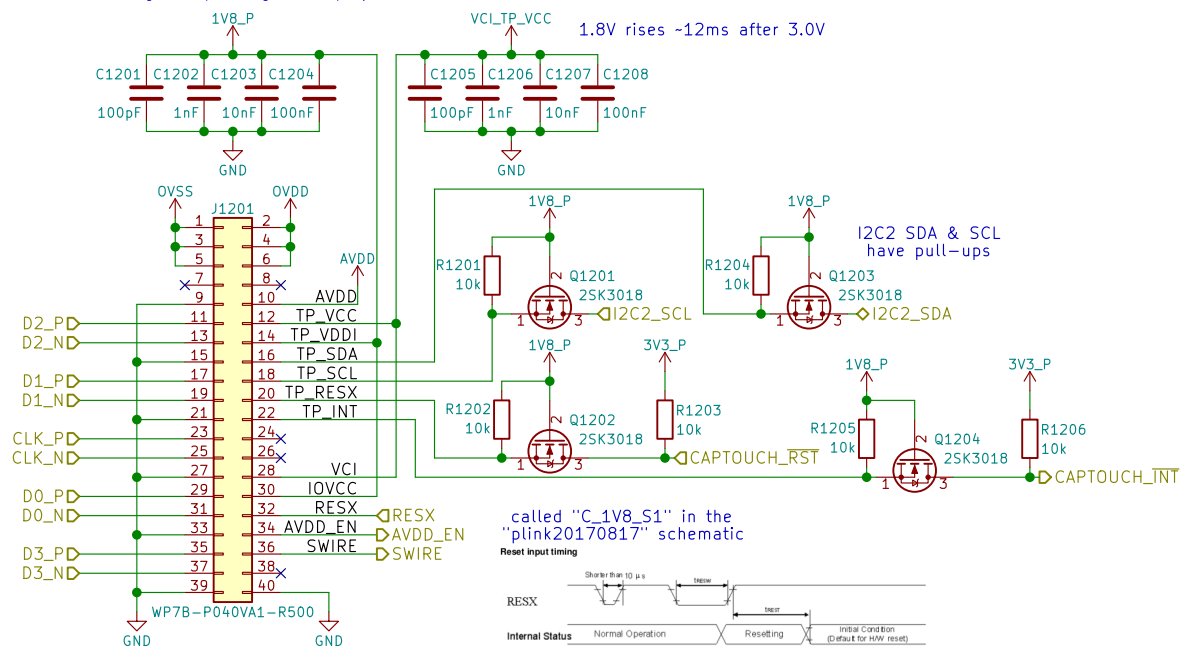
KiCad E.D.A. kicad 4.0.7

**Rev: v0.1.0**

Id: 9/17

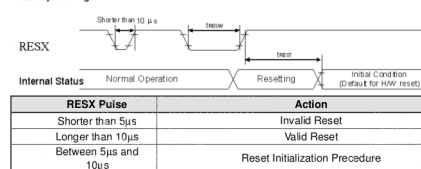


Using H546DLB01.1 pin assignment may need to be changed depending on display used



called "C\_1V8\_S1" in the "plink20170817" schematic

Reset input timing



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**Purism SPC**

Sheet: /MIPI DSI/  
File: mipi\_dsi.sch

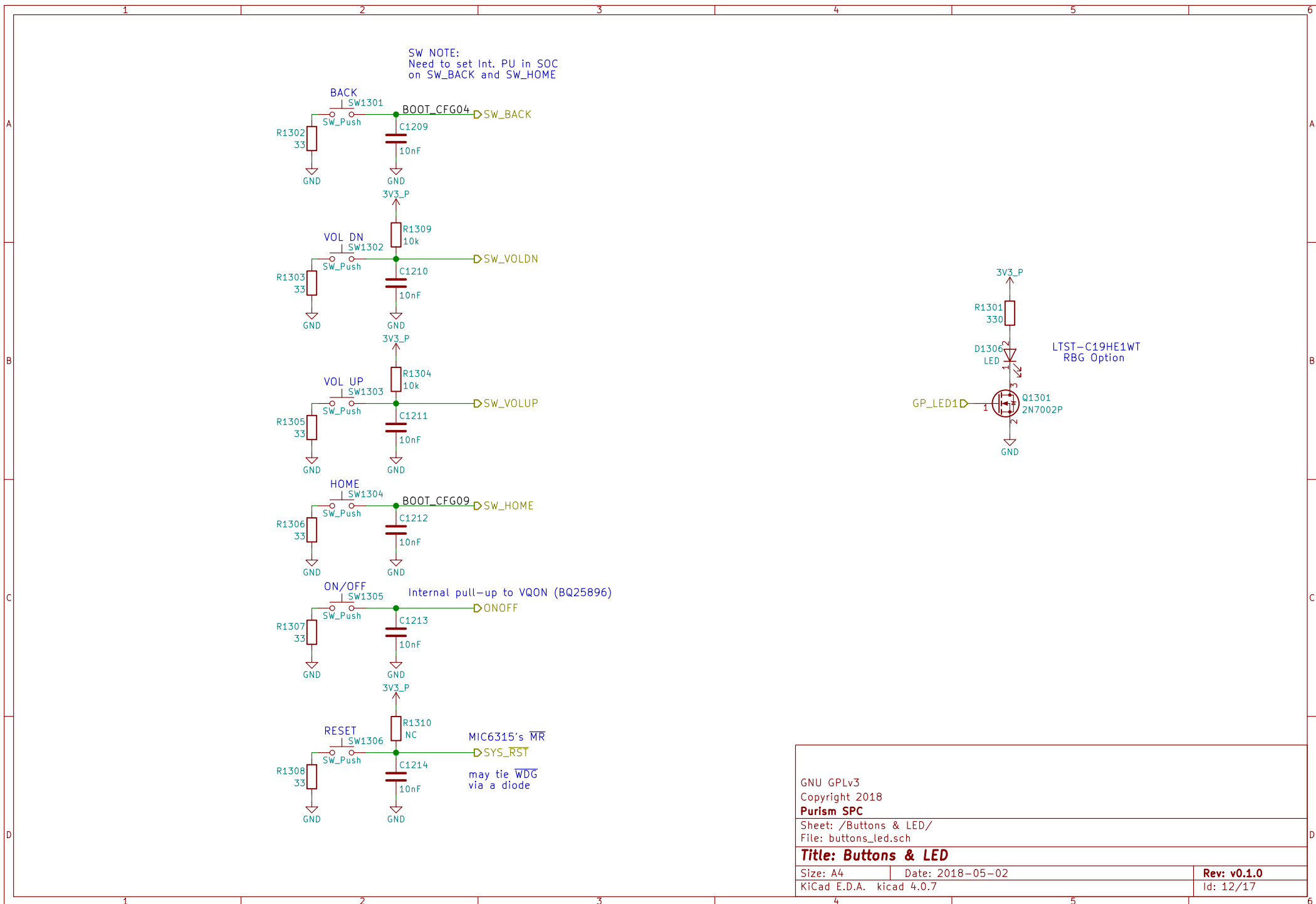
**Title: MIPI DSI**

Size: A4 Date: 2018-05-02

KiCad E.D.A. kicad 4.0.7

**Rev: v0.1.0**

Id: 11/17



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**Purism SPC**

Sheet: /Buttons & LED/  
File: buttons\_led.sch

**Title: Buttons & LED**

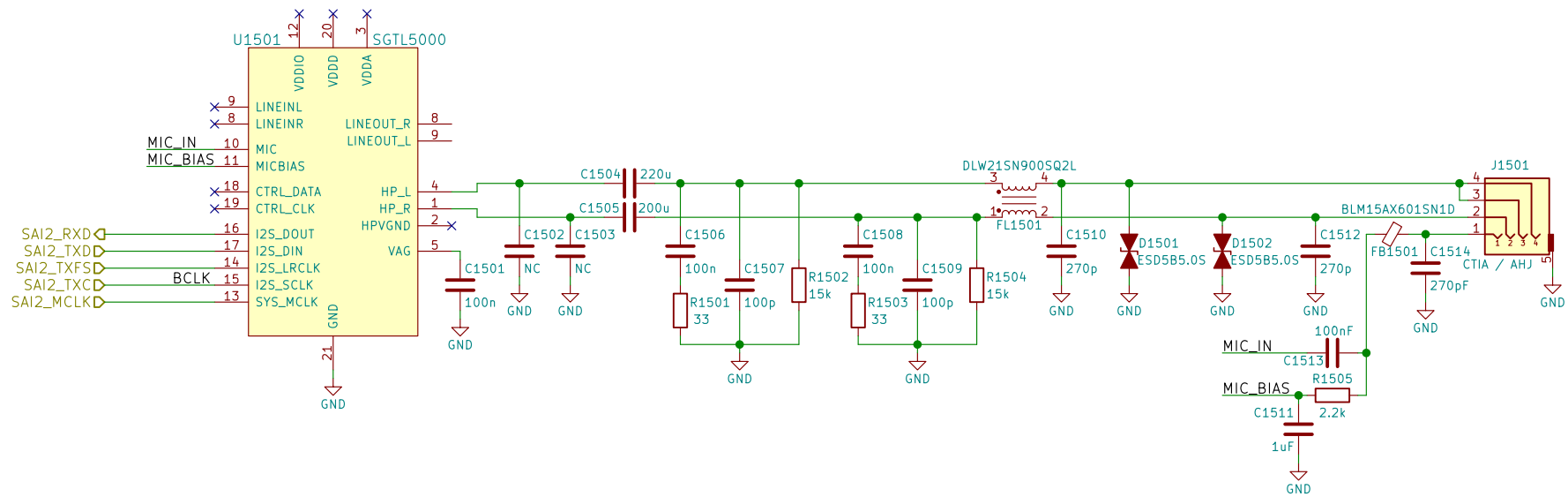
Size: A4 Date: 2018-05-02

KiCad E.D.A. kicad 4.0.7

**Rev: v0.1.0**

Id: 12/17





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**Purism SPC**

Sheet: /Audio/  
File: audio.sch

**Title: Audio**

Size: A4 Date: 2018-05-02

KiCad E.D.A. kicad 4.0.7

**Rev: v0.1.0**

Id: 14/17

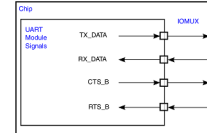
RS9116 NC:  
RTS, CTS, BT\_HOST\_WAKE, WIFI\_WAKE

## 6.2 M.2 Signal Directions

Module: Table 23  
Socket: Table 46

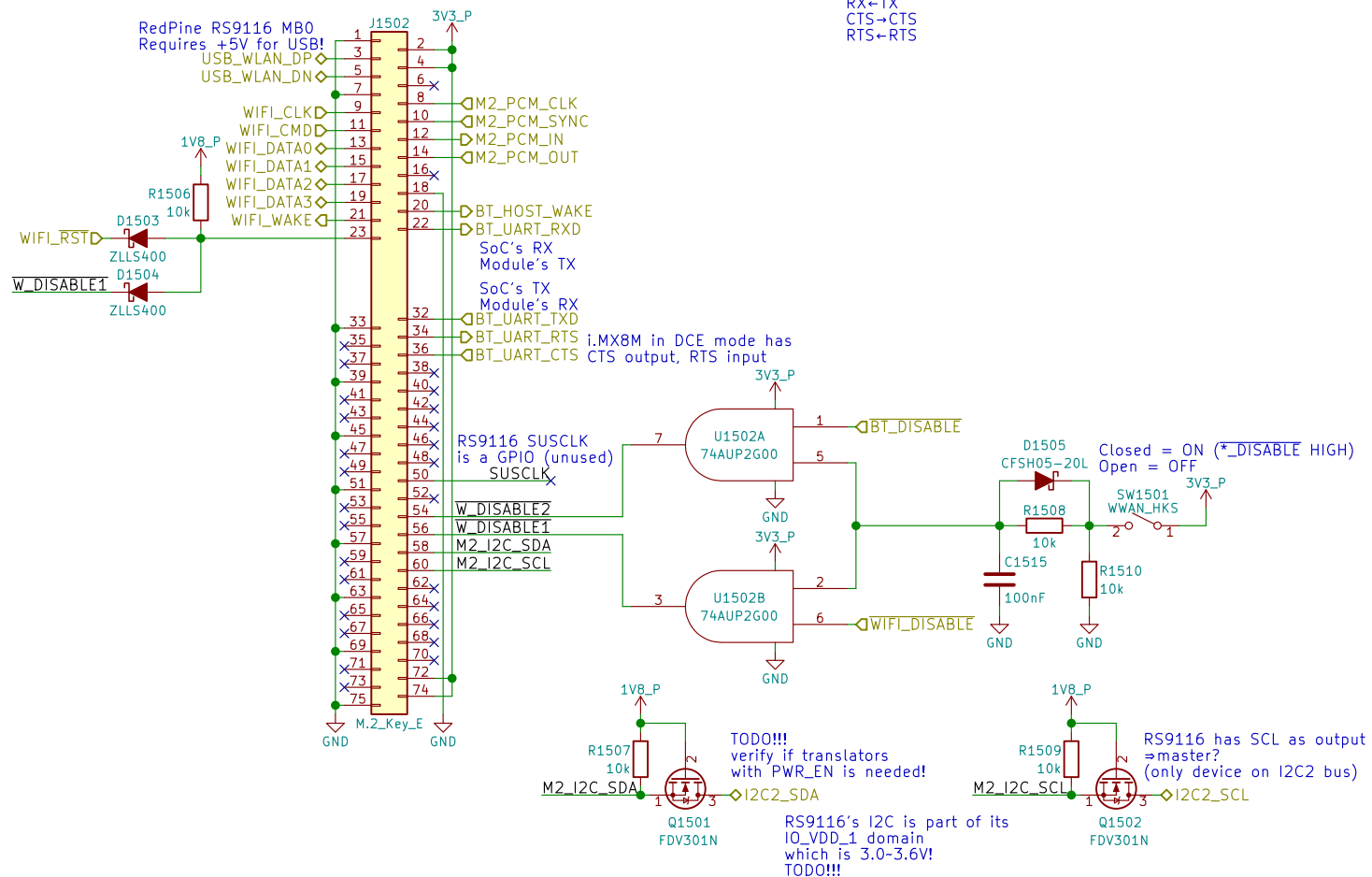
UARTn\_UFCR[DCEDTE]=0 on POR

DCE Mode (UARTn\_UFCR[DCEDTE]=0)



TX output  
RX input  
CTS output  
RTS input

⇒ TX→RX  
RX←TX  
CTS→CTS  
RTS→RTS



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**Purism SPC**

Sheet: /WLAN+BT M.2/

File: wifi\_bt\_m2.sch

**Title: WLAN+BT M.2**

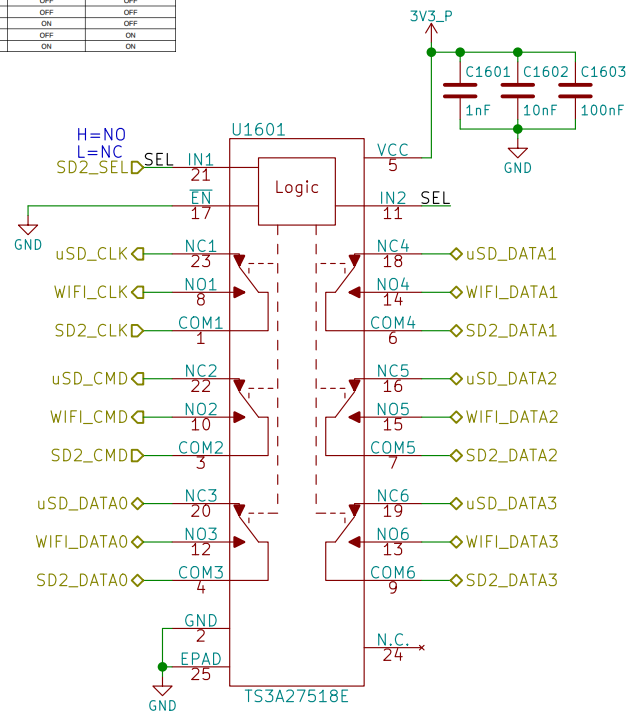
Size: A4 Date: 2018-05-02

KiCad E.D.A. kicad 4.0.7

**Rev: v0.1.0**

Id: 15/17

EN	IN1	IN2	NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	ON	OFF
L	H	L	OFF	ON	OFF	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON



Id: 16/17



# RGMII 10/100/1000 Ethernet

Sheet: /Ethernet/  
File: ethernet.sch

**Title:**

Size: A4	Date:	Rev:
KiCad E.D.A. kicad 4.0.7		Id: 17/17

<b>Title:</b>		
Size: A4	Date:	<b>Rev:</b>
KiCad E.D.A.    kicad 4.0.7		Id: 17/17