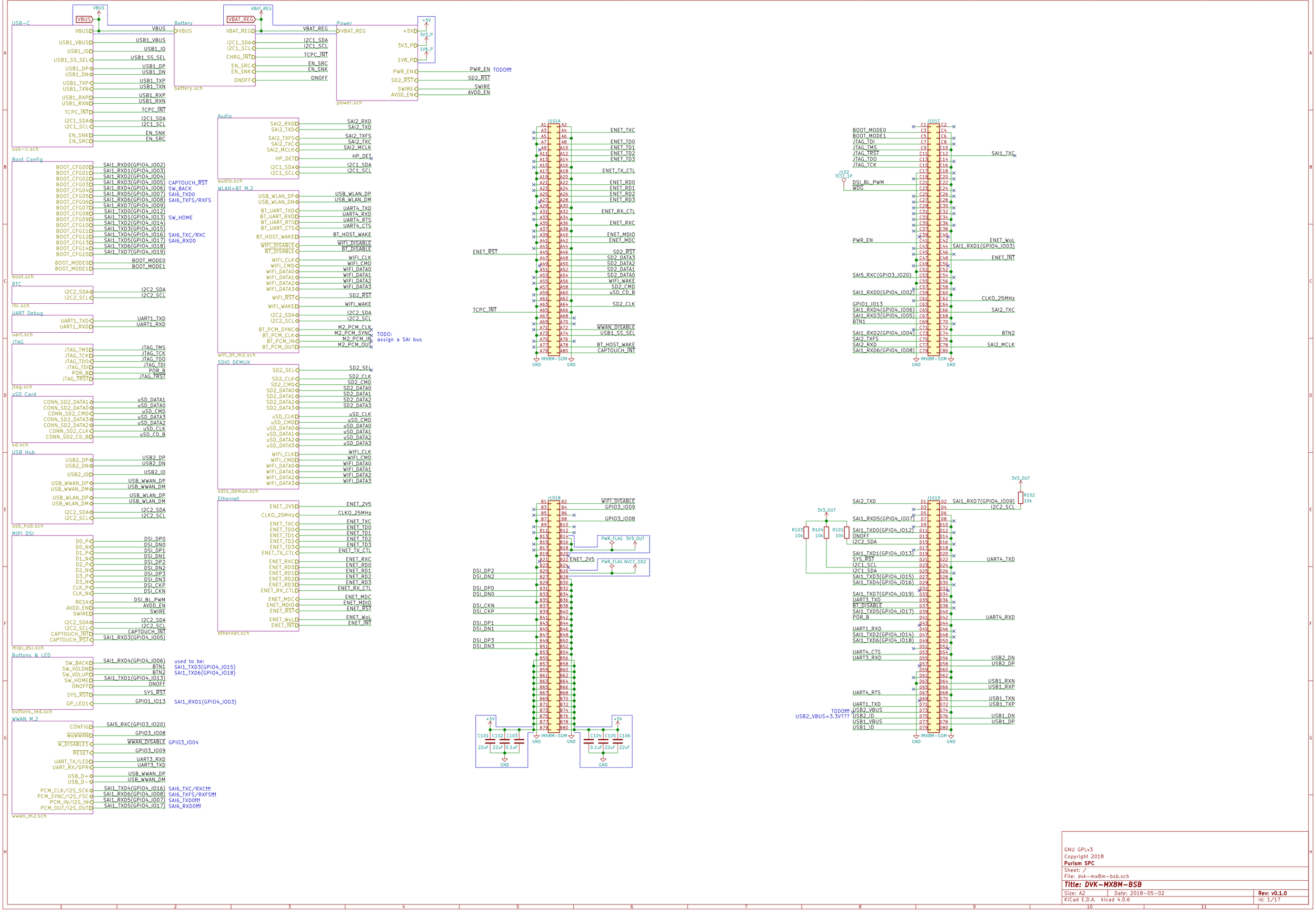


GNU GPLv3
Copyright 2018
Purism SPC

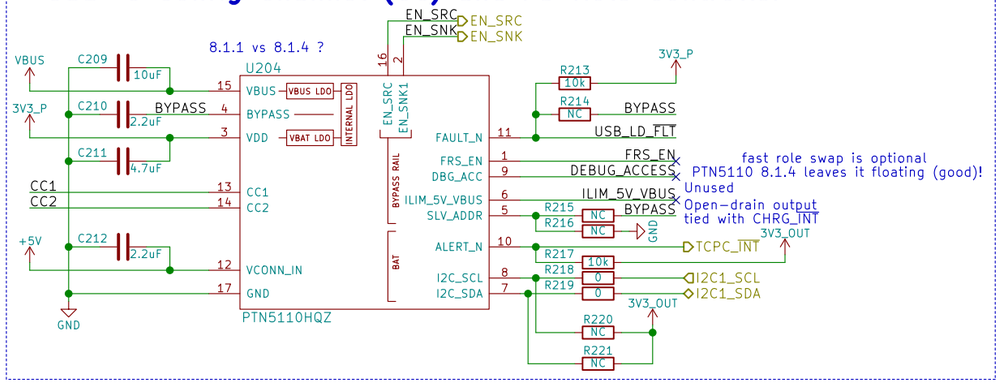
Sheet: /
File: dvk-mx8m-bsb.sch

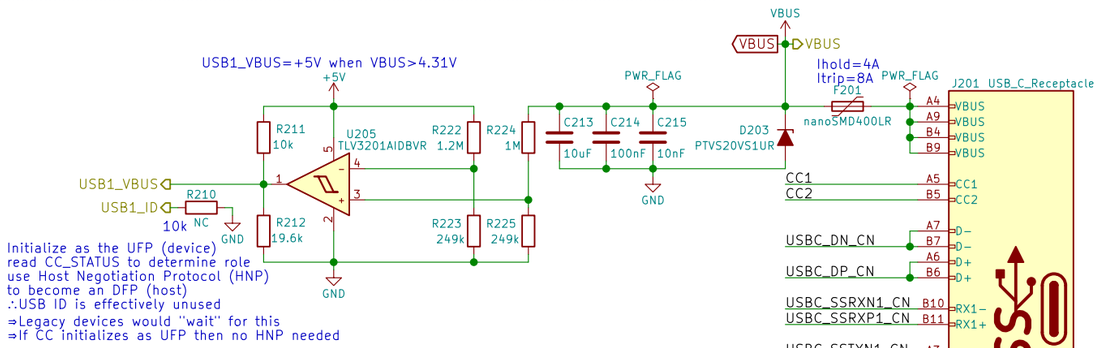
Title: DVK-MX8M-BSB

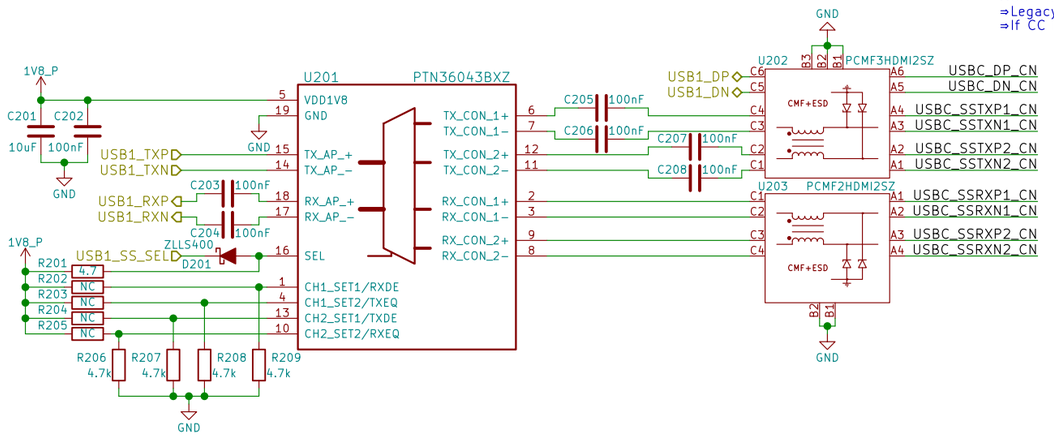
Size: A2	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 1/17

"Under dead battery operation, PTN5110 applies voltage clamps to both CC pins so that the system may receive power as a Sink. To support platforms with buck-boost configuration, PTN5110 asserts EN_SNK1 pin based on validity of VBUS voltage (facilitates 5 V VBUS sinking)."

USB-C Config Channel (CC) and PD Role Controller

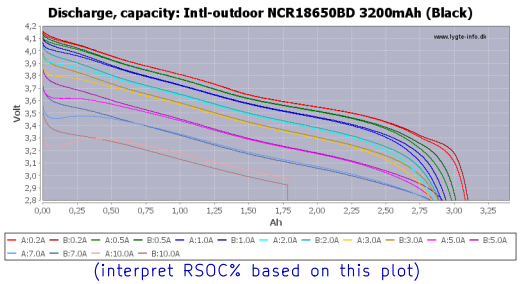






Sheet: /USB-C/		
File: usb-c.sch		
Title: USB Type C		
Size: A3	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 2/17

Battery Charge Controller



(interpret RSOC% based on this plot)

use AUTO_DPDM_EN
to auto-detect IINLIM

1.658≤ILIM≤2.063
ILIM(nom)≅1.859
3.9≤VIN≤14

U301 BQ25896

I(Lsat)=7A

3.5~4.25V

Default LOW:
adapter source

Open-drain output
tied with TCPC_INT

If enough I/O is available then
separate CHRG_INT & TCPC_INT

This disables charging
but maybe not VBUS->VOUT
if PTN5110HQ's FAULT_STATUS[6]==1
(Force Off VBUS bit) then set EN_HiZ=1
EN_HiZ may be auto-set when in hiccup

Reading PTN5110HQ's CC_STATUS and POWER_STATUS
registers will tell TCPM (i.MX8M) when to set EN_HiZ

Also, reading PTN5110HQ's CC_STATUS and POWER_STATUS
registers will tell TCPM (i.MX8M) when to set OTG_CONFIG=1
(this will also happen when PTN5110HQ sets EN_SRC HIGH)

BC1.2 is not mandated by PD spec
ICO used to determine max current
Also negotiated from CC pins (I2C)

Ihold=3.5A
Itrip=6.3A
Ttrip(max)=5s@8A

VBAT(DPL)=2.15~2.5V

Vrm=5.8V
Vz=6.8

NCR18650BD is recommended

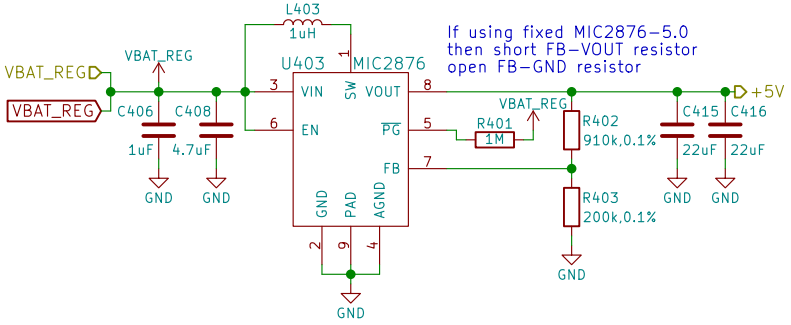
VBAT(nom)=REG06[7:2]
VBAT(default_max_ovp)=(REG06[7:2]×1.005)×1.04=4.3982016V
REG06[7:2]=010111⇒VBAT(max_ovp)=4.3814784
BQ29705 provides 4.425V as OVP!!!

reference design: http://www.ti.com/lit/ug/sluuba2b/sluuba2b.pdf

may want to include BQ29705 protection as in:
http://www.ti.com/lit/ug/tiducl1/tiducl1.pdf
schematic: http://www.ti.com/lit/df/tidrp70/tidrp70.pdf
(PTC may be good enough)

Sheet: /Battery/		
File: battery.sch		
Title: Battery		
Size: A4	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 3/17

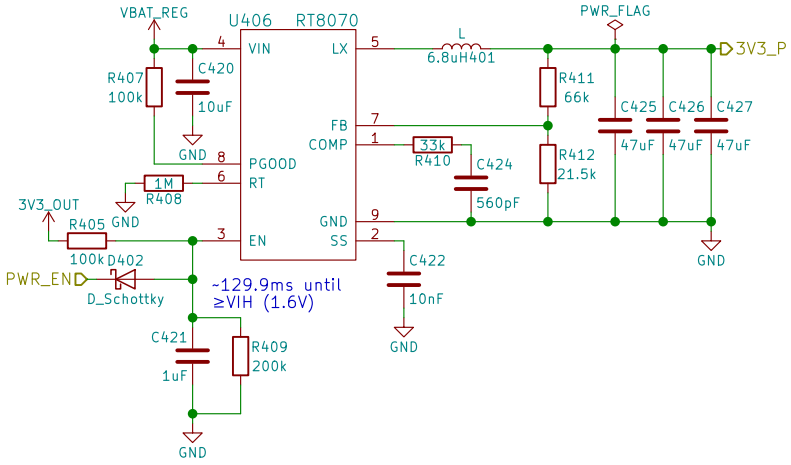
5.0V/3.8A



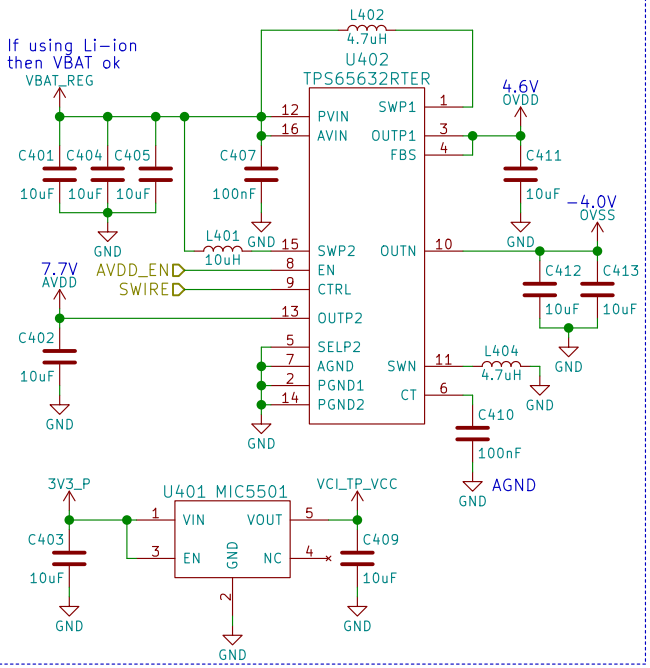
Cheaper, more efficient, smaller, and simpler than RT6150A
Explicitly mentions USB/smartphone application

3.3V/3A

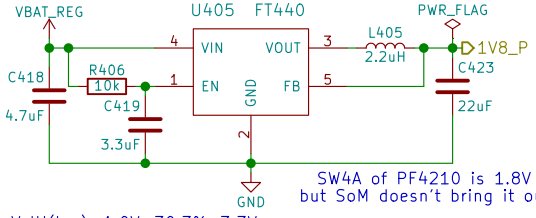
When VBAT can fall below
3.3V use TPS63020 instead!



AMOLED POWER



1.8V/600mA

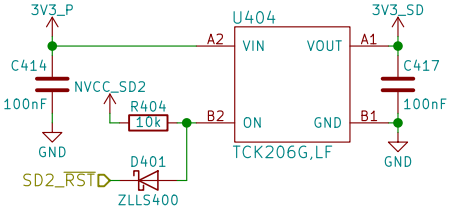


SW4A of PF4210 is 1.8V
but SoM doesn't bring it out

V_IH(typ)=1.0V≅30.3%×3.3V
t(0-30.3%)≈0.361RC
⇒0.361RC≈10ms
∴ R=10k
C=2.77uF≅3.3uF

Buck instead of TLV70218 LDO
saving up to ~100mW loss
LM3670MF-1.8 is much more expensive
ST1S12G18R is a drop-in

SD POWER



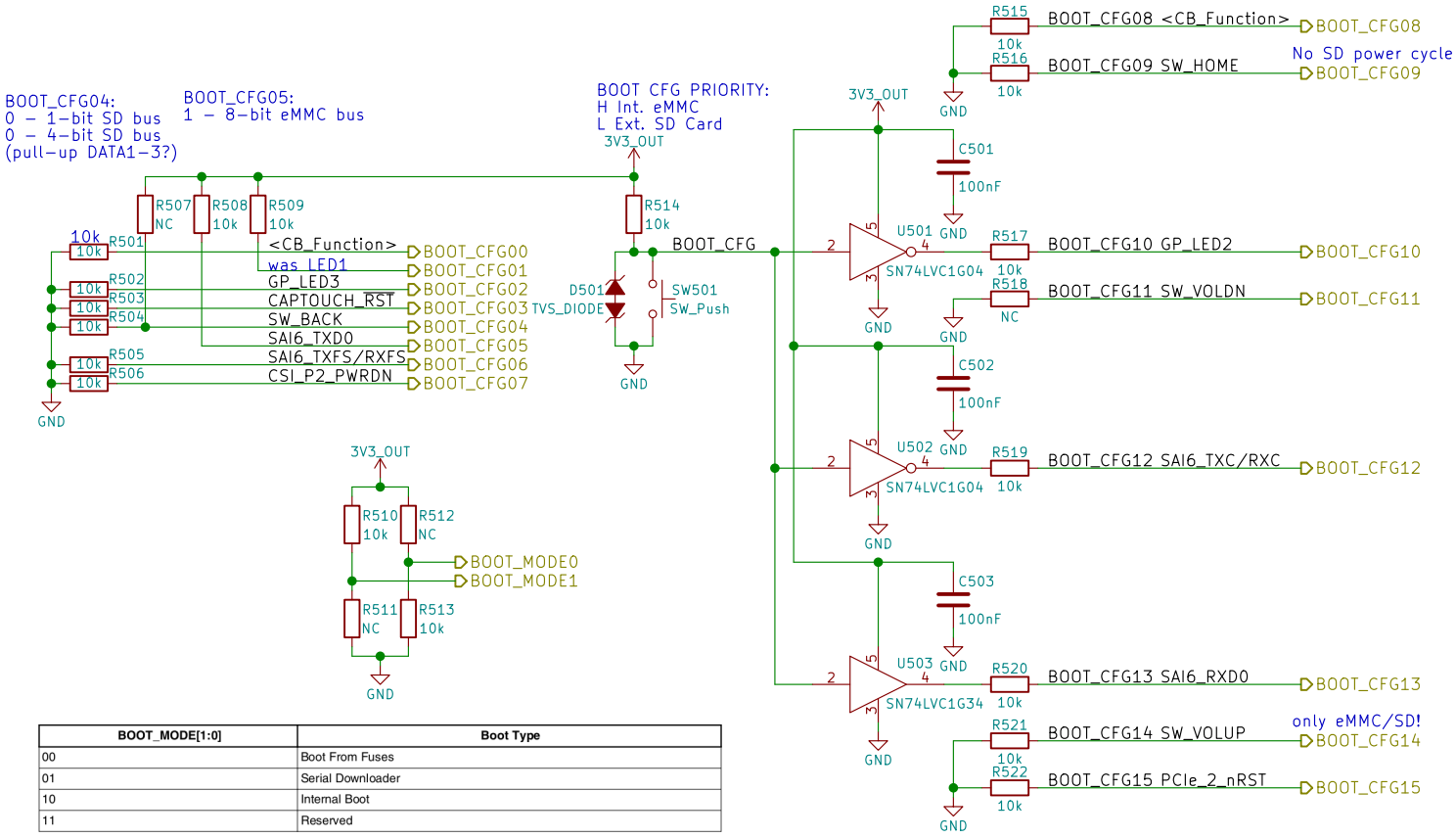
Sheet: /Power/
File: power.sch

Title: Power

Size: A4	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 4/17

BOOT_CFG[14:12]	Boot device
001	SD/eSD
010	MMC/eMMC
011	NAND

Fuse	Config	Definition	GPIO[1]	Shipped value	Settings
BOOT_CFG[11:10]	OEM	USDHC port selection	Yes	00	00 - USDHC-1 01 - USDHC-2 10 - USDHC-3 else - reserved

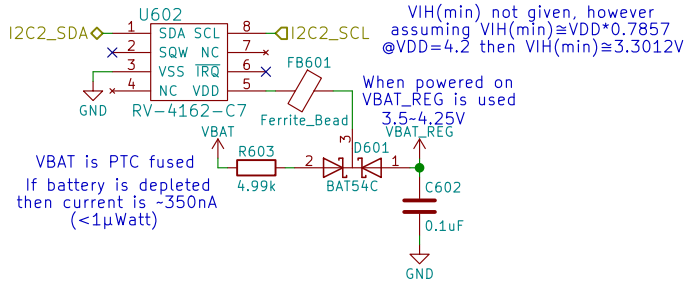


BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

Sheet: /Boot Config/
File: boot.sch

Title: Boot Configuration

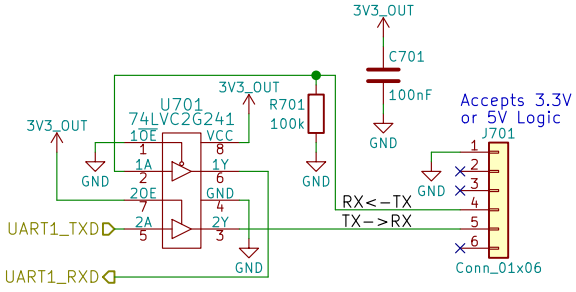
Size: A4	Date: 2018–05–02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 5/17



Sheet: /RTC/
File: rtc.sch

Title: RTC

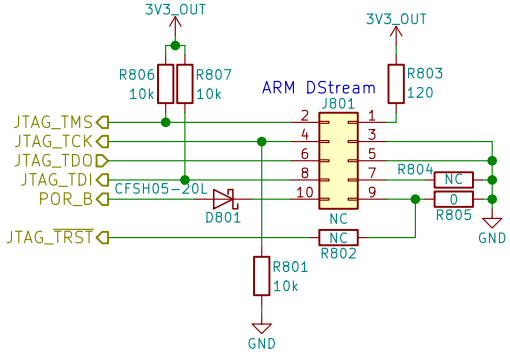
Size: A4	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 6/17



Sheet: /UART Debug/
File: uart.sch

Title: UART Debug

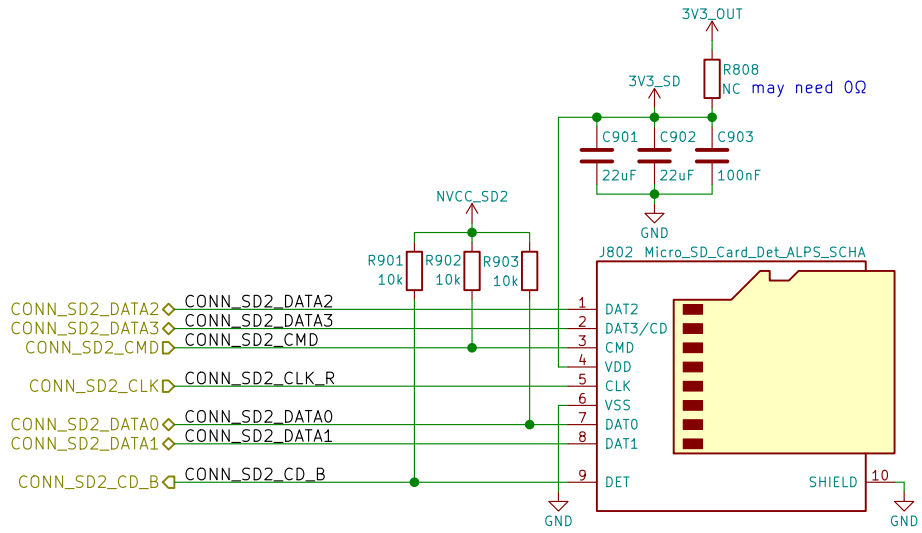
Size: A4	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 7/17

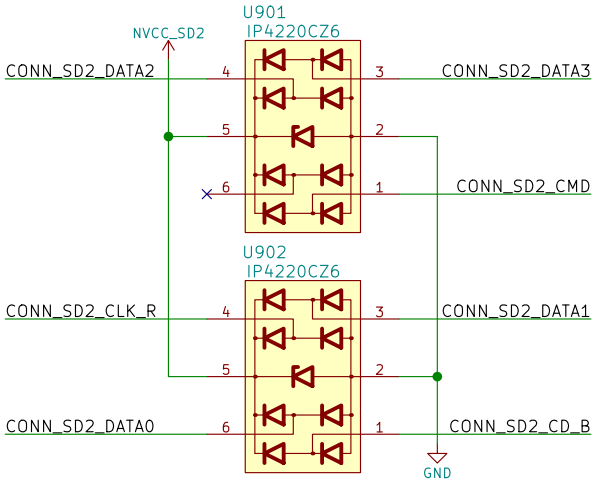


Sheet: /JTAG/
File: jtag.sch

Title: JTAG

Size: A4	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 8/17

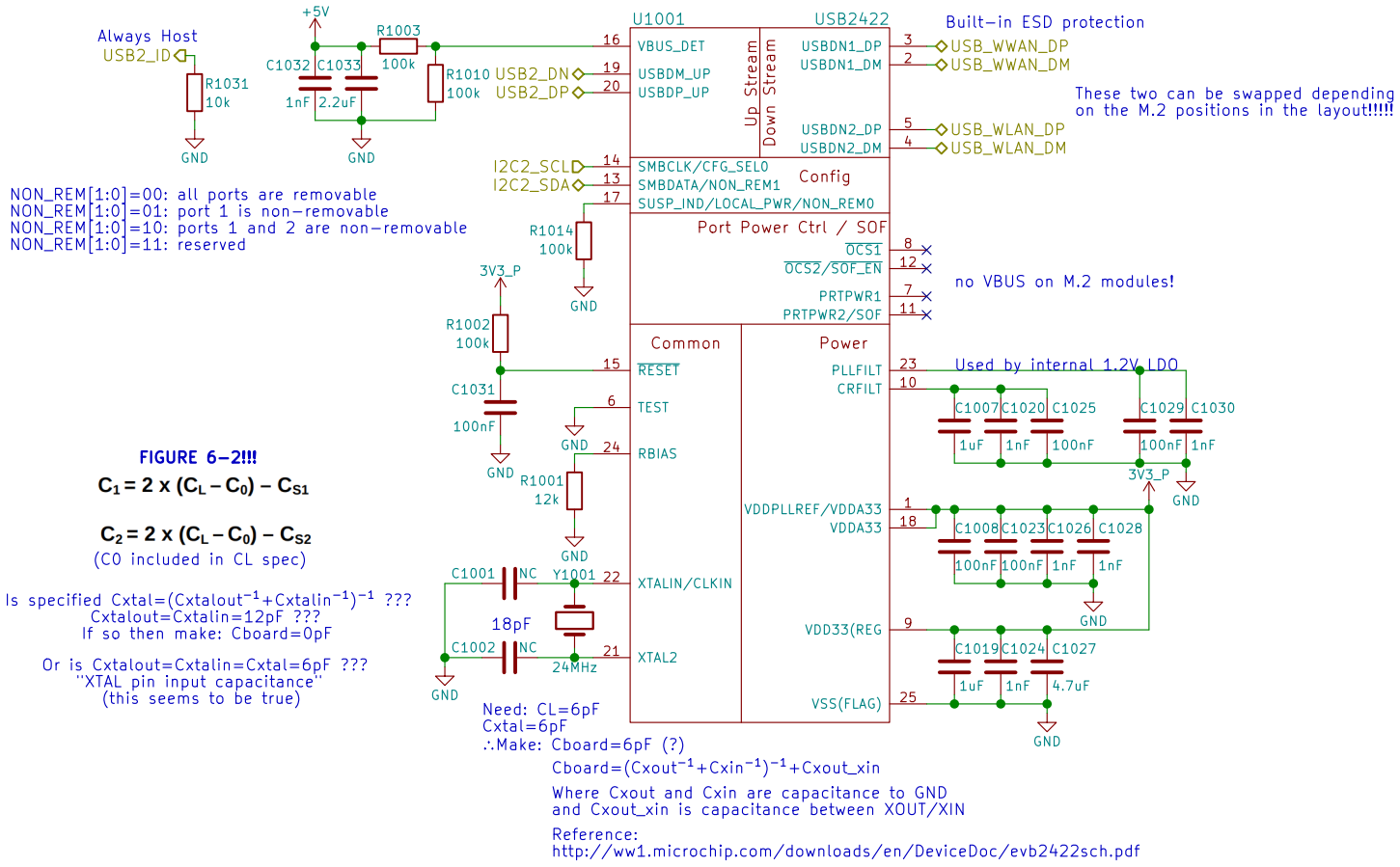




Sheet: /uSD Card/
File: sd.sch

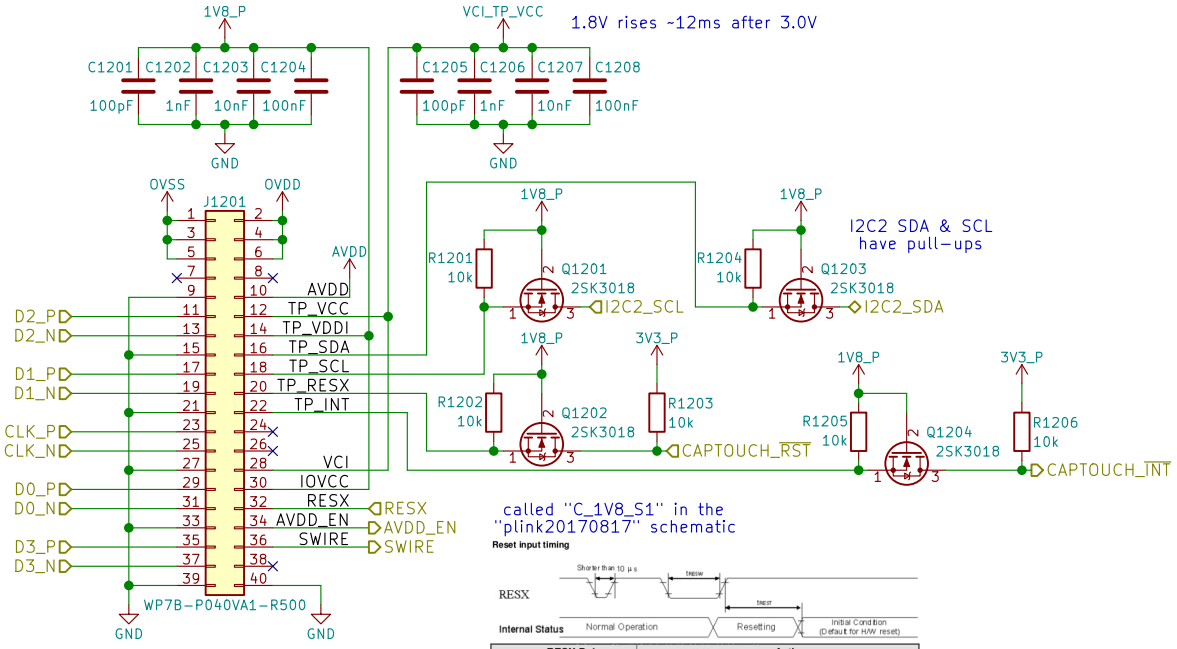
Title: uSD Card

Size: A4	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 9/17



Sheet: /USB Hub/		
File: usb_hub.sch		
Title:		
Size: A4	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 10/17

Using H546DLB01.1 pin assignment may need
to be changed depending on display used



called "C_1V8_S1" in the
"plink20170817" schematic

Reset input timing

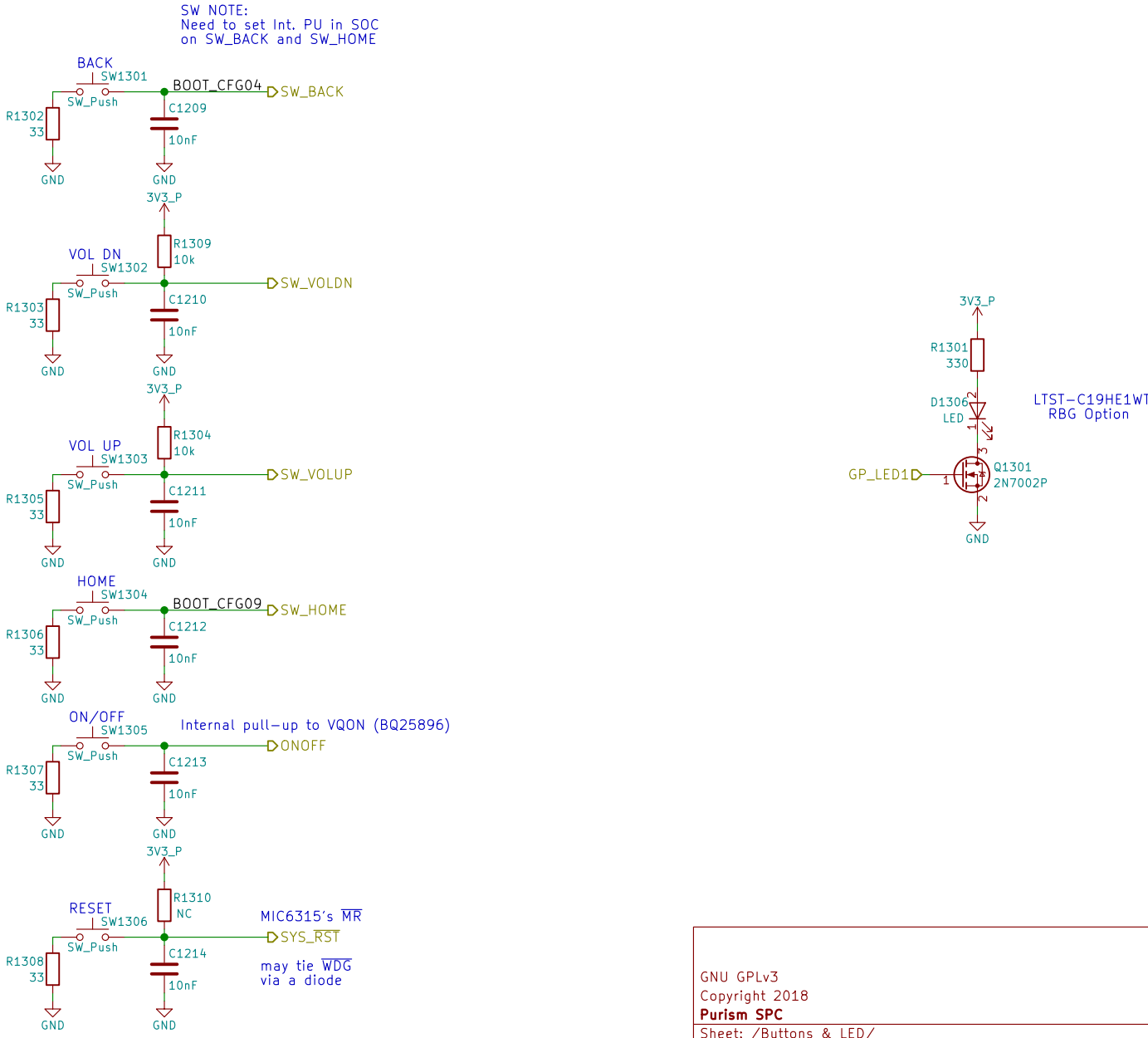
RESX Puise	Action
Shorter than 5µs	Invalid Reset
Longer than 10µs	Valid Reset
Between 5µs and 10µs	Reset Initialization Precedure

TODO: low power state signal??

Sheet: /MIPI DSI/
File: mipi_dsi.sch

Title: MIPI DSI

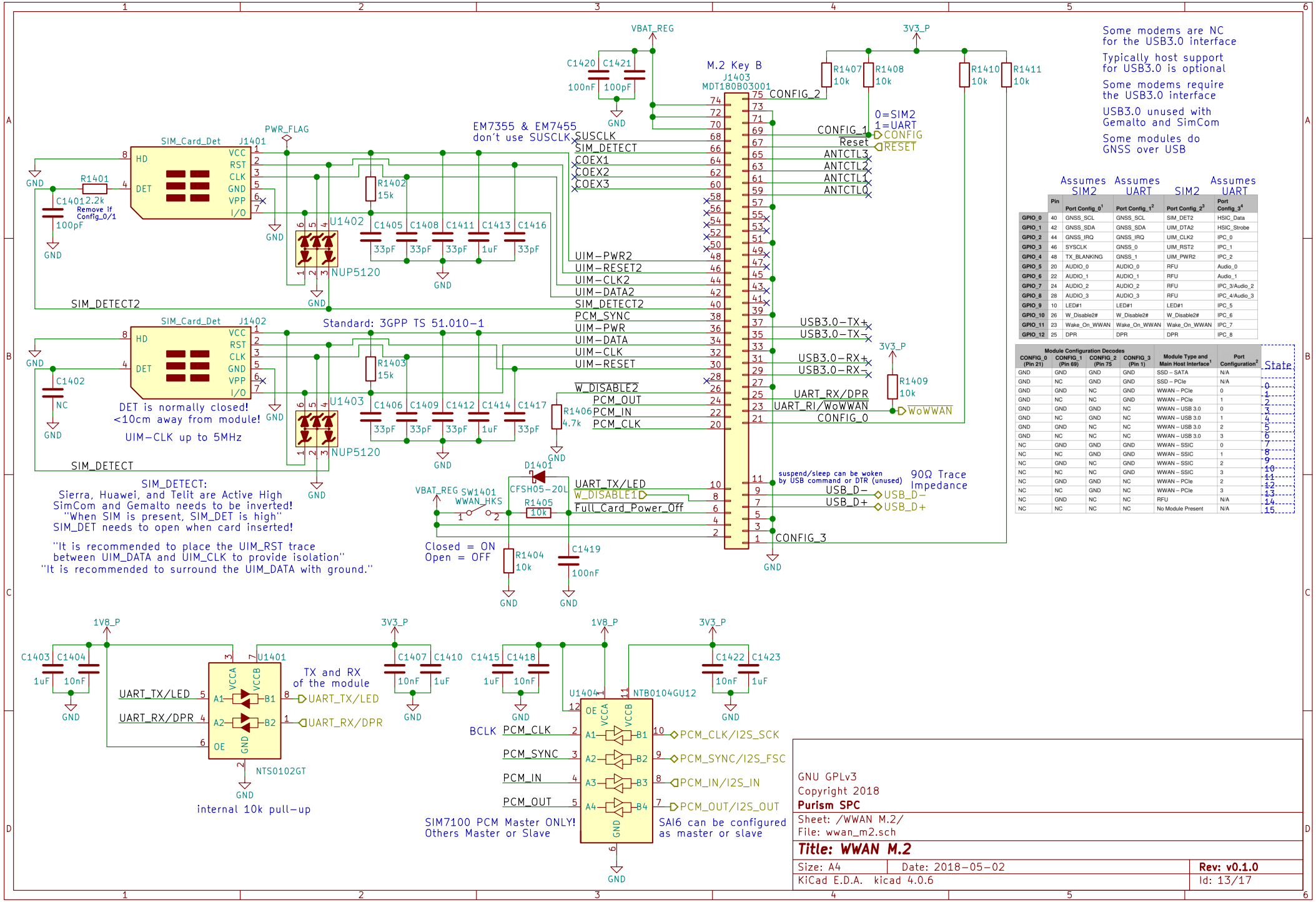
Size: A4 | Date: 2018-05-02 | **Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6 | Id: 11/17

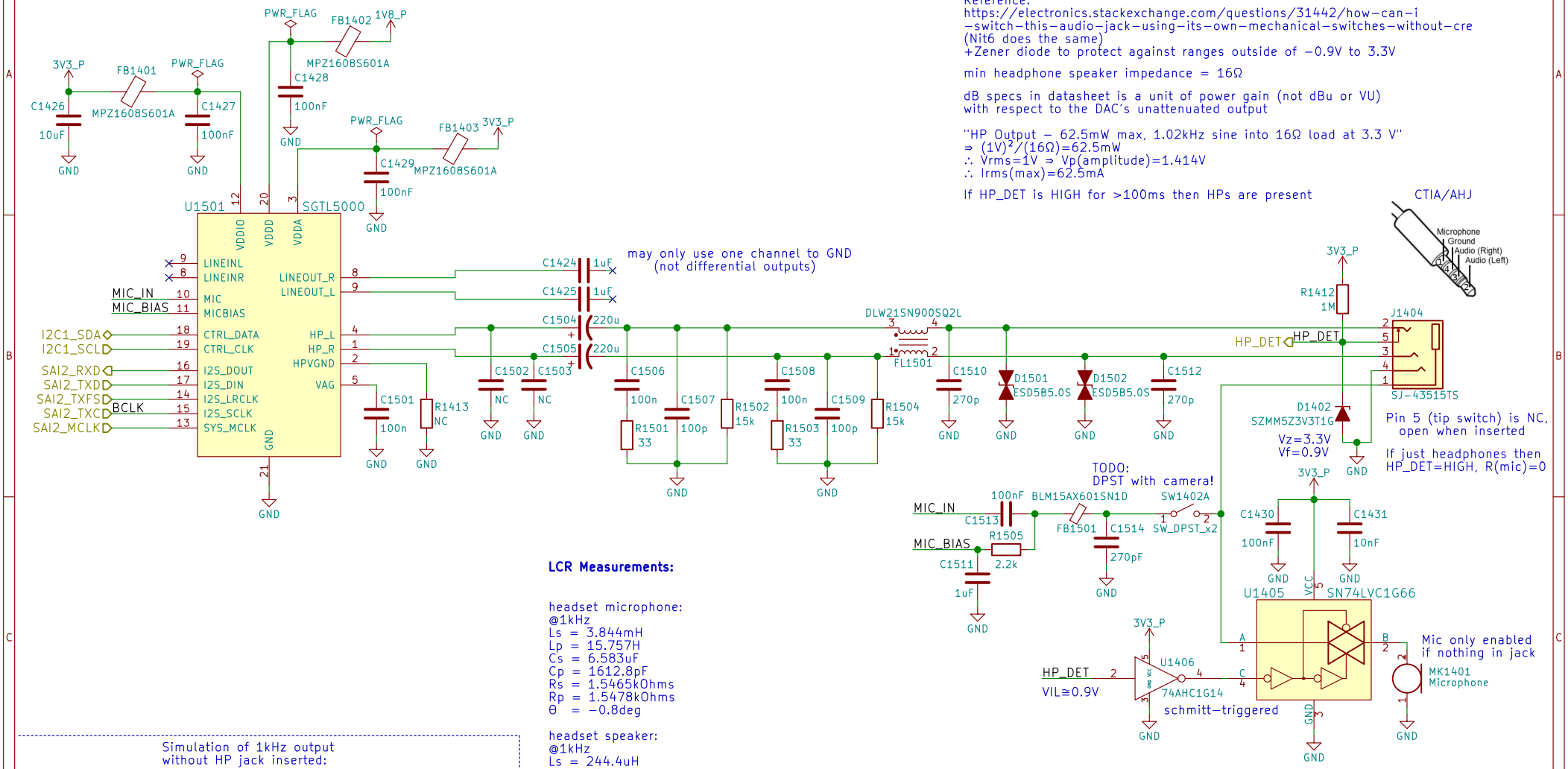


Sheet: /Buttons & LED/
File: buttons_led.sch

Title: Buttons & LED

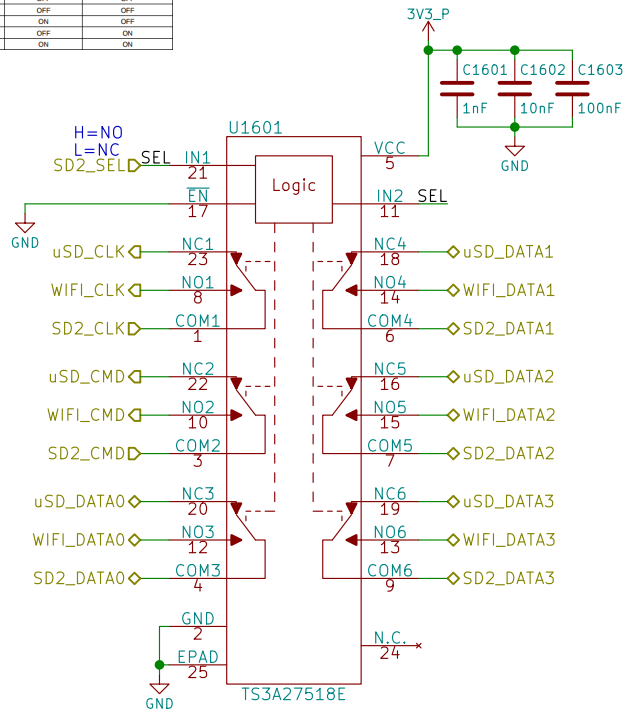
Size: A4	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 12/17


M.2 Key B
J1403
MDT180B03001
SIM_Card_Det
J1401
J1402
U1402
U1403
NUP5120
U1401
NTS0102GT
U1404
NTB0104GU12
D1401
CFSH05-20L
SW1401
WWAN_HKS
VBAT_REG
3V3_P
1V8_P
PWR_FLAG
EM7355 & EM7455
don't use SUSCLK
Standard: 3GPP TS 51.010-1
0=SIM2
1=UART
Some modems are NC
for the USB3.0 interface
Typically host support
for USB3.0 is optional
Some modems require
the USB3.0 interface
USB3.0 unused with
Gemalto and SimCom
Some modules do
GNSS over USB
Assumes SIM2
Assumes UART
Assumes SIM2
Assumes UART
DET is normally closed!
<10cm away from module!
UIM-CLK up to 5MHz
SIM_DETECT:
Sierra, Huawei, and Telit are Active High
SimCom and Gemalto needs to be inverted!
"When SIM is present, SIM_DET is high"
SIM_DET needs to open when card inserted!
"It is recommended to place the UIM_RST trace
between UIM_DATA and UIM_CLK to provide isolation"
"It is recommended to surround the UIM_DATA with ground."
Closed = ON
Open = OFF
suspend/sleep can be woken
by USB command or DTR (unused)
90Ω Trace
Impedance
TX and RX
of the module
internal 10k pull-up
BCLK
SIM7100 PCM Master ONLY!
Others Master or Slave
SAI6 can be configured
as master or slave
GPIO_0 40 GNSS_SCL GNSS_SCL SIM_DET2 HSIC_Data
GPIO_1 42 GNSS_SDA GNSS_SDA UIM_DTA2 HSIC_Strobe
GPIO_2 44 GNSS_IRQ GNSS_IRQ UIM_CLK2 IPC_0
GPIO_3 46 SYSCLK GNSS_0 UIM_RST2 IPC_1
GPIO_4 48 TX_BLANKING GNSS_1 UIM_PWR2 IPC_2
GPIO_5 20 AUDIO_0 AUDIO_0 RFU Audio_0
GPIO_6 22 AUDIO_1 AUDIO_1 RFU Audio_1
GPIO_7 24 AUDIO_2 AUDIO_2 RFU IPC_3/Audio_2
GPIO_8 28 AUDIO_3 AUDIO_3 RFU IPC_4/Audio_3
GPIO_9 10 LED#1 LED#1 LED#1 IPC_5
GPIO_10 26 W_Disable2# W_Disable2# W_Disable2# IPC_6
GPIO_11 23 Wake_On_WWAN Wake_On_WWAN Wake_On_WWAN IPC_7
GPIO_12 25 DPR DPR DPR IPC_8
GND GND GND GND SSD – SATA N/A
GND NC GND GND SSD – PCIe N/A
GND GND NC GND WWAN – PCIe 0 0
GND NC NC GND WWAN – PCIe 1 1
GND GND GND NC WWAN – USB 3.0 0 2
GND NC GND NC WWAN – USB 3.0 1 3
GND GND NC NC WWAN – USB 3.0 2 4
GND NC NC NC WWAN – USB 3.0 3 5
NC GND GND GND WWAN – SSIC 0 6
NC NC GND GND WWAN – SSIC 1 7
NC GND NC GND WWAN – SSIC 2 8
NC NC NC GND WWAN – SSIC 3 9
NC GND GND NC WWAN – PCIe 2 10
NC NC GND NC WWAN – PCIe 3 11
NC GND NC NC RFU N/A 12
NC NC NC NC No Module Present N/A 13
14
15
GNU GPLv3
Copyright 2018
Purism SPC
Sheet: /WWAN M.2/
File: wwan_m2.sch
Title: WWAN M.2
Size: A4
Date: 2018-05-02
Rev: v0.1.0
KiCad E.D.A. kicad 4.0.6
Id: 13/17


Reference:
https://electronics.stackexchange.com/questions/31442/how-can-i-switch-this-audio-jack-using-its-own-mechanical-switches-without-cre
(Nit6 does the same)
+Zener diode to protect against ranges outside of −0.9V to 3.3V
min headphone speaker impedance = 16Ω
dB specs in datasheet is a unit of power gain (not dBu or VU)
with respect to the DAC's unattenuated output
"HP Output − 62.5mW max, 1.02kHz sine into 16Ω load at 3.3 V"
⇒ (1V)²/(16Ω)=62.5mW
∴ Vrms=1V ⇒ Vp(amplitude)=1.414V
∴ Irms(max)=62.5mA
If HP_DET is HIGH for >100ms then HPs are present
U1501
SGTL5000
may only use one channel to GND
(not differential outputs)
DLW21SN900SQ2L
FL1501
CTIA/AHJ
Microphone
Ground
Audio (Right)
Audio (Left)
J1404
SJ-43515TS
Pin 5 (tip switch) is NC,
open when inserted
If just headphones then
HP_DET=HIGH, R(mic)=0
D1402
SZMM5Z3V3T1G
Vz=3.3V
Vf=0.9V
TODO:
DPST with camera!
SW1402A
SW_DPST_x2
U1405
SN74LVC1G66
U1406
74AHC1G14
schmitt-triggered
HP_DET
VIL≅0.9V
Mic only enabled
if nothing in jack
MK1401
Microphone
LCR Measurements:
headset microphone:
@1kHz
Ls = 3.844mH
Lp = 15.757H
Cs = 6.583uF
Cp = 1612.8pF
Rs = 1.5465kOhms
Rp = 1.5478kOhms
θ = −0.8deg
headset speaker:
@1kHz
Ls = 244.4uH
Lp = 141.99mH
Cs = 103.6uF
Cp = 178.77nF
Rs = 36.860hms
Rp = 36.860hms
θ = −2.3deg
headphone speaker:
@1kHz
Ls = 25.2uH
Lp = 311.0mH
Cs = 1.0mF
Cp = 81.95nF
Rs = 17.0300hms
Rp = 17.0340hms
θ = 0.5deg
Simulation of 1kHz output
without HP jack inserted:
transient
simulation
TR1
Type=lin
Start=0 ms
Stop=5 ms
TIME
GNU GPLv3
Copyright 2018
Purism SPC
Sheet: /Audio/
File: audio.sch
Title: Audio
Size: A4
Date: 2018-05-02
Rev: v0.1.0
KiCad E.D.A. kicad 4.0.6
Id: 14/17

Can swap around signals in the layout:

EN	IN1	IN2	NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	OFF	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

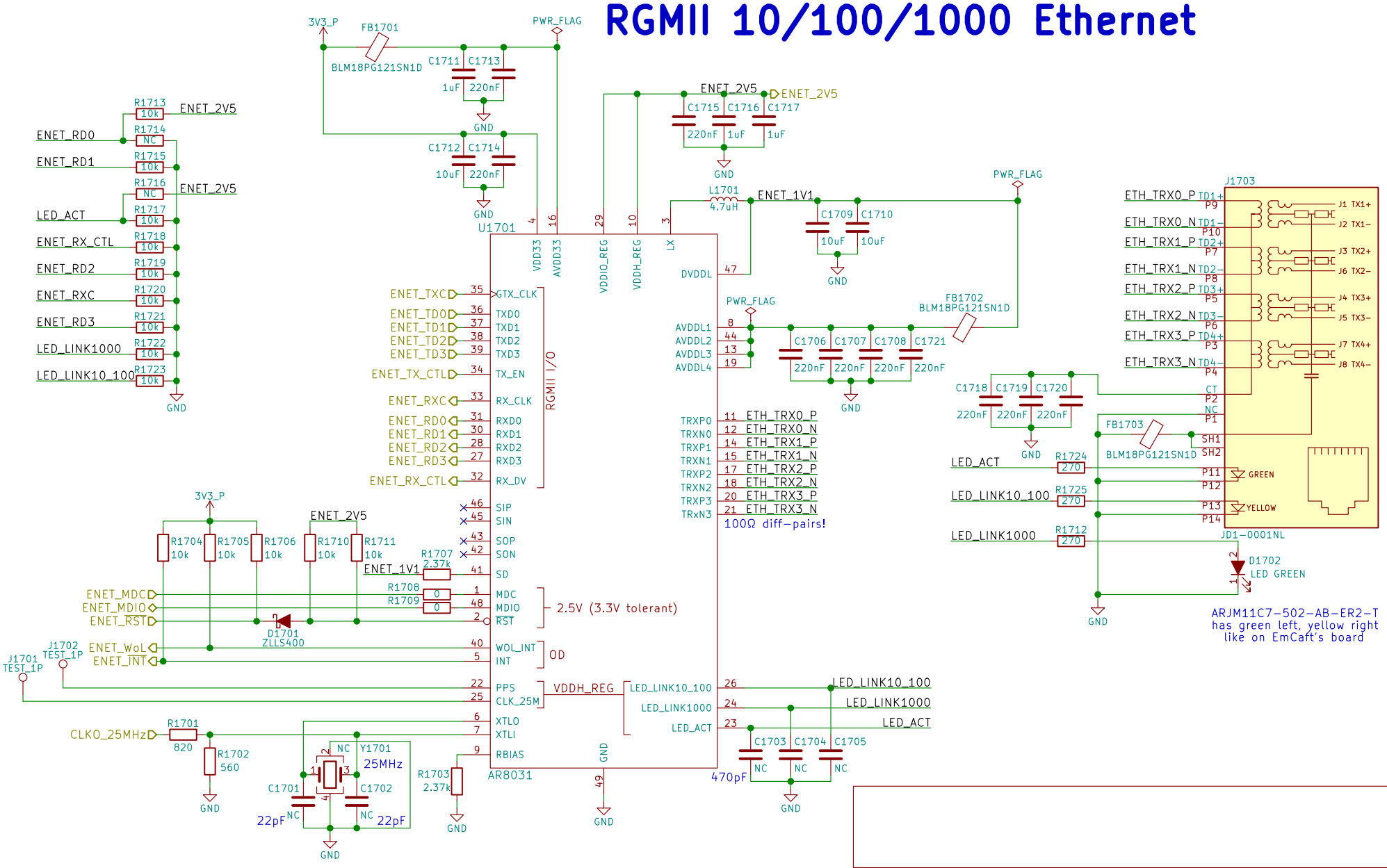


Sheet: /SDIO DEMUX/
File: sdio_demux.sch

Title: SDIO Demultiplexer

Size: A4	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 15/17

RGMII 10/100/1000 Ethernet



Sheet: /Ethernet/
File: ethernet.sch

Title:

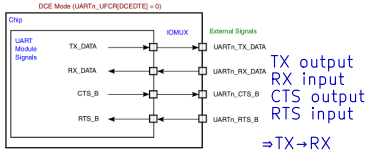
Size: A4	Date:	Rev:
KiCad E.D.A. kicad 4.0.6		Id: 16/17

6.2 M.2 Signal Directions

RS9116 NC:
RTS, CTS, BT_HOST_WAKE, WIFI_WAKE

Module: Table 23
Socket: Table 46

UARTn_UFCR[DCEDTE]=0 on POR



TX output
RX input
CTS output
RTS input

⇒TX→RX
RX←TX
CTS→CTS
RTS←RTS

RedPine RS9116 MB0
Requires +5V for USB!

J1502

3V3_P

USB_WLAN_DP
USB_WLAN_DN

M2_PCM_CLK
M2_PCM_SYNC
M2_PCM_IN
M2_PCM_OUT

WIFI_CLK
WIFI_CMD
WIFI_DATA0
WIFI_DATA1
WIFI_DATA2
WIFI_DATA3
WIFI_WAKE

1V8_P

R1506
10k

BT_HOST_WAKE
BT_UART_RXD

SoC's RX
Module's TX

SoC's TX
Module's RX

BT_UART_TXD
BT_UART_RTS
BT_UART_CTS

WIFI_RST
D1503
ZLLS400

W_DISABLE1
D1504
ZLLS400

RS9116 SUSCLK
is a GPIO (unused)
SUSCLK

W_DISABLE2
W_DISABLE1
M2_I2C_SDA
M2_I2C_SCL

M.2_Key_E

GND

i.MX8M in DCE mode has
CTS output, RTS input

U1502A
74AUP2G00

U1502B
74AUP2G00

BT_DISABLE
WIFI_DISABLE

D1505
CFSH05-20L

Closed = ON (*_DISABLE HIGH)
Open = OFF

SW1501
WWAN_HKS

R1508
10k

C1515
100nF

R1510
10k

TODO:
M.2 spec defines
UART&PCM 1.8V!
but RS9116 is 3.3V!!

U1702
NTB0104GU12

C1722 C1723
1uF 10nF

C1724 C1725
10nF 1uF

OE VCCA VCCB GND
A1 A2 A3 A4
B1 B2 B3 B4

BT_UART_RXD
BT_UART_TXD
BT_UART_RTS
BT_UART_CTS

RX, TX, RTS, CTS
of the SoC

internal 10k pull-up

U1504
NTB0104GU12

C1520 C1521
1uF 10nF

C1522 C1523
10nF 1uF

BCLK
M2_PCM_CLK
M2_PCM_SYNC
M2_PCM_IN
M2_PCM_OUT

BT_PCM_CLK
BT_PCM_SYNC
BT_PCM_IN
BT_PCM_OUT

configure as slave

TODO!!!
verify if translators
with PWR_EN is needed!

R1507
10k

Q1501
FDV301N

I2C2_SDA

RS9116's I2C is part of its
IO_VDD_1 domain
which is 3.0-3.6V!
TODO!!!

R1509
10k

Q1502
FDV301N

I2C2_SCL

RS9116 has SCL as output
⇒master?
(only device on I2C2 bus)

Sheet: /WLAN+BT M.2/
File: wifi_bt_m2.sch

Title: WLAN+BT M.2

Size: A4	Date: 2018-05-02	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.6		Id: 17/17