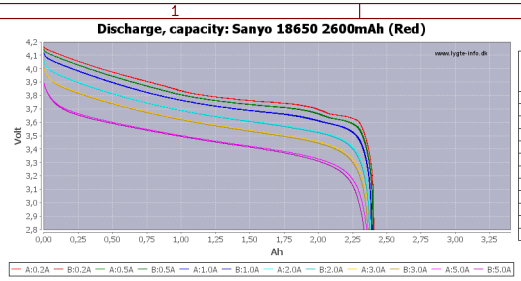
Battery
PWR_SAVE
PMIC_STBY_REQ
battery.sch
Power
PMIC_ON_REQ
PMIC_STBY_REQ
CONN_SD2_RST
power.sch
RTC_Battery
I2C2_SDA
I2C2_SCL
rtc.sch
Audio
SAI2_RXDD
SAI2_TXD
SAI2_TXFS
SAI2_TXC
SAI2_MCLK
audio.sch
Reset & Watchdog
GPIO1_IO02(WDOG)
POR_BD
PMIC_ON_REQD
watchdog.sch
USB
usb.sch
"Varicsite recommends using an external low power time keeping circuitry which is (more) power efficient than the SOC RTC core"
SOM_SNVS_3V3
PWR_FLAG
LICELL2
SOM_NVCC_3V3
Max 100mA
J1A
DART-MX8M
GPIO1_IO00/ENET_PHY_REF_CLK_ROOT/////REF_CLK_32K
ENET_TX_CTL/////GPIO1_IO22/*/NC
ENET_TXC/////GPIO1_IO23/*/LED_LINK10_100
ENET_RXC/////GPIO1_IO25/*/LED_LINK1000
ENET_RX_CTL/////GPIO1_IO24/*/LED_ACT
ENET_MDIO/////GPIO1_IO17
ENET_MDC/////GPIO1_IO16
NVCC_SNVS_3V3
I2C4_SCL/PWM2_OUT//PCIE1_CLKREQ_B/////GPIO5_IO20
I2C4_SDA/PWM1_OUT//PCIE2_CLKREQ_B/////GPIO5_IO21
BT_HOST_WAKE (A23 used to be CLK2_N)
WIFI_HOST_WAKE (A25 used to be CLK2_P)
SD2_WP/////GPIO2_IO20 (A29 used to be CLK1_N)
(A31 used to be CLK1_P)
NAND_DATA07/QSPIB_DATA3/////GPIO3_IO13
NAND_DATA06/QSPIB_DATA2/////GPIO3_IO12
NAND_DATA04/QSPIB_DATA0/////GPIO3_IO10
NAND_RE_B/QSPIB_DQS/////GPIO3_IO15
NAND_DATA05/QSPIB_DATA1/////GPIO3_IO11
NAND_CLE/QSPIB_SCLK/////GPIO3_IO05
NAND_CE2_B/QSPIB_SS0_B/////GPIO3_IO03
PCIE1_REF_CLKN
PCIE1_REF_CLKP
PCIE1_TXN
PCIE1_TXP
PCIE2_RXN
PCIE2_RXP
CSI_P1_DP3
CSI_P1_DN3
CSI_P1_DP1
CSI_P1_DN1
CSI_P1_DN2
CSI_P1_DP2
CSI_P1_DP0
CSI_P1_DN0
CSI_P1_CKP
CSI_P1_CKN
ENET_TD1/////GPIO1_IO20/*/ETH_TRX1_P
ENET_TD0/////GPIO1_IO21/*/ETH_TRX1_N
ENET_TD2/////GPIO1_IO19/*/ETH_TRX0_N
ENET_TD3/////GPIO1_IO18/*/ETH_TRX0_P
ENET_RD0/////GPIO1_IO26/*/ETH_TRX2_P
ENET_RD1/////GPIO1_IO27/*/ETH_TRX2_N
ENET_RD2/////GPIO1_IO28/*/ETH_TRX3_P
ENET_RD3/////GPIO1_IO29/*/ETH_TRX3_N
ONOFF
PMIC_ON_REQ
POR_B
PMIC_STBY_REQ
SD2_RESET_B/////GPIO2_IO19
NAND_DATA01/QSPIA_DATA1/////GPIO3_IO07
NAND_CE0_B/QSPIA_SS0_B/////GPIO3_IO01
NAND_READY_B/////GPIO3_IO16
NAND_DQS/QSPIA_DQS/////GPIO3_IO14
NAND_ALE/QSPIA_SCLK/////GPIO3_IO00
NAND_WP_B/////GPIO3_IO18
NAND_WE_B/////GPIO3_IO17
NAND_DATA03/QSPIA_DATA3/////GPIO3_IO09
NAND_DATA00/QSPIA_DATA0/////GPIO3_IO06
NAND_DATA02/QSPIA_DATA2/////GPIO3_IO08
PCIE2_REF_CLKN
PCIE2_REF_CLKP
PCIE1_RXN
PCIE1_RXP
PCIE2_TXN
PCIE2_TXP
EN_VBAT_3V3
SD2_CD_B/////GPIO2_IO12
SD2_DATA2/////GPIO2_IO17
SD2_DATA1/////GPIO2_IO16
SD2_CLK/////GPIO2_IO13
SD2_DATA3/////GPIO2_IO18
SD2_DATA0/////GPIO2_IO15
SD2_CMD/////GPIO2_IO14
NVCC_SD2_1V8_3V3
PMIC_ON_REQ
POR_B power button!
PMIC_STBY_REQ
CONN_SD2_RST
J1B
DART-MX8M
JTAG_TCK
JTAG_TMS
JTAG_TRST_B
JTAG_TDI
JTAG_TDO
BOOT_MODE1
BOOT_MODE0
HDMI_DDC_SCL
HDMI_DDC_SDA
HDMI_CEC
HDMI_HPD
HDMI_AUX_P
HDMI_AUX_N
HDMI_TX_M_LN_1
HDMI_TX_P_LN_1
HDMI_TX_P_LN_0
HDMI_TX_M_LN_0
HDMI_REFCLK_N
HDMI_REFCLK_P
VDD_PHY_1V8
HDMI_TX_P_LN_2
HDMI_TX_M_LN_2
HDMI_TX_P_LN_3
HDMI_TX_M_LN_3
SAI1_RXFS/SAI5_RXFS/////GPIO4_IO00
SAI1_RXC/SAI5_RXC/////GPIO4_IO01
SAI1_RXD1/SAI5_RXD1/////GPIO4_IO03//////BOOT_CFG01
SAI1_RXD0/SAI5_RXD0/////GPIO4_IO02//////BOOT_CFG00
SAI1_RXD2/SAI5_RXD2/////GPIO4_IO04//////BOOT_CFG02
SAI1_RXD4/SAI6_TXC//SAI6_RXC/////GPIO4_IO06//////BOOT_CFG04
SAI1_TXD1/SAI5_TXD1/////GPIO4_IO13//////BOOT_CFG09
SAI1_RXD5/SAI6_TXD0//SAI6_RXD0///SAI1_RXFS/////GPIO4_IO07//////BOOT_CFG05
SAI1_TXD5/SAI6_RXD0//SAI6_TXD0/////GPIO4_IO17//////BOOT_CFG13
SAI1_TXD3/SAI5_TXD3/////GPIO4_IO15//////BOOT_CFG11
ECSPI1_SCLK/UART3_RX/////GPIO5_IO06
ECSPI1_SS0/UART3_RTS_B/////GPIO5_IO09
ECSPI1_MISO/UART3_CTS_B/////GPIO5_IO08
ECSPI1_MOSI/UART3_TX/////GPIO5_IO07
UART2_RXD/ECSPI3_MISO/////GPIO5_IO24
UART3_RXD/UART1_CTS_B/////GPIO5_IO26
UART3_TXD/UART1_RTS_B/////GPIO5_IO27
SAI3_TXD/GPT1_COMPARE3//SAI5_RXD3/////GPIO5_IO01/*/HPLOUT
SAI3_TXC/GPT1_COMPARE2//SAI5_RXD2/////GPIO5_IO00/*/HPROUT
SAI3_RXFS/GPT1_CAPTURE1//SAI5_RXFS/////GPIO4_IO28/*/HPOUTFB
SAI3_RXC/GPT1_CAPTURE2//SAI5_RXC/////GPIO4_IO29/*/LINEIN1_LP
SAI3_TXFS/GPT1_CLK//SAI5_RXD1/////GPIO4_IO31/*/LINEIN1_RP
AGND
SAI3_RXD/GPT1_COMPARE1//SAI5_RXD0/////GPIO4_IO30/*/DMIC_CLK
SAI3_MCLK/PWM4_OUT//SAI5_MCLK/////GPIO5_IO02/*/DMIC_DATA
ECSPI2_MOSI/UART4_TX/////GPIO5_IO11
ECSPI2_MISO/UART4_CTS_B/////GPIO5_IO12
ECSPI2_SCLK/UART4_RX/////GPIO5_IO10
ECSPI2_SS0/UART4_RTS_B/////GPIO5_IO13
GPIO1_IO02/WDOG_B
I2C2_SDA/ENET1_1588_EVENT1_OUT/////GPIO5_IO17
I2C2_SCL/ENET1_1588_EVENT1_IN/////GPIO5_IO16
SAI5_RXFS/SAI1_TXD0/////GPIO3_IO19
SAI5_RXD0/SAI1_TXD2/////GPIO3_IO21
SAI5_RXD2/SAI1_TXD4//SAI1_TXFS///SAI5_TXC/////GPIO3_IO23
SAI5_RXC/SAI1_TXD1/////GPIO3_IO20
SAI5_RXD1/SAI1_TXD3//SAI1_TXFS///SAI5_TXFS/////GPIO3_IO22
SAI5_RXD3/SAI1_TXD5//SAI1_TXFS///SAI5_TXD0/////GPIO3_IO24
SAI5_MCLK/SAI1_TXC//SAI4_MCLK/////GPIO3_IO25
SAI2_RXFS/SAI5_TXFS/////GPIO4_IO21
SAI2_RXC/SAI5_TXC/////GPIO4_IO22
SAI2_TXFS/SAI5_TXD1/////GPIO4_IO24
SAI2_MCLK/SAI5_MCLK/////GPIO4_IO27
SAI2_TXC/SAI5_TXD2/////GPIO4_IO25
SAI2_RXD0/SAI5_TXD0/////GPIO4_IO23
SAI2_TXD0/SAI5_TXD3/////GPIO4_IO26
SAI1_RXD3/SAI5_RXD3/////GPIO4_IO05//////BOOT_CFG03
SAI1_TXFS/SAI5_TXFS/////GPIO4_IO10
SAI1_RXD6/SAI6_TXFS//SAI6_RXFS/////GPIO4_IO08//////BOOT_CFG06
SAI1_RXD7/SAI6_MCLK//SAI1_TXFS///SAI1_TXD4/////GPIO4_IO09//////BOOT_CFG07
SAI1_TXD0/SAI5_TXD0/////GPIO4_IO12//////BOOT_CFG08
SAI1_TXC/SAI5_TXC/////GPIO4_IO11
SAI1_TXD4/SAI6_RXC//SAI6_TXC/////GPIO4_IO16//////BOOT_CFG12
SAI1_TXD7/SAI6_MCLK/////GPIO4_IO19//////BOOT_CFG15
SAI1_TXD2/SAI5_TXD2/////GPIO4_IO14//////BOOT_CFG10
SAI1_TXD6/SAI6_RXFS//SAI6_TXFS/////GPIO4_IO18//////BOOT_CFG14
SAI1_MCLK/SAI5_MCLK//SAI1_TXC/////GPIO4_IO20
UART2_TXD/ECSPI3_SSO/////GPIO5_IO25
UART1_RXD/ECSPI3_SCLK/////GPIO5_IO22
UART1_TXD/ECSPI3_MOSI/////GPIO5_IO23
PWR_FLAG
GNDA
BASE_PER_3V3
R1 10k
R2 10k
GPIO1_IO02/WDOG_B
I2C2_SDA
I2C2_SCL
SAI2_TXFS
SAI2_MCLK
SAI2_TXC
SAI2_RXD
SAI2_TXD
J1C
DART-MX8M
UART4_TXD/UART2_RTS_B//PCIE2_CLKREQ_B/////GPIO5_IO29
UART4_RXD/UART2_CTS_B//PCIE1_CLKREQ_B/////GPIO5_IO28
NC/*/LVDS1_TX2_P
NC/*/LVDS1_TX2_N
NC/*/LVDS1_CLK_P
NC/*/LVDS1_CLK_N
NC/*/LVDS1_TX3_P
NC/*/LVDS1_TX3_N
DSI_TX2_P/*/LVDS2_CLK_P
DSI_TX2_N/*/LVDS2_CLK_N
DSI_CLK_N/*/LVDS2_TX2_N
DSI_CLK_P/*/LVDS2_TX2_P
USB2_RXN
USB2_RXP
USB2_TXN
USB2_TXP
USB2_DP
USB2_DN
USB1_RXN
USB1_RXP
USB1_TXN
USB1_TXP
USB1_DP
USB1_DN
VBAT_3V3
VBAT
NC/*/LVDS1_TX0_P
NC/*/LVDS1_TX0_N
NC/*/LVDS1_TX1_P
NC/*/LVDS1_TX1_N
DSI_TX0_P/*/LVDS2_TX0_P
DSI_TX0_N/*/LVDS2_TX0_N
DSI_TX1_P/*/LVDS2_TX1_P
DSI_TX1_N/*/LVDS2_TX1_N
DSI_TX3_P/*/LVDS2_TX3_P
DSI_TX3_N/*/LVDS2_TX3_N
USB2_VBUS
SPDIF_RX/PWM2_OUT/////GPIO5_IO04
GPIO1_IO11/USB2_OTG_ID/////PMIC_READY
SPDIF_EXT_CLK/PWM1_OUT/////GPIO5_IO05
SPDIF_TX/PWM3_OUT/////GPIO5_IO03
GPIO1_IO15/USB2_OTG_OC/////PWM4_OUT/////CLKO2
GPIO1_IO13/USB1_OTG_OC/////PWM2_OUT
I2C3_SDA/PWM3_OUT//GPT3_CLK/////GPIO5_IO19
USB2_ID
I2C3_SCL/PWM4_OUT//GPT2_CLK/////GPIO5_IO18
GPIO1_IO14/USB2_OTG_PWR/////PWM3_OUT
GPIO1_IO12/USB1_OTG_PWR
GPIO1_IO10/USB1_OTG_ID
GPIO1_IO03/USDHC1_VSELECT/////XTAL_OK
USB1_ID
GPIO1_IO06/////SD1_CD_B/////EXT_CLK3
GPIO1_IO08/ENET1_1588_EVENT0_IN/////SD2_RESET_B
GPIO1_IO05/M4_NMI/////PMIC_READY
GPIO1_IO01/PWM1_OUT/////REF_CLK_24M/////EXT_CLK2
USB1_VBUS
CSI_P2_CKN
CSI_P2_CKP
CSI_P2_DN3
CSI_P2_DP3
CSI_P2_DN1
CSI_P2_DP1
CSI_P2_DN0
CSI_P2_DP0
CSI_P2_DN2
CSI_P2_DP2
Internal SOM regulator 3.3V output generated from VBAT used to be LICELL
SOM_VBAT_3V3
Max 100mA
SOM_VBAT
GND

Purism SPC
Sheet: /
File: dvk-dart-mx8m.sch
Title: DVK-DART-MX8M
Size: A2 | Date: 2018-04-05 | Rev: v0.1.0
KiCad E.D.A. kicad 4.0.7 | Id: 1/7



Estimated remaining capacity

Voltage	AW 18650 2600mAh (Black)	Sanyo 18650 2600mAh (Red)	Panasonic CGR18650CH 2250mAh	Panasonic NCR18650A 3100mAh	Panasonic NCR18650B 3400mAh
4.2	100%	100%	100%	100%	100%
4.1	92%	92%	94%	94%	94%
4.0	78%	79%	85%	83%	84%
3.9	61%	63%	76%	73%	74%
3.8	43%	44%	66%	60%	62%
3.7	14%	15%	54%	52%	53%
3.6	3%	5%	26%	38%	39%
3.5	1%	2%	12%	20%	22%
3.4	0%	1%	5%	11%	13%
3.3	0%	0%	2%	1%	3%
3.2	0%	0%	0%	0%	0%

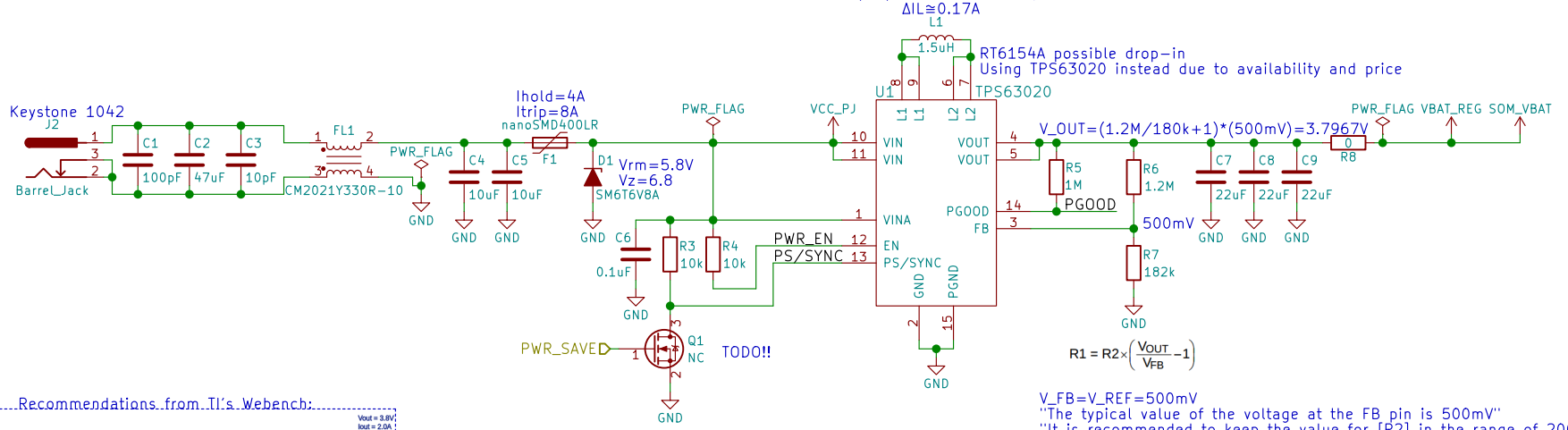
Measured 1 hour after discharge at 1A

⇒18650 batteries don't reach 3.3V until depleted

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L}$$

$$\frac{2A}{0.9\times\left(1-\left(\frac{3.7967V-3.0V}{3.7967V}\right)\right)}+\frac{3.0V\times\left(\frac{3.7967V-3.0V}{3.7967V}\right)}{2\times2.4MHz\times1.5uH}=2.899803756A$$

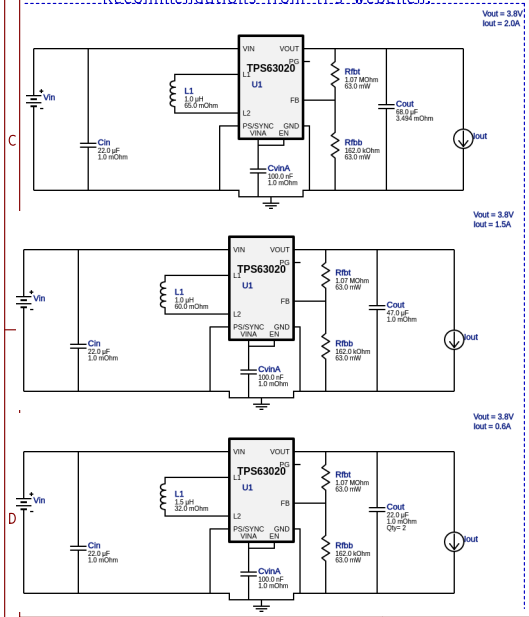
Calculated Ipeak≅2.9A
IL(sat)=4.4A @ 20% drop
ΔIL≅0.17A



$$R1 = R2\times\left(\frac{V_{OUT}}{V_{FB}}-1\right)$$

V_FB=V_REF=500mV
"The typical value of the voltage at the FB pin is 500mV"
"It is recommended to keep the value for [R2] in the range of 200kΩ; lower than 500kΩ"
Their example application circuit uses 180k for R2, therefore:
R2≅200k±20k (±10%) or 180k~220k
Given this, V_OUT≅3.8V, 1.1188M≤R1≤1.452M
The most common value in this range is 1.2M
Making R2≅181.818k or roughly 182k

Recommendations from TI's Webench:

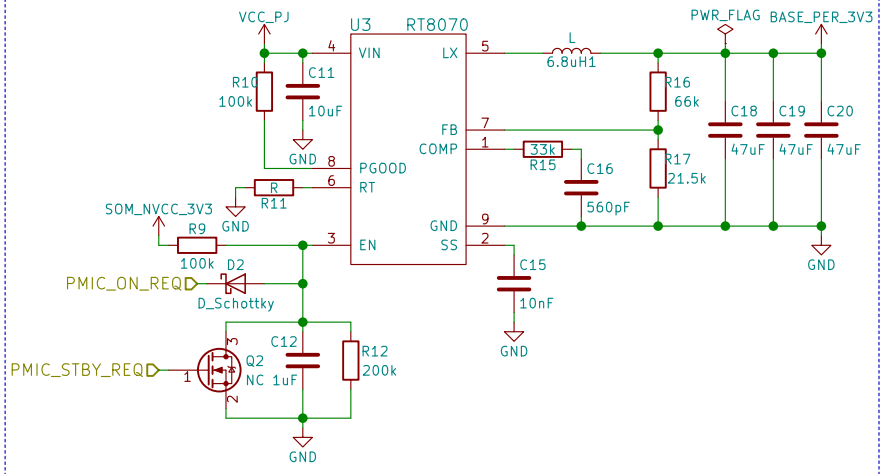


Sheet: /Battery/
File: battery.sch

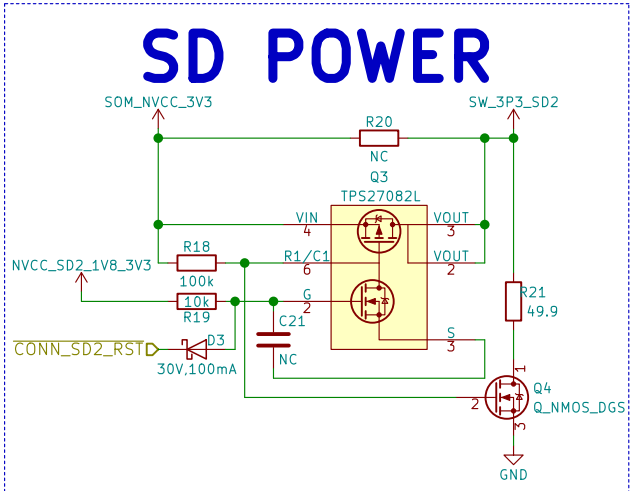
Title: Battery

Size: A4	Date: 2018-04-05	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 2/7

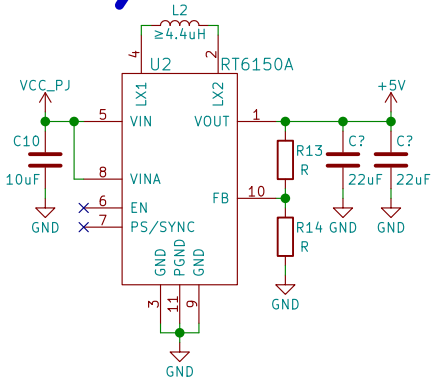
3.3V/3A



SD POWER



5.0V/800mA

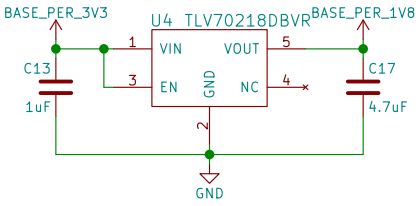


for Cout≥27.2uF ⇒ ΔVout,peak(Boost)≤10mV
or ≤0.2% ripple

0.2×Iout(max)≤ΔIL≤0.4×Iout(max)
for ΔIL≅34.44%×Iout(max)
⇒ L≅4.4uH

their example:
for Vin(min)=2.5V, Vout=3.3V, L=2.2uH
⇒ ΔIL=0.275482A≅34.44% of Iout(max) (being 0.8A)

1.8V/300mA

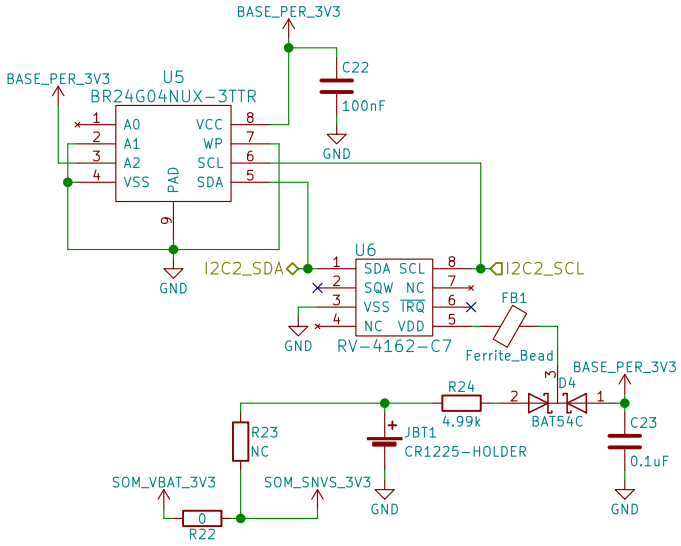


Purism SPC

Sheet: /Power/
File: power.sch

Title: Power

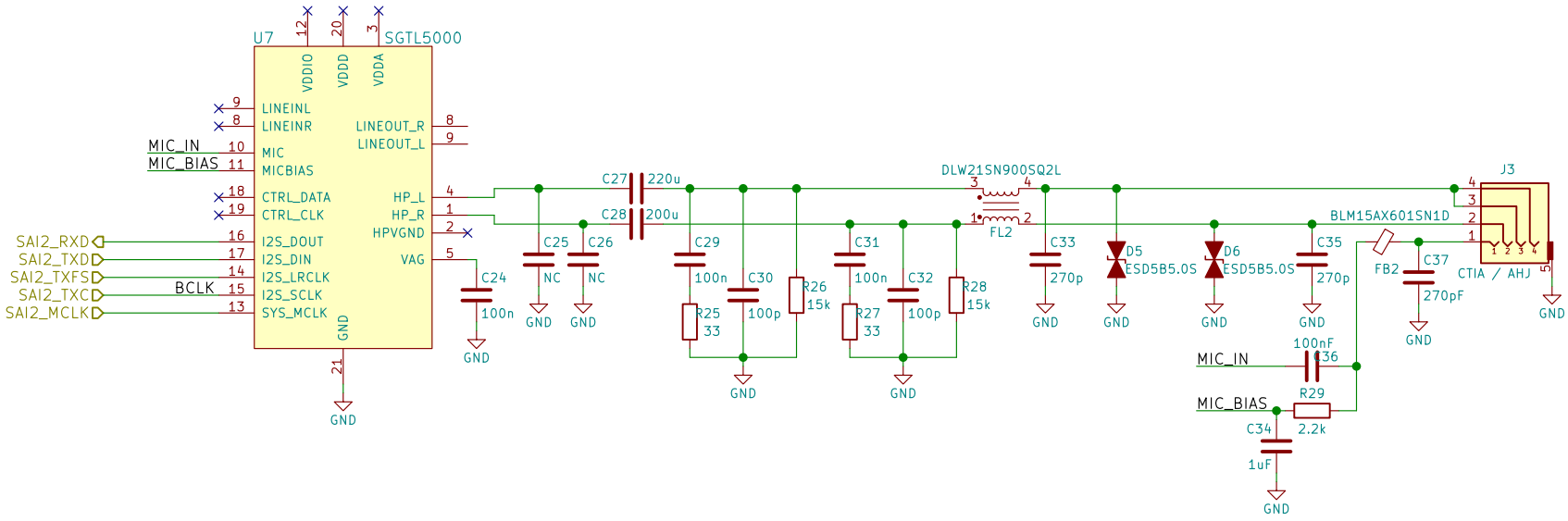
Size: A4	Date: 2018-04-05	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 3/7



Sheet: /RTC Battery/
File: rtc.sch

Title: RTC Battery

Size: A4	Date: 2018-04-05	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 4/7

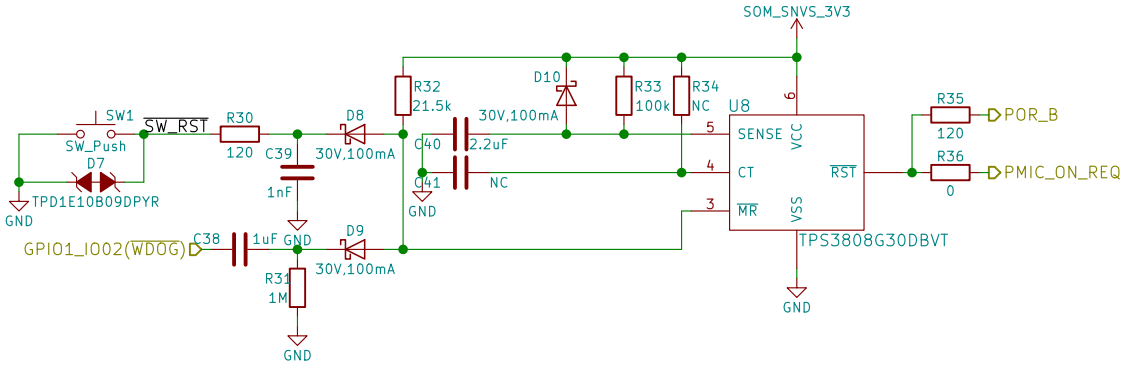


GNU GPLv3
Copyright 2018
Purism SPC

Sheet: /Audio/
File: audio.sch

Title: Audio

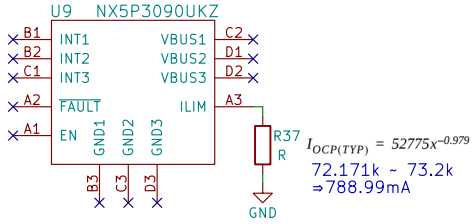
Size: A4	Date: 2018-04-05	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 5/7



Sheet: /Reset & Watchdog/
File: watchdog.sch

Title: Reset & Watchdog

Size: A4	Date: 2018-04-05	**Rev: v0.1.0**
KiCad E.D.A. kicad 4.0.7		Id: 6/7



Sheet: /USB/ File: usb.sch		
Title:		
Size: A4	Date: 2018-04-05	**Rev:**
KiCad E.D.A. kicad 4.0.7		Id: 7/7