

USB-C TCPC – Config Channel (CC) and PD Role Controller

8.1.1 vs 8.1.4 ?

fast role swap is optional
PTN5110 8.1.4 leaves it floating..(good)!

Unused
Open-drain output
tied with CHRG_INT
3V3_OUT

Read: 0xA5
Write: 0xA4
7-Bit Slave Address: 0x52
(1010 010x)

Initialize as the UFP (device)
read CC_STATUS to determine role
use Host Negotiation Protocol (HNP)
to become an DFP (host)
∴ USB ID is effectively unused
⇒ Legacy devices would "wait" for this
⇒ If CC initializes as UFP then no HNP needed

USB1_VBUS=5V when VBUS>4.31V

Under dead battery operation, PTN5110 applies voltage clamps to both CC pins so that the system may receive power as a Sink. To support platforms with buck-boost configuration, PTN5110 asserts EN_SNK1 pin based on validity of VBUS voltage (facilitates 5 V VBUS sinking)."

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Purism SPC
Sheet: /USB-C/
File: usb-c.sch

Title: USB Type C

Size: A4 Date: 2018-06-07
KiCad E.D.A. kicad 4.0.7

Rev: v0.1.0
Id: 2/24



(interpret RSOC% based on this plot)

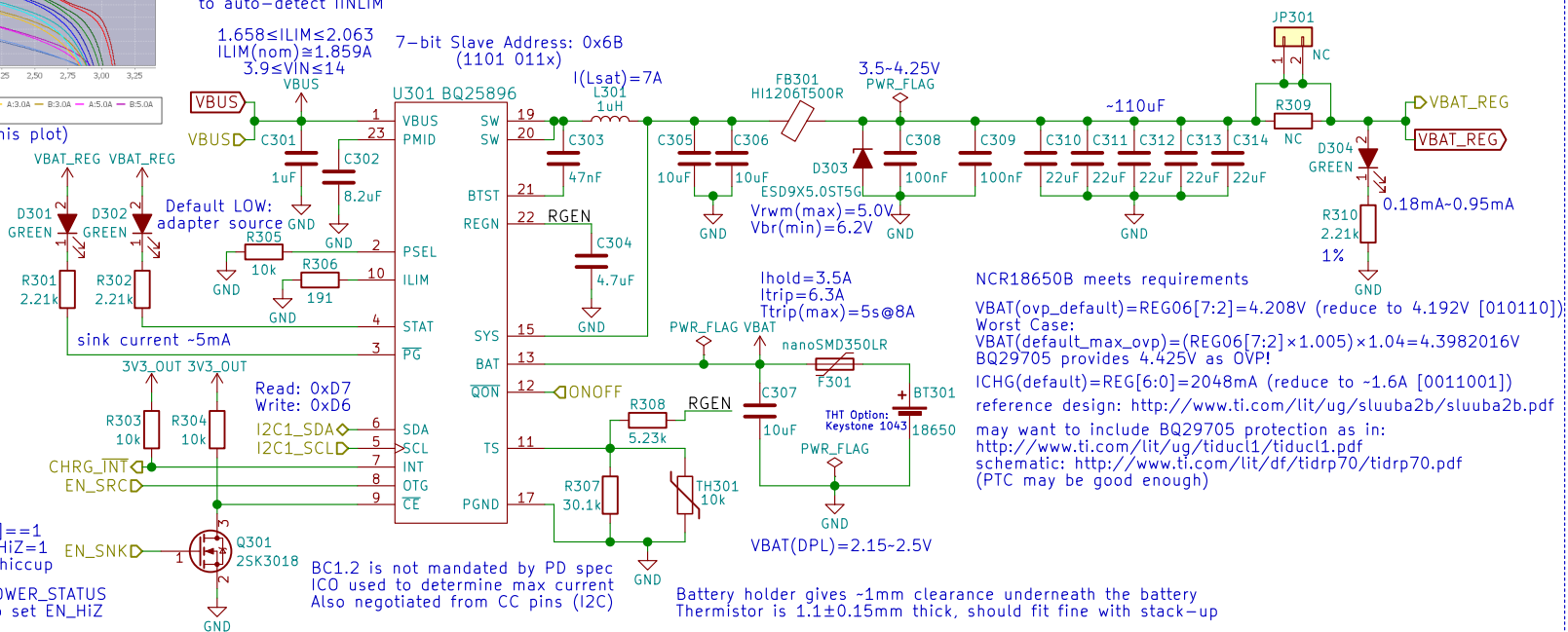
Drawing ~333.33mA, or consuming <1.2W, should give close to 10 hours going from 100% to 0% charge

use AUTO_DPDM_EN to auto-detect IINLIM

$1.658 \leq I_{LIM} \leq 2.063$
 $I_{LIM}(\text{nom}) \approx 1.859A$
 $3.9 \leq V_{IN} \leq 14$

7-bit Slave Address: 0x6B (1101 011x)

Battery Charge Controller



NCR18650B meets requirements

VBAT(ovp_default)=REG06[7:2]=4.208V (reduce to 4.192V [010110])
Worst Case:
VBAT(default_max_ovp)=(REG06[7:2]×1.005)×1.04=4.3982016V
BQ29705 provides 4.425V as OVP!
ICHG(default)=REG[6:0]=2048mA (reduce to ~1.6A [0011001])
reference design: <http://www.ti.com/lit/ug/sluuba2b/sluuba2b.pdf>
may want to include BQ29705 protection as in:
<http://www.ti.com/lit/ug/tiduc1/tiduc1.pdf>
schematic: <http://www.ti.com/lit/df/tidrp70/tidrp70.pdf>
(PTC may be good enough)

This disables charging but maybe not VBUS->VOUT if PTN5110HQ's FAULT_STATUS[6]=1 (Force Off VBUS bit) then set EN_HI_Z=1 EN_HI_Z may be auto-set when in hiccup

Reading PTN5110HQ's CC_STATUS and POWER_STATUS registers will tell TCPM (i.MX8M) when to set EN_HI_Z

Also, reading PTN5110HQ's CC_STATUS and POWER_STATUS registers will tell TCPM (i.MX8M) when to set OTG_CONFIG=1 (this will also happen when PTN5110HQ sets EN_SRC HIGH)

BC1.2 is not mandated by PD spec ICO used to determine max current Also negotiated from CC pins (I2C)

Battery holder gives ~1mm clearance underneath the battery Thermistor is 1.1±0.15mm thick, should fit fine with stack-up
Battery holder seems to fit up to ~68.88mm long batteries need to test 18650 protected cells which are ~69.35mm long

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Sheet: /Battery/

File: battery.sch

Title: Battery

Size: A4

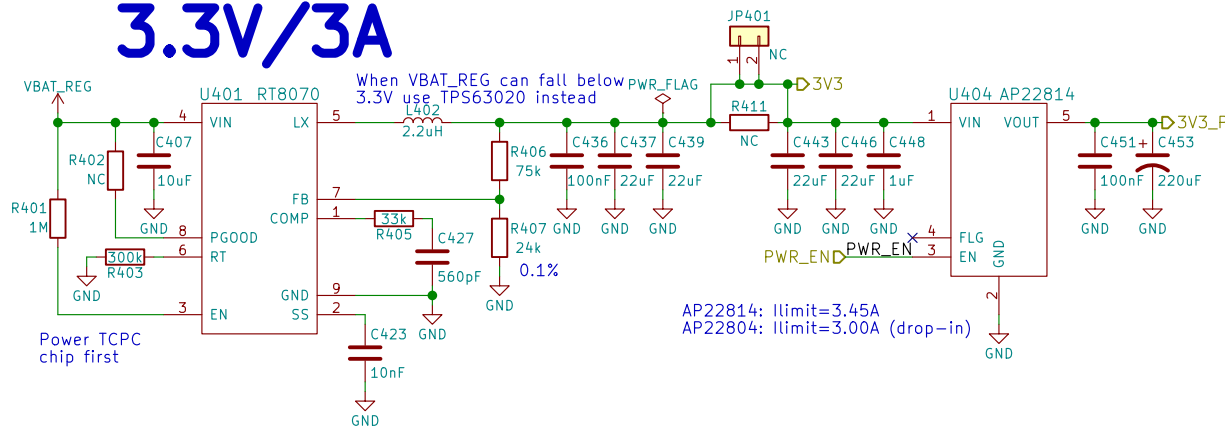
Date: 2018-06-07

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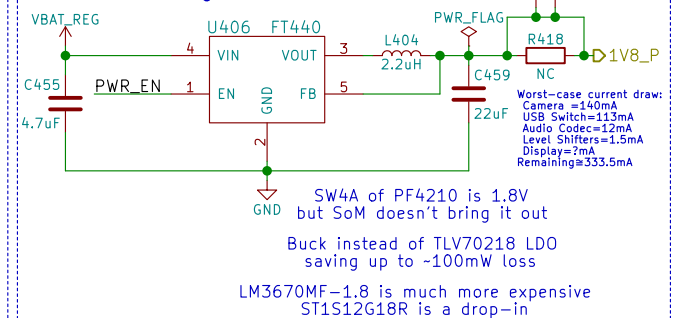
Rev: v0.1.0

Id: 3/24

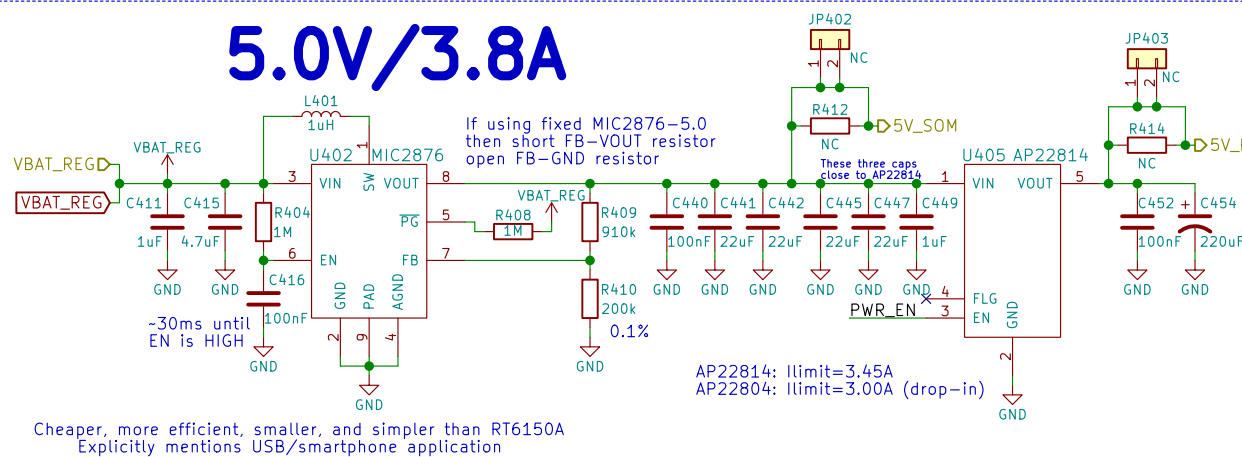
3.3V/3A



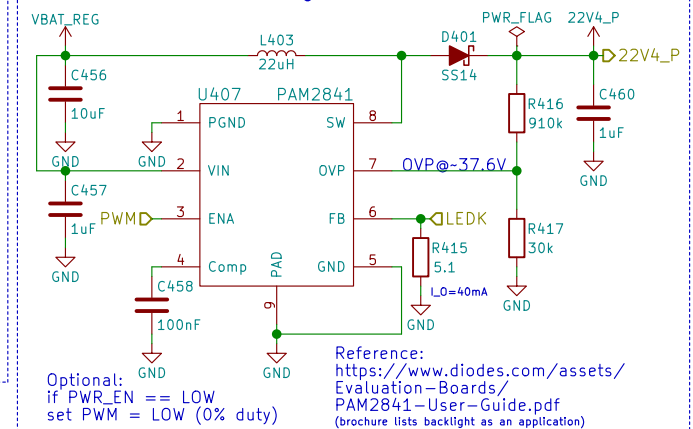
1.8V/600mA



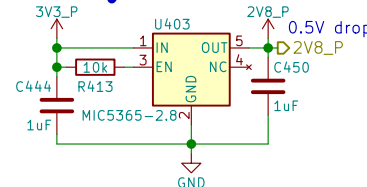
5.0V/3.8A



22.4V/40mA



2.8V/150mA



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Sheet: /Power/
File: power.sch

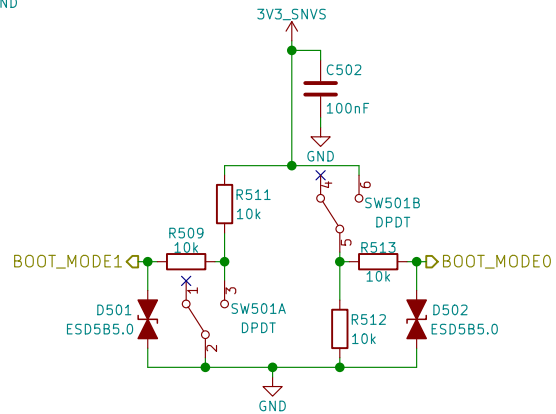
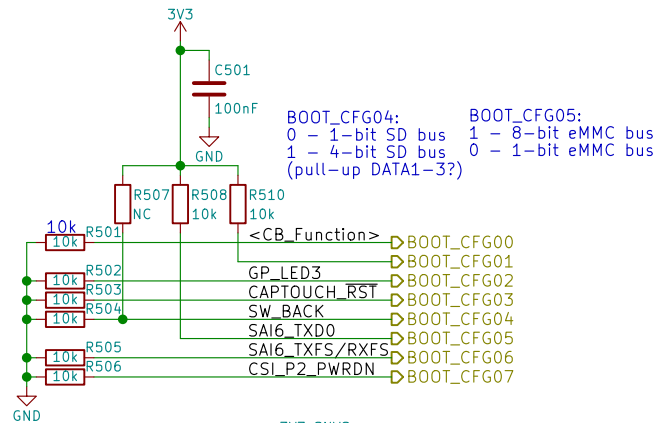
Title: Power

Size: A4
KiCad E.D.A. kicad 4.0.7

Date: 2018-06-07

Rev: v0.1.0

Id: 4/24

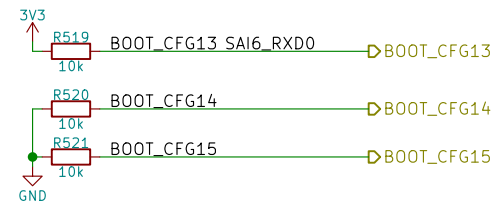
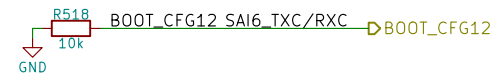
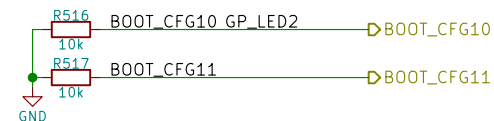
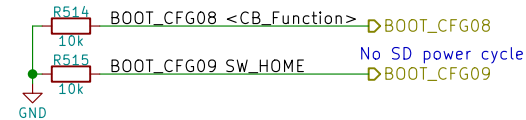


2->1: eMMC 2->3: USB (Serial Downloader)	
BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

Only eMMC

BOOT_CFG[14:12]		Boot device			
001		SD/eSD			
010		MMC/eMMC			
011		NAND			

Fuse	Config	Definition	GPIO ¹	Shipped value	Settings
BOOT_CFG[11:10]	OEM	USDHC port selection	Yes	00	00 - USDHC-1 01 - USDHC-2 10 - USDHC-3 else - reserved



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Sheet: /Boot Config/
 File: boot.sch

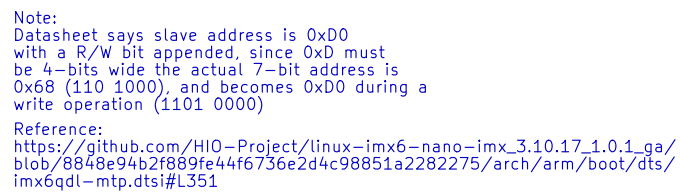
Title: Boot Configuration

Size: A4 Date: 2018-06-07

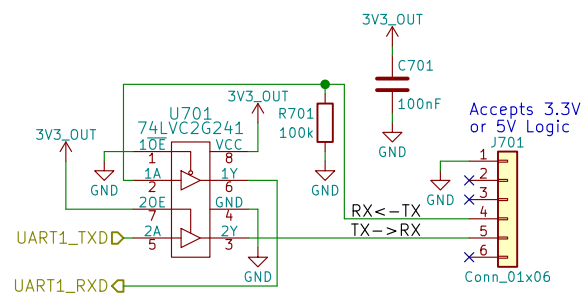
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Rev: v0.1.0

Id: 5/24



Id: 6/24



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Sheet: /UART Debug/
File: uart.sch

Title: UART Debug

Size: A4 Date: 2018-06-07

KiCad E.D.A. kicad 4.0.7

Rev: v0.1.0

Id: 7/24

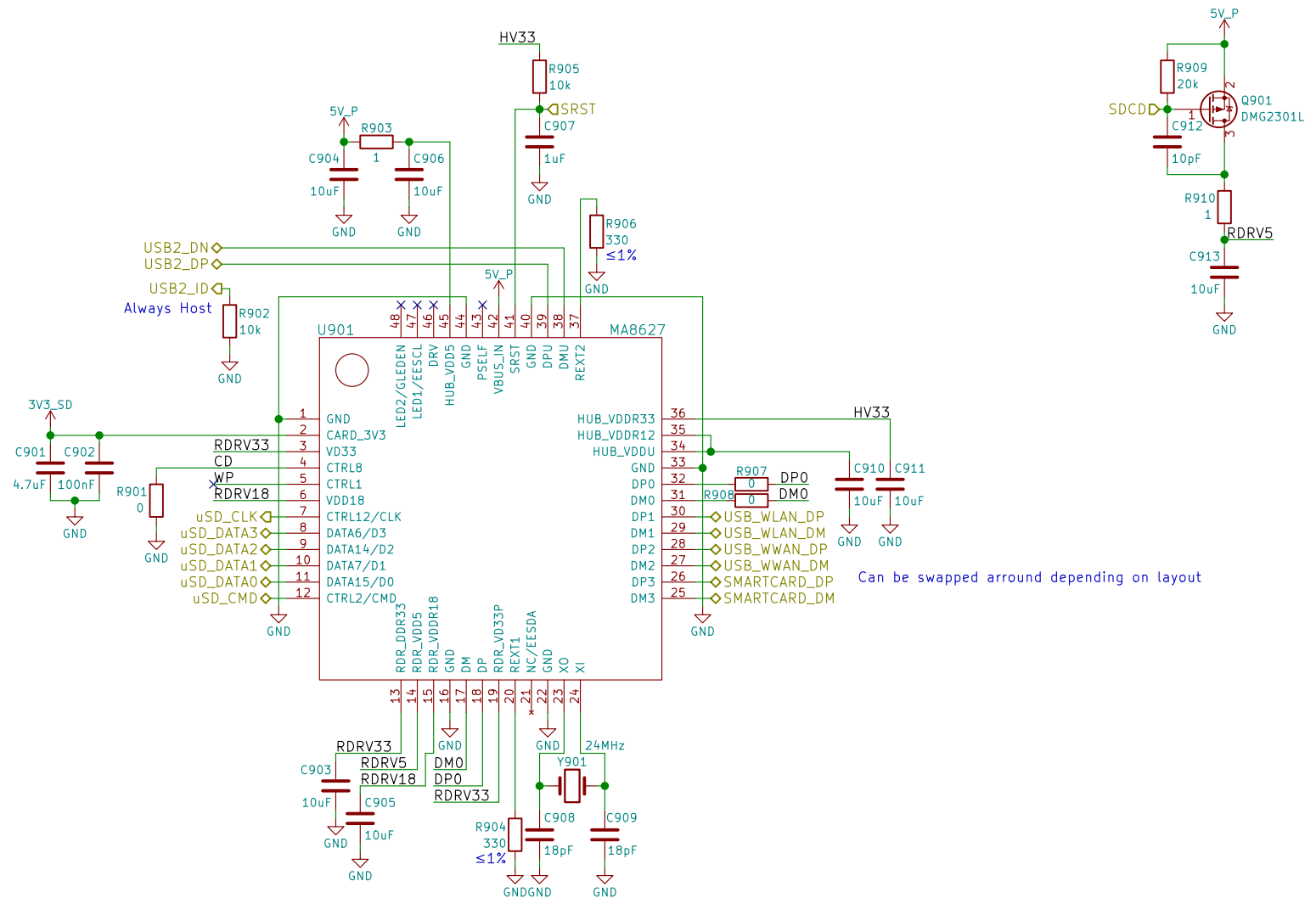


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Sheet: /JTAG/
File: jtag.sch

Title: JTAG

Size: A4 Date: 2018-06-07
KiCad E.D.A. kicad 4.0.7

Rev: v0.1.0
Id: 8/24



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Sheet: /USB Hub + SDIO Bridge/

File: usb_hub_sdio.sch

Title: USB Hub + SDIO Bridge

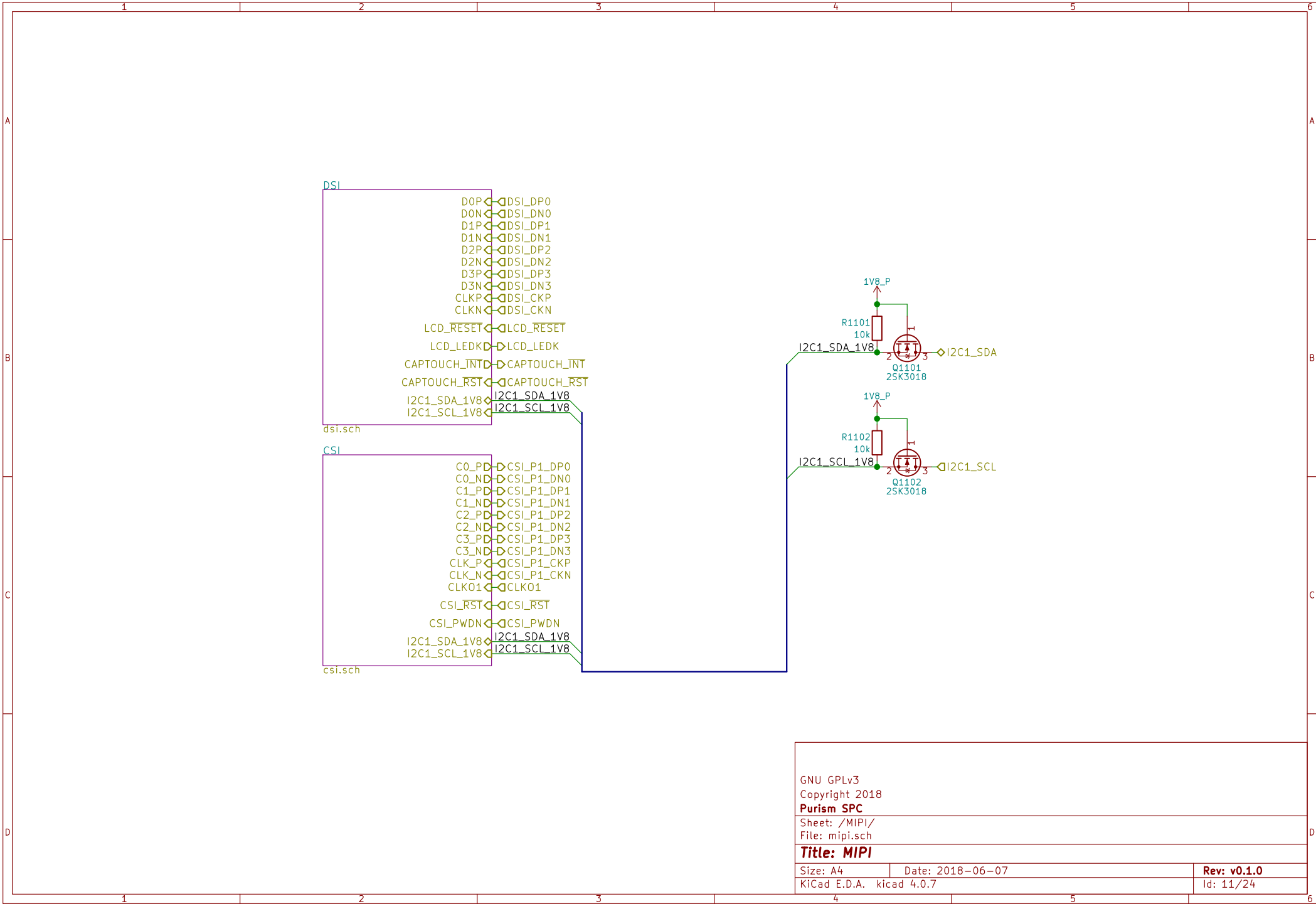
Size: A4 Date: 2018-06-07

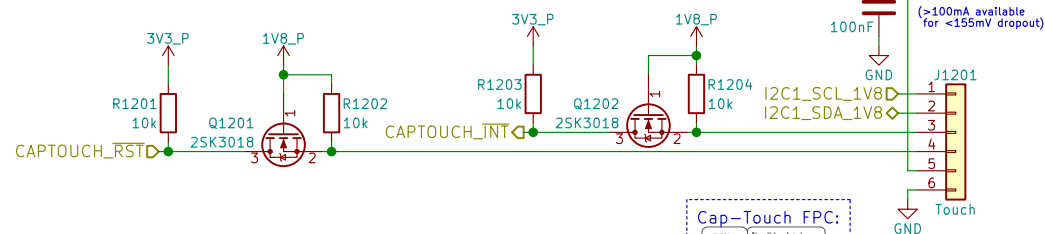
KiCad E.D.A. kicad 4.0.7

Rev: v0.1.0

Id: 9/24

Id: 10/24

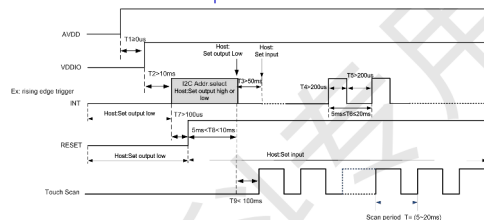




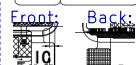
The upper 7 bits are the address, and bit 0 is used to select read or write. GT5688 has two slave device addresses to choose from:

INT	7-Bit Address	8-Bit Write Address	8-Bit Read Address
LOW	0x5D	0xBA	0xBB
HIGH	0x14	0x28	0x29

Every time you power on or reset, you need to use the INT pin to set the I2C address:

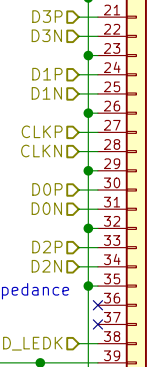
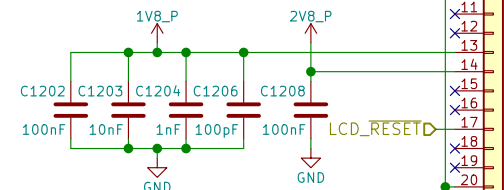


Pin#	Definition
1	SCL
2	SDA
3	INT
4	RESET
5	VDD2_R5
6	GND

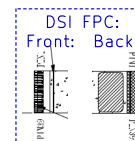
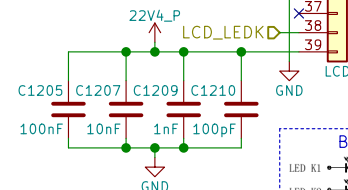


LCD PN:
Shenzhen Jinghong Electronics Co., Ltd.
JH057N00900

Note:
No power-up sequence is given in the spec sheet



100Ω Differential Impedance



Backlight Array:



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Sheet: /MIPI/DSI/
File: dsi.sch

Title: MIPI DSI

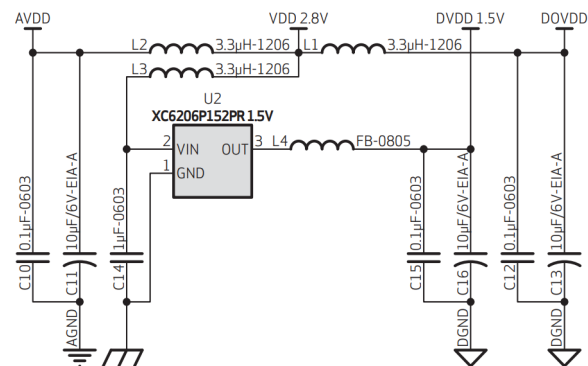
Size: A4 Date: 2018-06-07

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Rev: v0.1.0

Id: 12/24

Using Internal DVDD 1.5V Regulator:



2.7 POWER UP SEQUENCE

Based on the system power configuration (1.8V or 2.8V for I/O power, using external DVDD or internal DVDD, requiring access to the I2C during power up period or not), the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred. If 2.8V is used for I/O power, due to a high voltage drop at the internal DVDD regulator, there is a potential heat issue. Hence, for a 2.8V power system, OmniVision recommends using an external DVDD source. Due to the higher power down current when using an external DVDD source, OmniVision strongly recommends cutting off all powers, including the external DVDD, when the sensor is not in use in the case of 2.8V I/O and external DVDD.

2.7.1 POWER UP WITH INTERNAL DVDD

For powering up with the internal DVDD and I2C access during the power ON period, the following conditions must occur:

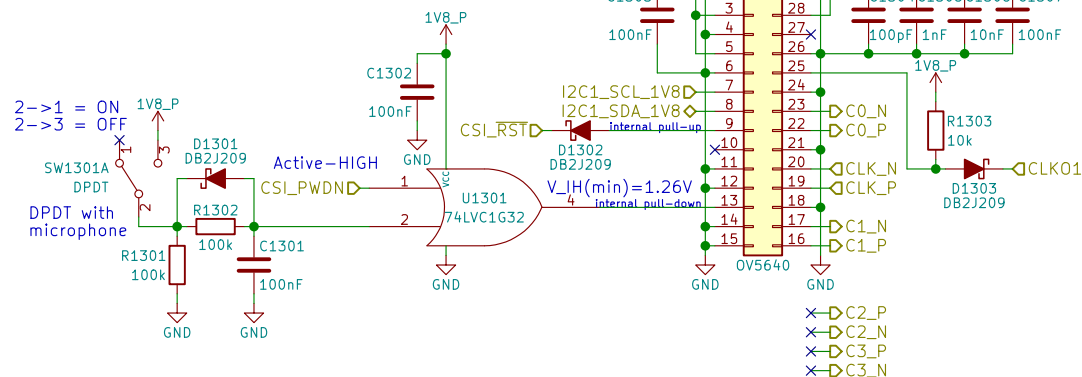
1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. PWDN is active high with an asynchronized design (does not need clock)
3. PWDN pin tied to digital ground if it is not controlled.
4. if PWDN pin is controlled as below, for PWDN to go low, power must first become stable (AVDD to PWDN ≥ 5 ms)
5. RESETB is active low with an asynchronized design
6. master clock XVCLK should provide at least 1 ms before host accesses the sensor's registers
7. host can access I2C bus (if shared) during entire period. 20ms after RESETB goes high, host can access the sensor's registers to initialize sensor

figure 2-3 power up timing with internal DVDD



note $t_0 \geq 0$ ms, delay from DOVDD stable to AVDD stable, it is recommended to power up AVDD shortly after DOVDD has been powered up
 $t_1 \geq 0$ ms, delay from XVCLK off to AVDD off
 $t_2 \geq 5$ ms, delay from AVDD stable to sensor power up stable, PWDN can be pulled low after this point, XVCLK can be turned on after power on
 $t_3 \geq 1$ ms, delay from sensor power up stable to RESETB pull up
 $t_4 \geq 20$ ms, delay from RESETB pull high to SCCB initialization
 $t_5 \geq 0$ ms, delay from AVDD off to DOVDD off
 $t_6 \geq 0$ ms, delay from RESETB pull low to AVDD off

5640_05_2-2



Camera PN:
 Truly C08725-B5SA-E
 7-bit Slave Address: 0x78
 (1111 000x)
 Read: 0xF1
 Write 0xF0

OV5640 CMOS Image Sensor Datasheet:
https://cdn.sparkfun.com/datasheets/Sensors/LightImaging/OV5640_datasheet.pdf

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Sheet: /MIPI/CSI/
 File: csi.sch

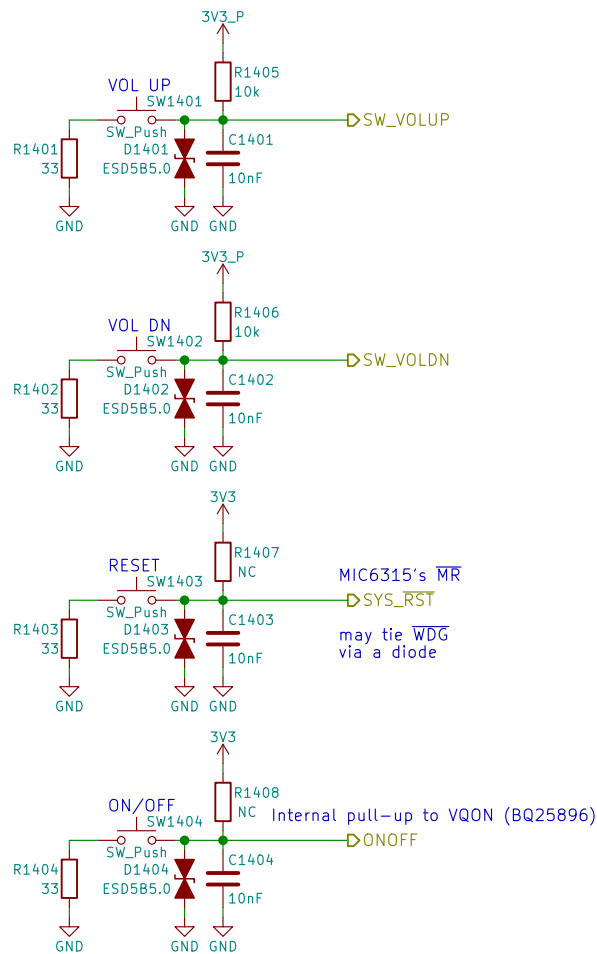
Title: MIPI CSI

Size: A4 Date: 2018-06-07

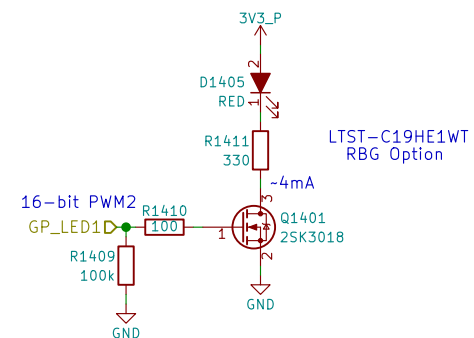
KiCad E.D.A. kicad 4.0.7

Rev: v0.1.0

Id: 13/24



Use PWM2_PWMSAR to set the compare value (duty cycle)
 Use PWM2_PWMCR[15:4] to set the PRESCALER (frequency)
 Use PWM2_PWMPR to set the top of the counter (frequency)



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Sheet: /Buttons & LED/
 File: buttons_led.sch

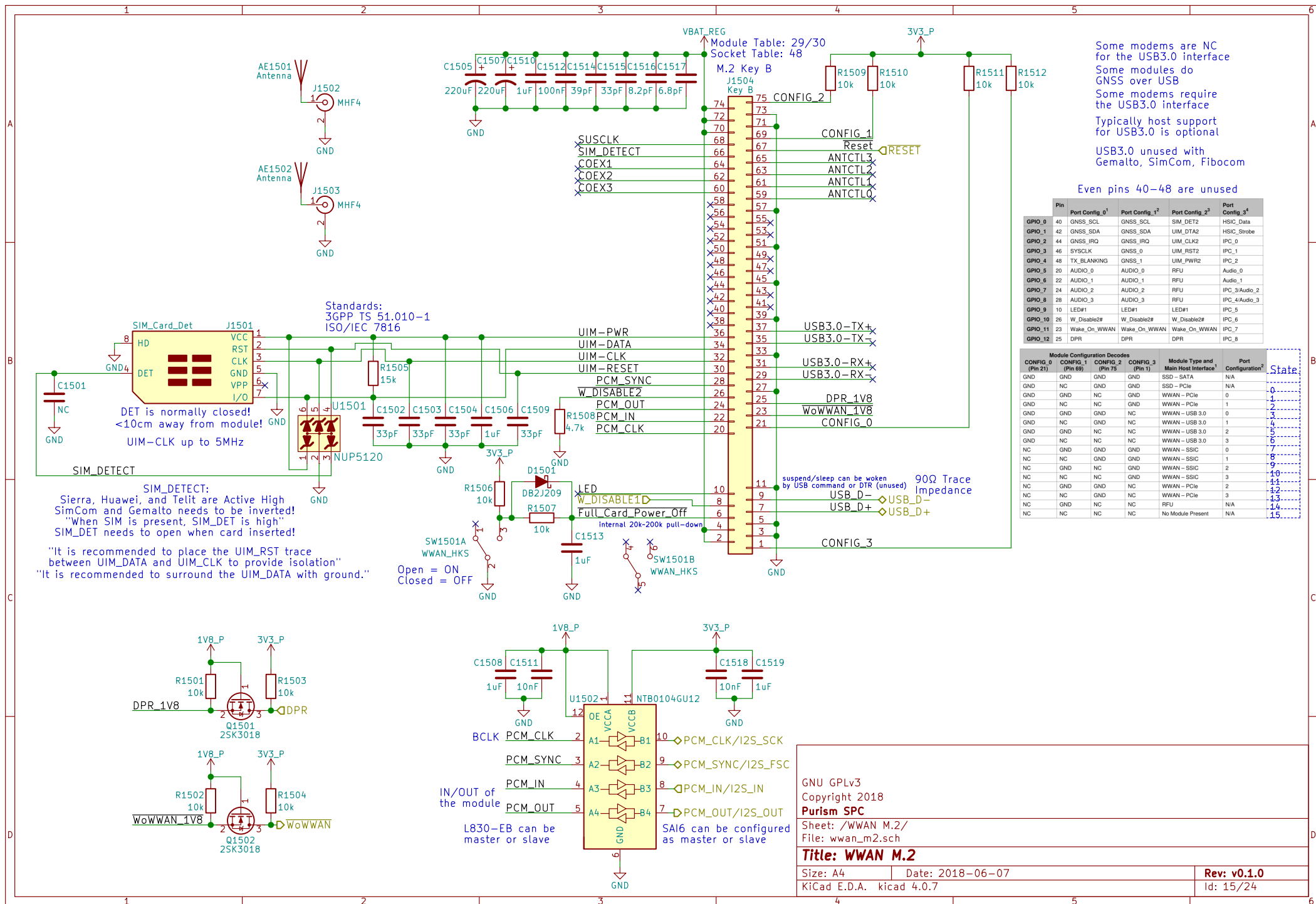
Title: Buttons & LED

Size: A4 Date: 2018-06-07

KiCad E.D.A. kicad 4.0.7

Rev: v0.1.0

Id: 14/24



Some modems are NC for the USB3.0 interface
Some modules do GNSS over USB
Some modems require the USB3.0 interface
Typically host support for USB3.0 is optional
USB3.0 unused with Gemalto, SimCom, Fibocom

Even pins 40-48 are unused

Pin	Port Config_0 ¹	Port Config_1 ²	Port Config_2 ³	Port Config_3 ⁴
GPIO_0	40	GNSS_SCL	GNSS_SCL	SIM_DET2
GPIO_1	42	GNSS_SDA	GNSS_SDA	UIM_DTA2
GPIO_2	44	GNSS_IRQ	GNSS_IRQ	UIM_CLK2
GPIO_3	46	SYSClk	GNSS_0	UIM_RST2
GPIO_4	48	TX_BLANKING	GNSS_1	UIM_PWR2
GPIO_5	20	AUDIO_0	AUDIO_0	RFU
GPIO_6	22	AUDIO_1	AUDIO_1	RFU
GPIO_7	24	AUDIO_2	AUDIO_2	RFU
GPIO_8	28	AUDIO_3	AUDIO_3	RFU
GPIO_9	10	LED#1	LED#1	LED#1
GPIO_10	26	W_Disable2#	W_Disable2#	W_Disable2#
GPIO_11	23	Wake_On_WWAN	Wake_On_WWAN	Wake_On_WWAN
GPIO_12	25	DPR	DPR	DPR

Module Configuration Decodes				Module Type and Main Host Interface ¹	Port Configuration ²
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
GND	GND	GND	GND	SSD - SATA	N/A
GND	NC	GND	GND	SSD - PCIe	N/A
GND	GND	NC	GND	WWAN - PCIe	0
GND	NC	NC	GND	WWAN - PCIe	1
GND	GND	GND	NC	WWAN - USB 3.0	2
GND	NC	GND	NC	WWAN - USB 3.0	3
GND	GND	NC	NC	WWAN - USB 3.0	4
GND	NC	NC	NC	WWAN - USB 3.0	5
NC	NC	GND	GND	WWAN - SSIC	6
NC	GND	NC	GND	WWAN - SSIC	7
NC	NC	NC	GND	WWAN - SSIC	8
NC	GND	NC	GND	WWAN - SSIC	9
NC	NC	NC	GND	WWAN - SSIC	10
NC	GND	GND	NC	WWAN - PCIe	2
NC	NC	GND	NC	WWAN - PCIe	11
NC	GND	NC	NC	RFU	12
NC	NC	NC	NC	No Module Present	13
NC	NC	NC	NC	No Module Present	14

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Purism SPC
Sheet: /WWAN M.2/
File: wwan_m2.sch
Title: WWAN M.2
Size: A4 Date: 2018-06-07
KiCad E.D.A. kicad 4.0.7
Rev: v0.1.0
Id: 15/24

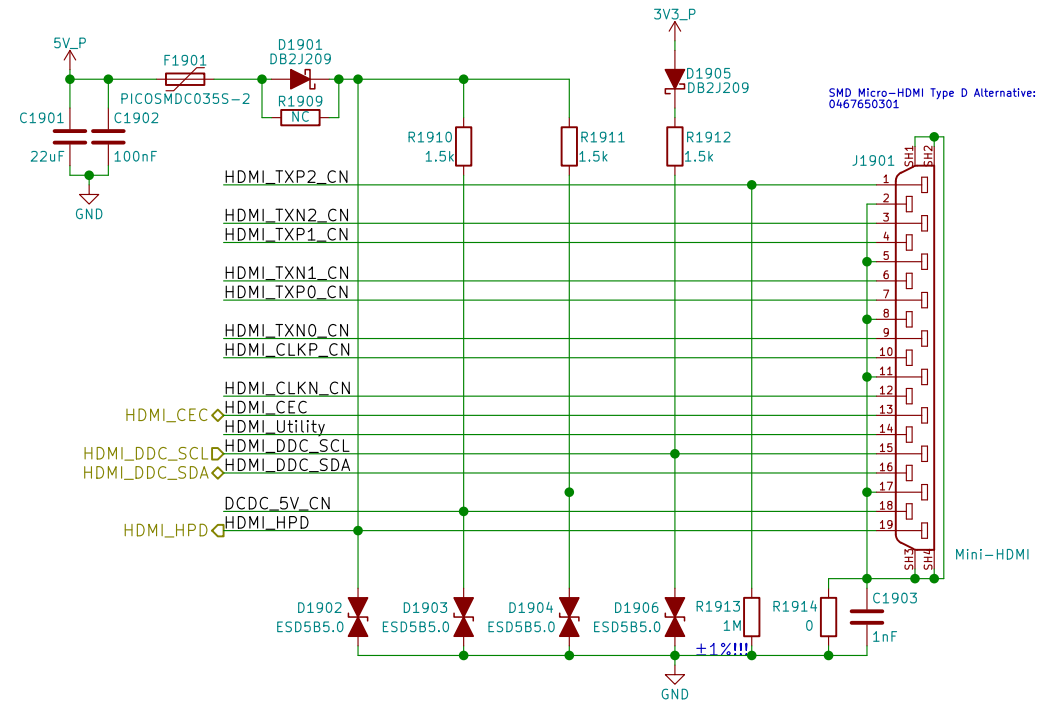
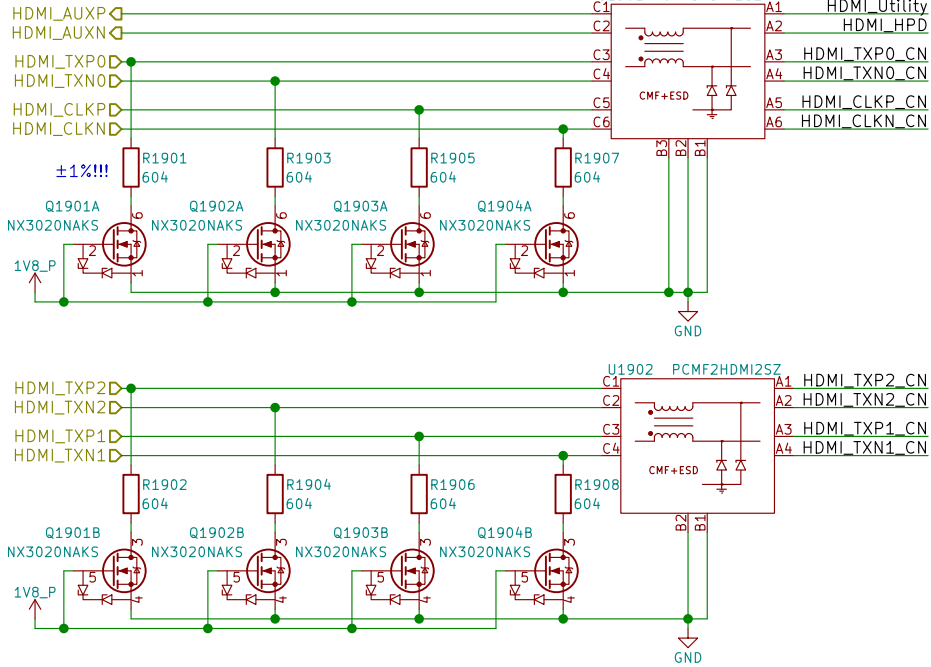
[illegible]

Id: 17/24

HD3SS460 can be used for DP over USB-C

Layout Note:
May need swap some signals
due to micro-HDMI pinout diff
depending on pin location/routing

100Ω diff pairs



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Sheet: /HDMI/
File: hdmi.sch

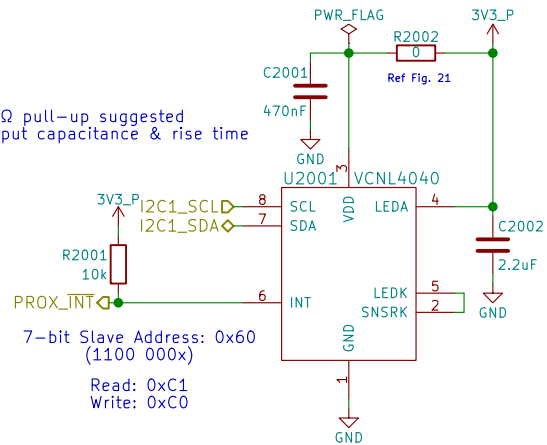
Title: HDMI

Size: A4 Date: 2018-06-07
KiCad E.D.A. kicad 4.0.7

Rev: v0.1.0
Id: 19/24

Proximity & Ambient Light

Note:
I2C 2.2kΩ pull-up suggested
check input capacitance & rise time



Reference:
<https://www.vishay.com/docs/84307/designingvcnl4040.pdf>
<http://www.vishay.com/docs/84931/vcnl4040sensorboardfiles.pdf>

9-Axis IMU

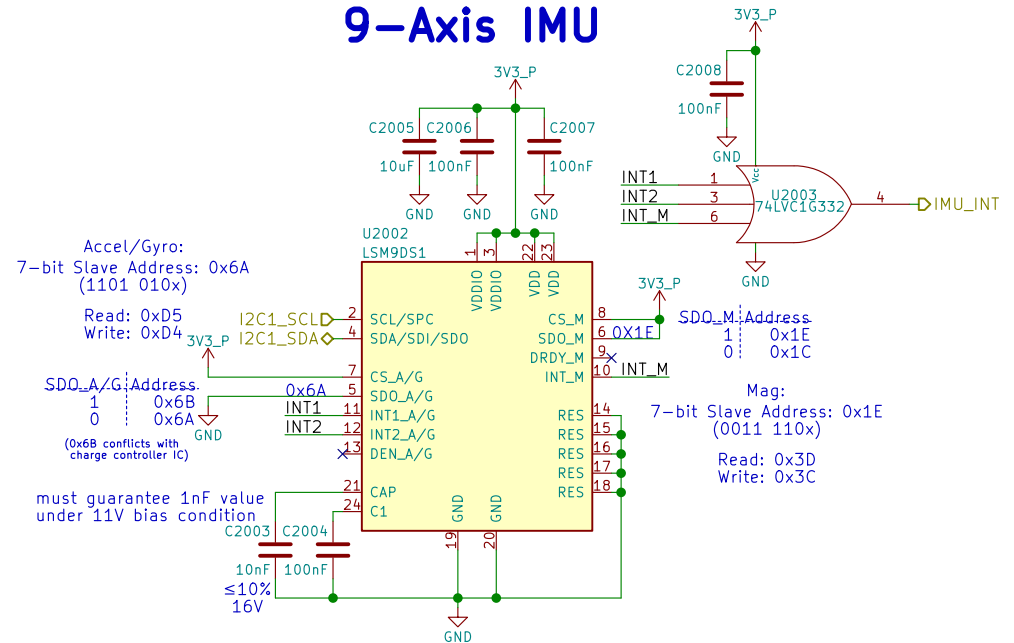


Table 19. Accelerometer and gyroscope SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 20. Magnetic sensor SAD+Read/Write patterns

Command	SAD[6:2]	SAD[1] = SDO/SA1	SAD[0]	R/W	SAD+R/W
Read	00111	0	0	1	00111001 (39h)
Write	00111	0	0	0	00111000 (38h)
Read	00111	1	0	1	00111101 (3Dh)
Write	00111	1	0	0	00111100 (3Ch)

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Sheet: /Sensors/

File: sensors.sch

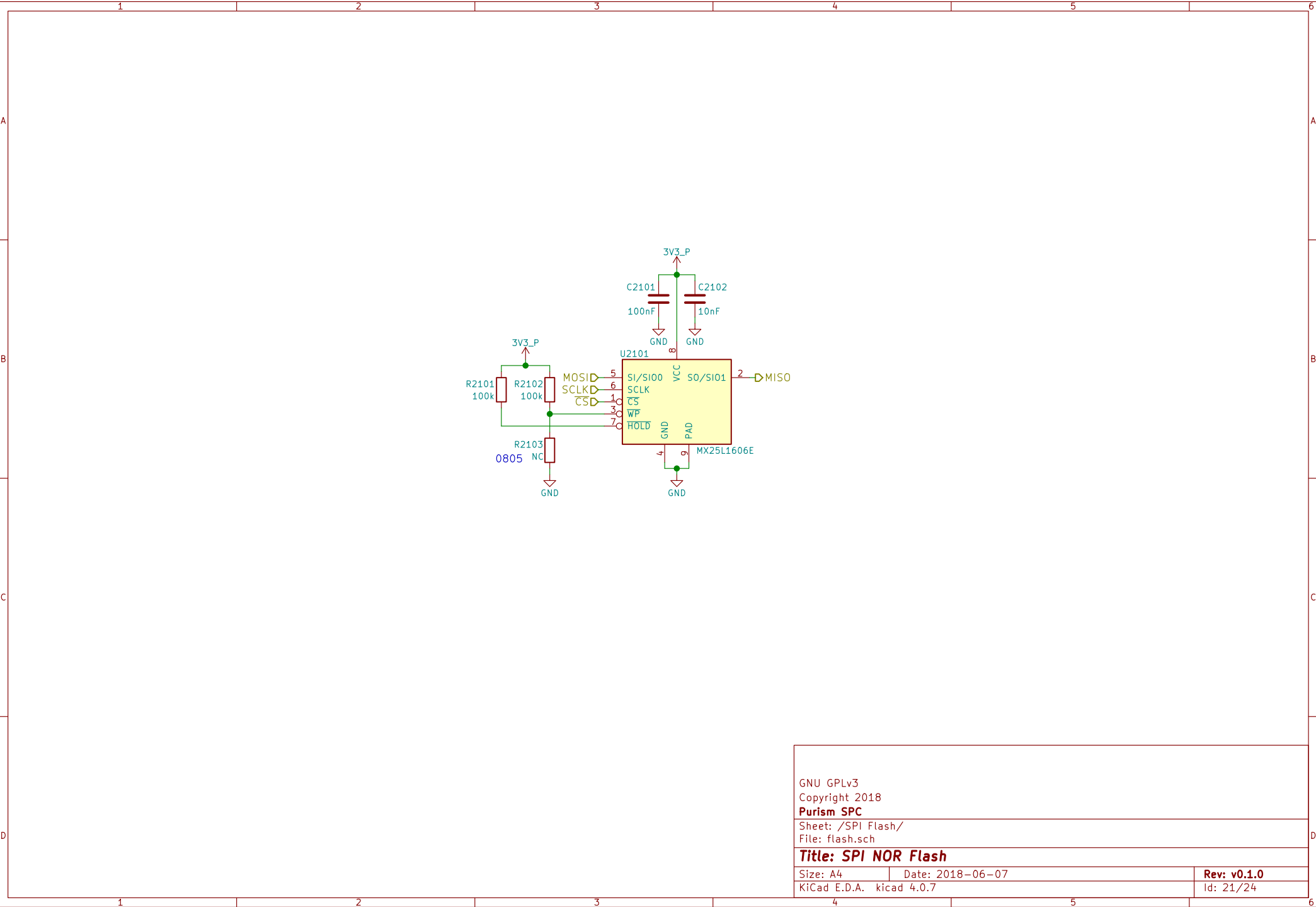
Title: Sensors

Size: A4 Date: 2018-06-07

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Rev: v0.1.0

Id: 20/24



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Sheet: /SPI Flash/

File: flash.sch

Title: SPI NOR Flash

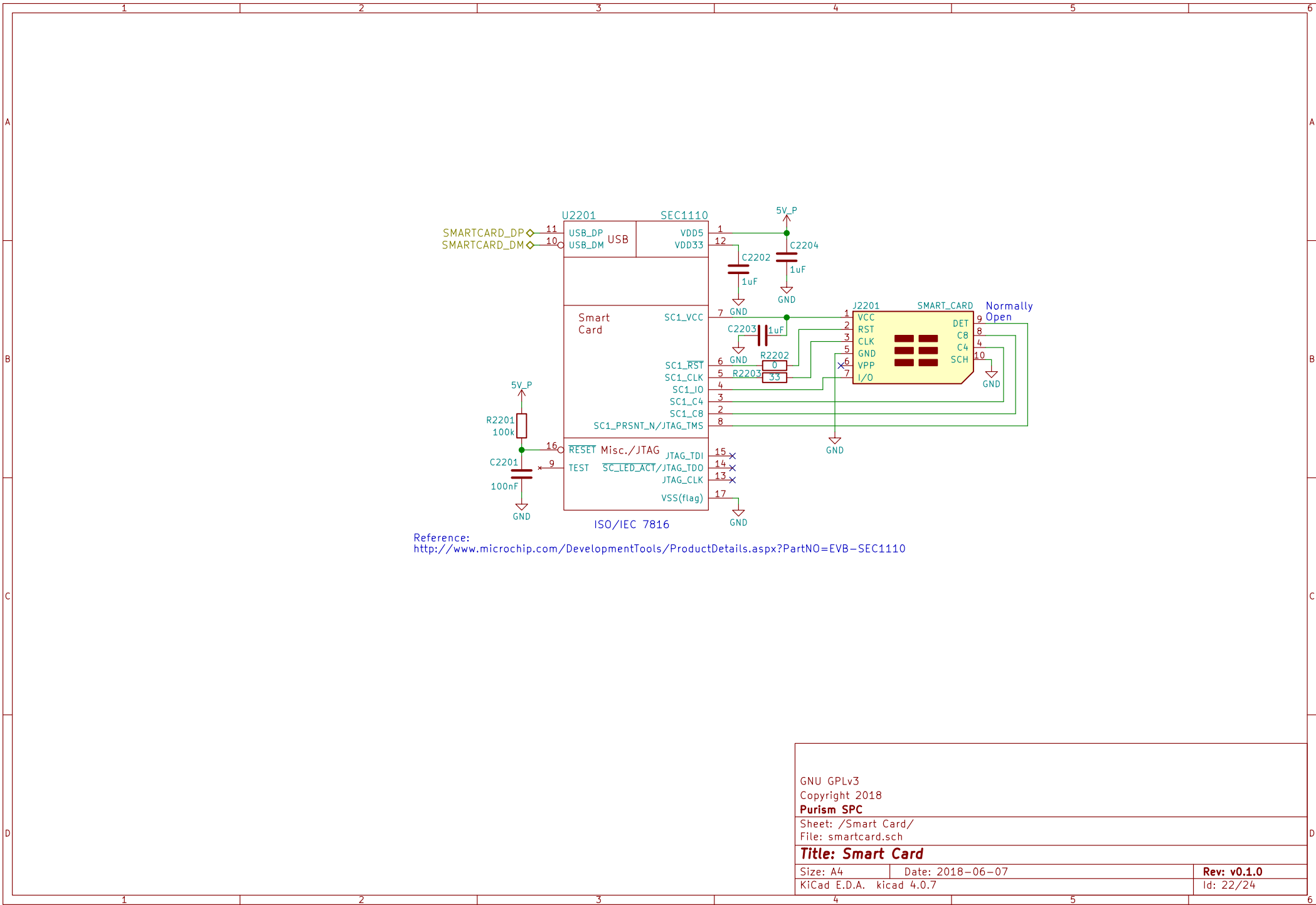
Size: A4

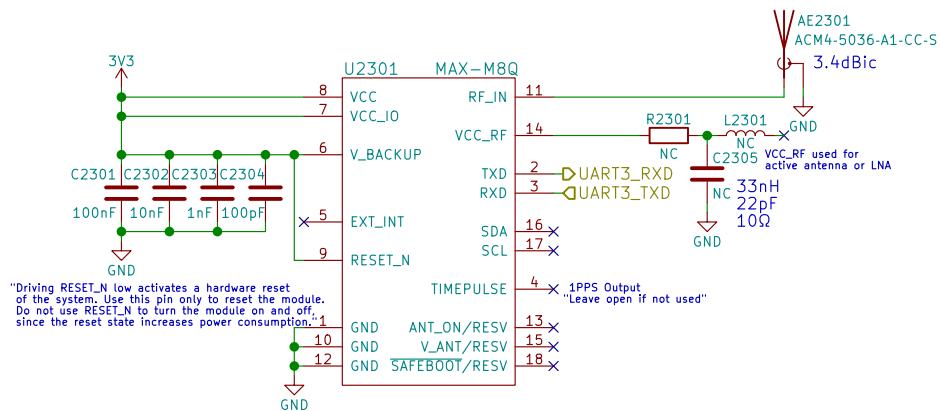
Date: 2018-06-07

Rev: v0.1.0

KiCad E.D.A. kicad 4.0.7

Id: 21/24





Reference:
https://www.u-blox.com/sites/default/files/MAX-8-M8-FW3_HardwareIntegrationManual_1503005929.pdf

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Purism SPC

Sheet: /GNSS/
 File: gnss.sch

Title: GNSS

Size: A4 Date: 2018-06-07

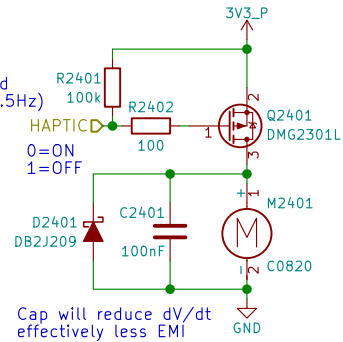
KiCad E.D.A. kicad 4.0.7

Rev: v0.1.0

Id: 23/24

PWM pins occupied:
 GPIO1_I001 - LCD Backlight
 GPIO1_I013 - LED
 GPIO1_I014 - Ethernet (CLKO_25MHz)
 GPIO1_I015 - CSI (CLKO2)

PWM needed?
 Only needs to be toggled
 ON 1 sec, OFF 1 sec (0.5Hz)
 Can MUX as either
 GPIO or PWM2
 swapping with LED



When the motor is off
 both terminals are at GND

Motor will have wire leads
 with a 2-pin Molex or Boom Precision
 connector installed (by request)!

Cap will reduce dV/dt
 effectively less EMI

Cheaper Motor Connector:
https://lcsc.com/product-detail/1-25T-Connectors_1-25T-1-2AW_C10832.html

Motor Source:
https://www.alibaba.com/product-detail/Coin-motor-vibration-dc-motor-cellphone_1994583657.html?spm=a2700.8443308.0.0.5aa13e5f1wxHgs
 Motor Datasheet:
<https://cloud.puri.sm/s/z8JR6DJ4KrJYzoW>

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Purism SPC

Sheet: /Haptic Motor/
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