V06 1, Del NFC PN7150, Add CON24, UART1 for GNSS or Debug, SPI2 to CON24, UART2 for BT 2, Move SMC_BOOT0 to Page 22, TP6. 3, HKs Add Pull-up Resistor, And add Read state GPIO. 4, TYPE-C U27 LSX no connect. 5. Correct Y2. Y3 Connect. 6, Add Voltage Test Point, >40 point 7, Add SIM DET D6. 8, CAMERA Modify. Add LDO for DVDD 1.2 and 1.05. 9, TFT con Modify. 10, STM32 PA10 NC. UART add Pull-up R108, R135 1, UART1 to LSX, UART2 to GNSS, UART4 to bt, SPI1 to CON24 2, U329 19PIN add Pull-up R229 . V08 1. UART2 to LSX 2, HW state IO add resister. R48, R66, R145 3, 4G, WIFI ant CON add Debug L,C 4, Add shielding Case Hold. 5, DEL F12, Modified IO U329 for L9 layer to GND. 6, INT_M/A/G, NFC_EN, NFC_IRQ modified IO to E1 for L2 to GND 7, ADD R232 V09 1, AUX_P, AUX_N swapped. 2, Add R236. 3, Del R153 4, LED_G to 8M D3 pin. NFC_IRQ to 8M E1 pin, INT_M/A/G to 8M L4 pin. 5, R122,R58 to 27K, R123 to 47K. 6, 4G used SAI6. ADD u5 V091 1, U5 8pin to SAI1 TXD5, 9pin to SAI1 RXD5. 2, ADD U7 for CAM_AFVDD, 2.8V 120mA. 3. U2 modified USB2642 V092 1, BOOT Resistor Modified. 2. EMMC 32G. 4, PWM IO modify. MOTO E6, PMIC_5V T7, LED_B K6. V093 1, R830 NC, R811 10k. V094 1, BAT CON Modified for 1000 times. 2, ADD L66 L67 V095 1, R115 Modified to 200. V096 1, ADD R153 for TPS65983B Slave. 2, Modified LM36922 to I2C3, J10 to I2C4. V097 0, CHG_STATUS_B connect Red LED. 1, Add N-mosfet Q8 on SD2_NCD. 2, TPS65982 LDO_1V8D Connected BUSPOWERZ. 3, VDD_3V3 add 4x22uf C231.... 4, VSYS_3V4_4V3 add 7x22uf C281.... 5, U27 TPS65982 F2 UART_RX 100k R223 connect GND. 6, Add NET BT_WAKE 7, AUDIO_POWER_KEY connect Q2 PIN1. 8, ADD U68 NTSX2102 9, BOOT_CFG PU to NVCC_SNVS_3V3 10, R176 PU to NVCC_SNVS_3V3 11. R104 10 value. 12, R82 0402 0.1% 13 R934 100K 14, U2 USB2642 27,28 connect GND, 26 connect VDD. 15, ADD Q9, Modified WIFI_REG_ON, BT_REG_ON. 16, ADD R238 UART2_RXD PU USB_PD_LDO3V3 17, ADD Q10, R239, R240,R241 18, Add TYPEC_HRESET, 19, R42 1M, 20, U147 connect TPS65982 21, SW3,SW5,SW7 2-3PIN 22, J50 modified 23, J12 modifed

1, 0 ohm jumpers SPI.
2, C181 NC
3,main board usb 2.0 connector
4,PFET pull up UART2_RX
5,red LED powered by VSYS
6, TPS65982 IZC2 10K pull-ups 7, TPS65982 remove_usb 2.0
8, TP34 connect USB_VBUS for test
9, SPI MISO ADD pull-up 10K
10, ADD u50,U51 , C335,C336
V099
(11) Battery connector (J20): changed to P / N: BA32-111203-01 3pin
(12) Cancel J50 (flash holder) and move the flash to the rear camera FPC
(13) change J22 to P / N: OK-06F034-04
(14) J9 smartcard (80500122) is changed to SA070112150-105
(15) Headphone socket (J2) changed to JA-36A1-111
(16)
(17) SIM +TF Card changed to SA2101110135-103-01, TF_NCD and 4G_ SIM_ CD two port exchange (Change to plastic tray)
(18) R166, R109 changed to 0R
(19) Connect SMC_ Boot0 to D7 pin of imx8mq
(20) R41(47K) changed to 0R
(21) ADD CLOCK Crystal(Y1)VALUE:32.768K 10pF +/-20ppm
(22) Use TLV75801PDBVR instead of LCDL015MR for U21 and U37
Make R33=11.8k
Make R70=9.09k
Remove R234 (0)
(23) add a test point to pin C2 of the TPS65982 (U27's GPIO1_CFG0)
(24) add inverter (Q12)
(25) ADD C339 (26) ADD C351/352/356/388/396/397/398/399/400/406/407/408/409/410/411/412/413/414/415/416/417//418/
419/420/421/422/423/424/427/4287/429/430/431/432/433 1UF 6.3V 0201
(27) C434 C435 NC
(28) ADD C436/437/439/440/441/442/443/444 0201/1UF ADD: C448 C449 C450 22UF 0603 6.3V
(29) R209 R210 changed to 1.5K
(30) DEL R1903
(31) ADD: LNA BGA725L6 & SAW filter B39162B4327P810. etc
(32)Bring USB_PD_LDC3V3 to pin 23 of J12 on the main board:
(33)Remove TVS11, TVS30, TVS31, and TVS32 on the main board:
(34) C343/C377 changed to 220PF
(35)change the connection of PMIC(U1) Pin49
(36) Change U101 MIPI_ VDDHA3 connection
(37) R63/R64/R100/R103 NC. (38) C379 and C380 = 100nF (0.1uF) (39) ADD R25/R252 1M
(40) ADD:Y2 (32.768K)/C332/C333(6.8Pf)
(41) ADD:R253/NC
(42) ADD R254/0 OHM
(43) Add connection between J4's pin12 and U101's G6
(44) add R255/0 ohm
(45) C87/C256 changed to 56pF (46) ADD C451/C454 56pF
(40) ADD C4311C434 30pp:
V1.02 & V1.03
Q12 CHANGE TO ISS138PW RS CHANGE TO IOR
3. D10 change to PTVS16VS1UR (USB Board)

5. DEL R180, R184 6. ADD L9 7. ADD D25(NSR20F30NXT5G); The connection network of R2 and R3 is changed to nvcc_ SNVS_ 3V3 9. The 33 and 34pin of PMIC increase 0 ohm resistance (R259/R260) 10. D6 changed to 0 ohm resistor (R261) 11. R55 and R218 connect to VDD 1V8 13. J22pin of U101 is connected to TF_ NCD 14. C736 Change to 22uF 16. 312 PIN define have changed. 17. The value of R118,R126 change to 18R, the value of R132 change to 100R

V098

(26)

1. Schematic of V2.0 mainboard is not add new part, only changed net and define of 33 8J12 . USB_board is add U1,U3,U4,U5,R5,R6,R7,R8,R9,R10,R11,R12,R13,R14,C6,C7,C8,C9,C10,C11,C12,C13,C18,C19,C23,C24

3. USB_board is add CON4,CON5, CON9; delete fuse F1

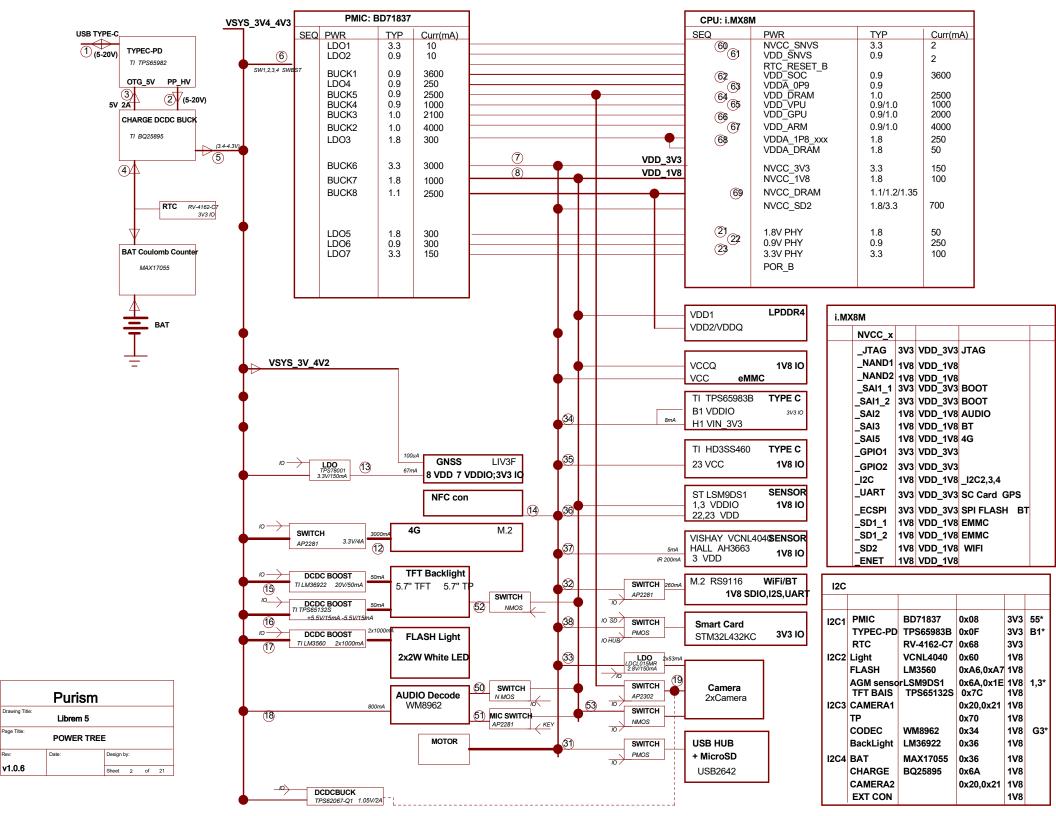
Changed define of J11 (USB_board)

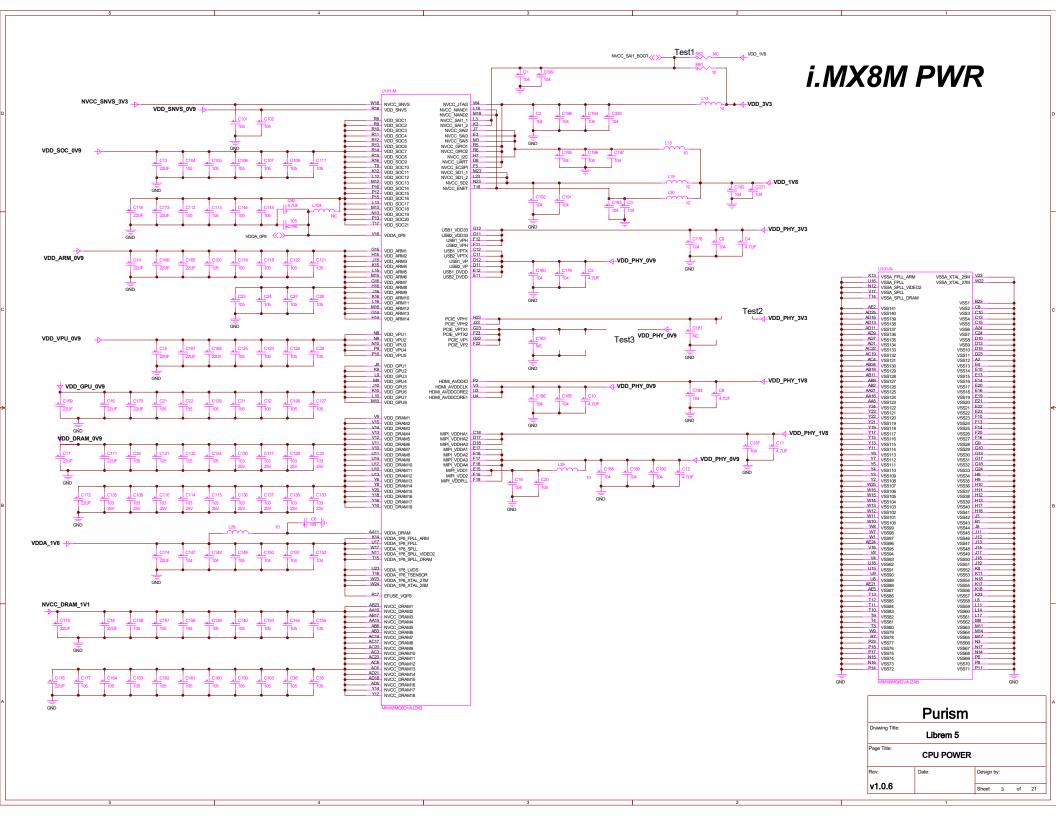
6. Mainboard: Add T1.T2

7. USB-C Board: DEL U5,R12,R13,R14,C20,C23,C24,L1,C2





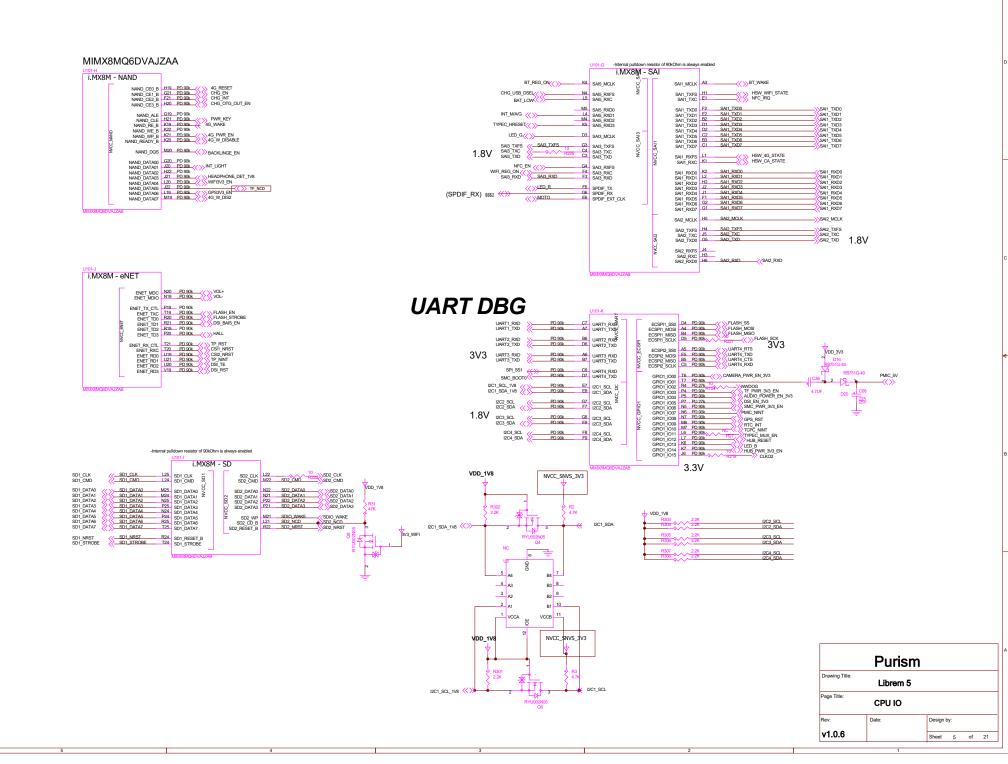




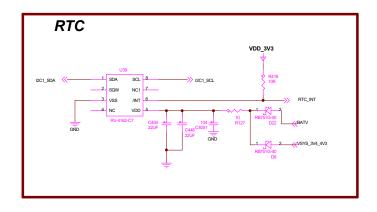
i.MX8M - DDR DMIO_A C3 __DRAM_DMIO_A AD17. AB16. DRAM ACORICAO A/A12/A12 / BTC AD20. DRAM ACORICA A/A11/A11 AD20. DRAM AC10/CA A/A7/A7 AE20. DRAM AC11/CAS A/A8/A8 AD19. DRAM AC12/CA4 A/A6/A6 DRAM AC13/CA5 A/A5/A5 DQ0_A B2 DQ1_A C2 DQ2_A E2 DQ3_A E2 DQ4_A E4 DQ5_A E4 DQ6_A C4 DQ7_A B4 DRAM DATAO A DRAM CAD A DRAM_CA1_A DRAM_CA2_A DRAM DATA1 A H4 CS0_A H3 CS1_A K5 NC_K5 DRAM DATA2 A (LPDDR4/DDR4/DDR3) DRAM CA3 A DRAM_DATA3_A DRAM_DATA4_A DRAM_DATA5_A J4 CKE0_A J5 CKE1_A K8 NC_K8 DRAM_NCS0_A AE18 DRAM_AC02/CS0_A/CS0_N/CS0 DRAM_NCS1_A AC18 DRAM_AC03/CS1_A/C0/ DQS0_T_A D3 __DRAM_SDQS0_T_A DQS0_C_A E3 __DRAM_SDQS0_C_A DRAM_CKE0_A DRAM_CKE1_A AC16 DRAM_AC00/CKE0_A/CKE0/CKE0 AE17 DRAM_AC01/CKE1_A/CKE1/CKE1 NVCC_DRAM_1V1 DRAM_CK_T_A DRAM_CK_C_A DMI1_A C10 DRAM_DMI1_A DRAM_CA0_A H2 CA0_A DRAM_CA1_A J2 CA1_A DRAM_CA2_A H9 CA2_A DRAM_CA3_A H10 CA3_A DRAM_CA4_A H11 CA4_A DRAM_CA5_A J11 CA5_A DMITA ATT DRAM DATAS A DOS A SIT DRAM DATAS A DOS A CIT DRAM DATAS A DRAM_CK_T_A DRAM_CK_C_A DRAM_DM0/DMI0_A/DMIL_N_A/_DBIL_N_A/DMIL_A AD23 __DRAM_DMI0_A DRAM_DM1/DM11_A/DMU_N_A/_DBIU_N_A/DMU_A AB20 __DRAM_DMI1_A AB16 DRAM AC14/A4/A4 AE8. DRAM AC32/CA0_B/C2/ AE9. DRAM AC33/CA1_B/CAS_N / A15/CAS AC7. DRAM AC23/CAS_B/A13/A13 AE7. DRAM AC23/CAS_B/A13/A13 AE8. DRAM AC3/CAS_B/A10/_AP AD6. DRAM_AC3/CAS_B/A0/A0 DRAM_CA0_B DRAM_CA1_B DRAM_CA2_B DRAM_CA3_B DRAM_CA4_B DRAM_CA4_B DRAM_DQS0_P/DQS0_T_A/DQSL_T_A/DQSL_A DRAM_DQS0_NDQS0_C_A/DQSL_C_A/DQSL_A AC25___DRAM_SDQS0_C_A G2 ODT_CA_A DMI0_B Y3 __DRAM_DMI0_B DRAM_DO16/DQ0_B/DQ1_B/DQ1_B/DQ1_B DRAM_DO17/DQ1_B/DQ1_B/DQ1_B DRAM_DO18/DQ2_B/DQ1_B/DQ1_B DRAM_DO18/DQ3_B/DQ1_B DRAM_DO18/DQ3_B/DQ1_B DRAM_D018/DQ3_B/DQ1_B/DQ1_B DRAM_D018/DQ3_B/DQ1_B/DQ1_B DRAM_D018/DQ3_B/DQ1_B/DQ1_B DRAM_D018/DQ3_B/DQ1_B/DQ1_B DRAM_D018/DQ3_B/DQ1_B/DQ1_B DRAM_D018/DQ3_B/DQ1_ DO B AA2 DRAM DATAG B DOT B Y2 DRAM DATAG B DOT B Y2 DRAM DATAG B DOZ B Y2 DRAM DATAG B DOZ B U2 DRAM DATAG B DOZ B U2 DRAM DATAG B DOZ B W4 DRAM DATAG B AC10 DRAM_AC34WE_N_/_A14/WE NVCC_DRAM_1V1 DRAM_CK_T_B DRAM_CK_C_B R2 CA0 B P2 CA1 B R9 CA2 B R10 CA3 B R11 CA4 B P11 CA5 B DMI1_B Y10 __DRAM_DMI1_B DRAM CAD B AD15. DRAM_AC17CK_C_ACKT_A AE15. DRAM_AC16CK_T_ACK_A AE12. DRAM_AC16CK_T_ACK_A AE12. DRAM_AC56CNT000T0 AE11. DRAM_AC58C0T0100T1 AE11. DRAM_AC58C0T100T1 AE15. DRAM_AC58C0T1N015 AE15. DRAM_AC58AC1X AE15. DRAM_AC58AC1X AE16. DRAM_AC58AC1X AE16. DRAM_AC58AC1X AE16. DRAM_AC58AC1X AE17. DRAM DRAM_CA1_B DRAM_CA2_B DOS B A411 DRAM DATAS B DOS B Y11 DRAM DATAS B DO10 B Y11 DRAM DATAS B DO10 B Y11 DRAM DATAS B DO10 B U11 DRAM DATAS B DO11 B U11 DRAM DATAS B DRAM_CA3_B DRAM_CA4_B DRAM_DM2/DMI0_B/DML_N_B / DBIL_N_B/DML_B AD3 __DRAM_DMI0_B DRAM_DMI1_B/DMU_N_B / DBIU_N_B/DMU_B AB6 __DRAM_DMI1_B DRAM_DGS2_P/DGS0_T_B/DQSL_T_B/DGSL_B DRAM_DGS2_NDGS0_C_B/DGSL_C_B/DGSL_B AC1 __DRAM_SDGS0_C_B ODT CA B T2 ODT_CA_B DQS1_T_B W10 DRAM_SDQS1_T_B DQS1_C_B V10 DRAM_SDQS1_C_B NVCC_DRAM_1V1 R208 DRAM_NRESET AB13 DRAM_RESET_N/RES GND .I DNU_AB12 AB12. DNU_AB1 AB11. DNU_AB2 AB2. DNU_AB1 AB1. DNU_AB1 AB1. DNU_AA12 AA12. DNU_B1 B12. DNU_B1 B12. DNU_B1 B12. DNU_A11 AB1. DNU_A11 AA1. DNU_A12 AA2. DNU_A11 AA1. AA14 DRAM_VREF/VREF/VREF DRAM VREF AA13 DRAM_ZN/ZQ/ZQ/ZQ A5 ZQ0 AB14 DRAM_AC19/MTEST/MTEST/MTEST AC13 DRAM_ALERT_N/MTEST1/ALERT_N / MTEST1/MTE GND GND G11 NC_G11 LPDDR4 Power supply voltage ramp RESET_n is held LOW. VDD1 >= VDD2 F1 VDD1-F1 F12 VDD1-F12 G4 VDD1-G4 G9 VDD1-G9 T4 VDD1-T4 T9 VDD1-T4 U12 VDD1-U12 VDD2 >= VDDQ **VDD 1V8** | VSS A10 AB. | DRAM CK T A DRAM CK T B GND DRAM_CK_C_A DRAM CK C B A4 VDD2_A4 VDD2_A9 VDD2_F5 VDD2_F5 VDD2_F8 H1 VDD2_H1 H1 VDD2_H1 H5 VDD2_H5 H8 VDD2_H8 H12 VDD2_H1 K1 VDD2_K1 K3 VDD2_K3 K10 VDD2_K10 K12 VDD2_K12 NVCC DRAM 1V1 K12 VDD2 K12 N1. VDD2 N1 N10. VDD2 N1 N10. VDD2 N3 N10. VDD2 N3 N10. VDD2 N1 R1. VDD2 N1 R5. VDD2 R5 R8. VDD2 R5 R8. VDD2 R2 US. VDD2 US US. VDD2 US US. VDD2 US US. VDD2 US AB4. VDD2 AB9 VDD2 AB9 GND NVCC DRAM 1V1 GND B3 VDDQ B3 B5 VDDQ B5 B8 VDDQ B5 B8 VDDQ B5 B10 VDDQ B10 D1 VDDQ B10 D1 VDDQ B10 D1 VDDQ D10 D2 VDDQ D10 D3 VDDQ D10 D4 VDDQ D10 D5 VDDQ D5 D6 VDDQ D5 D7 VDDQ D10 DRAM_VREF NVCC_DRAM_1V1 CND GND GND

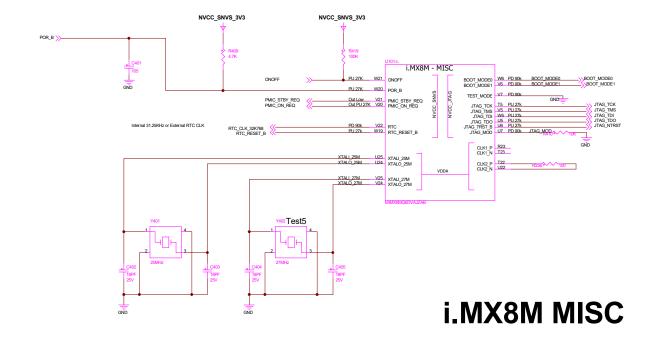
LPDDR4

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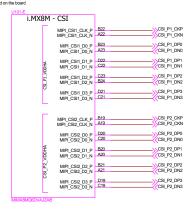
JTAG Debug

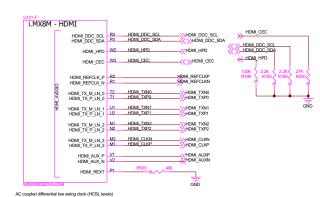




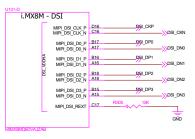
i.MX8M PHY

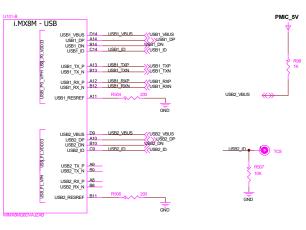
USB_RESREF. Atlach a 200-], 1% 100-ppm/C precision resistor-to-ground on the board.
MIPIOS_REXT: 15K-],
PCIE: 200_1/his h, 100 ppm/siC precision resistor to-ground on the board.
HDMIta 499(, (j.41% tolerance) resistor to-ground on the board.



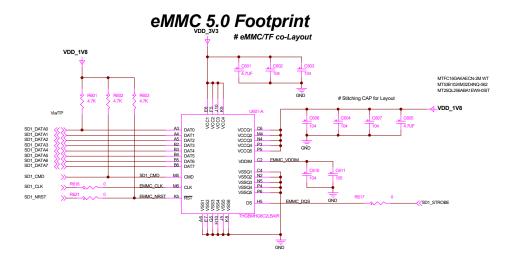


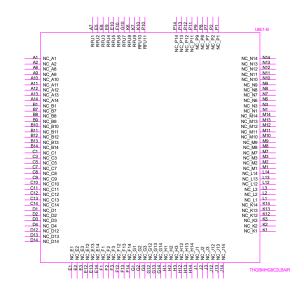




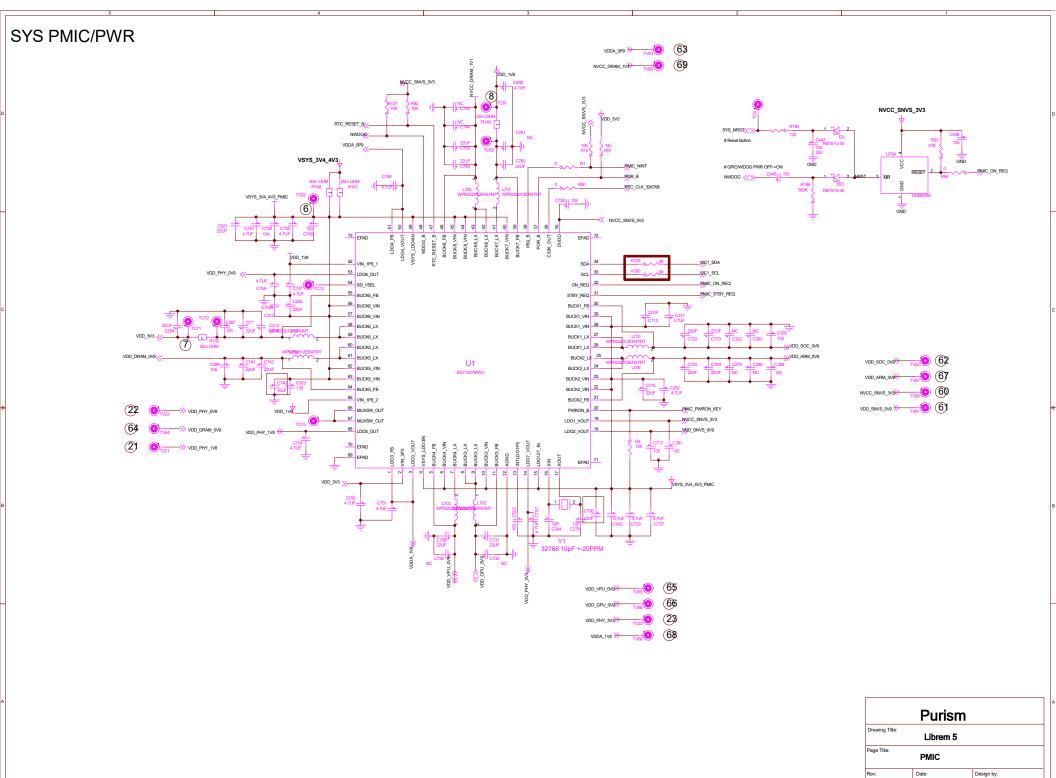


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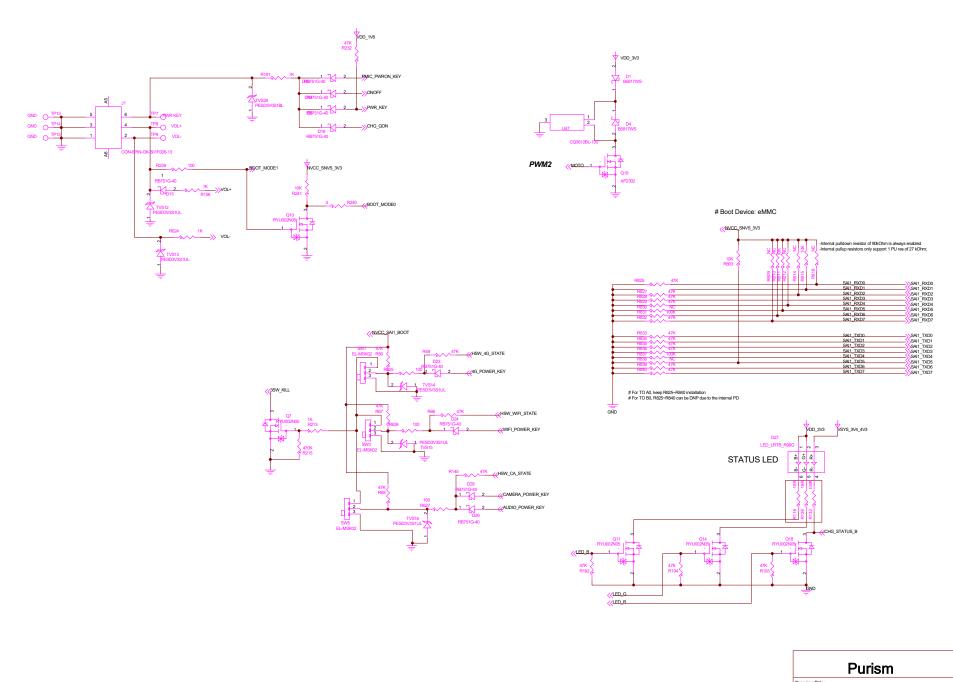


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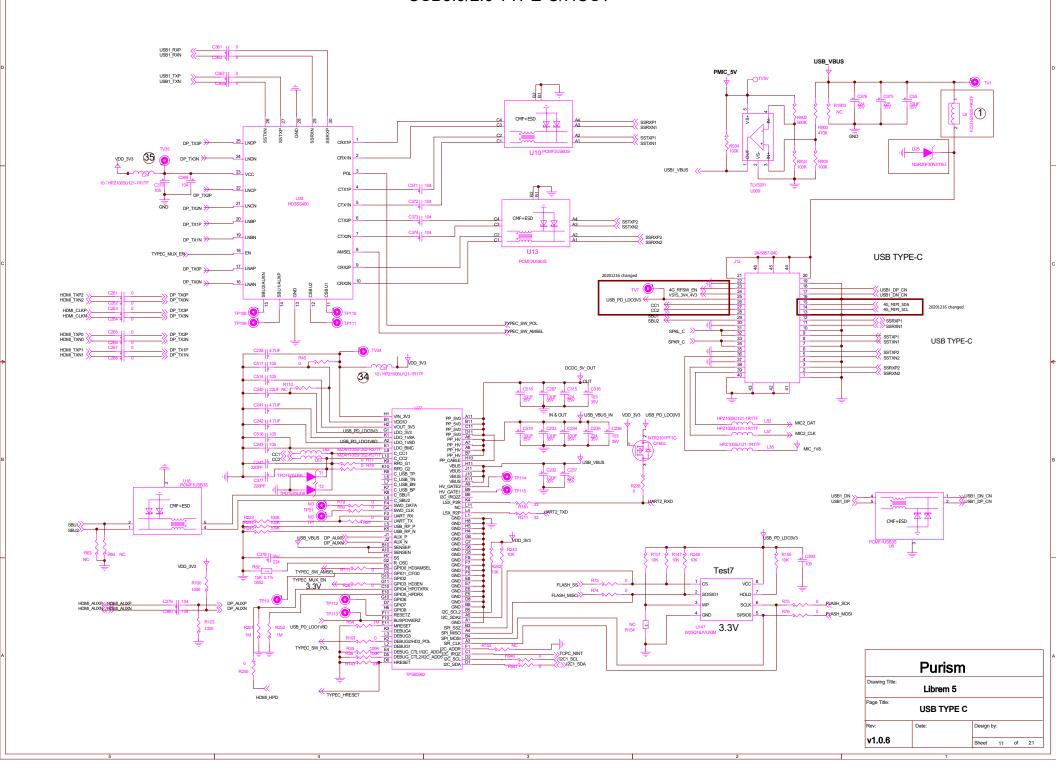
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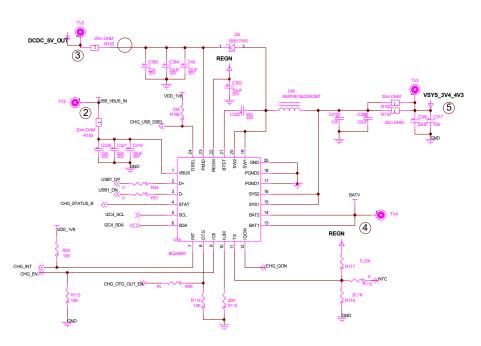
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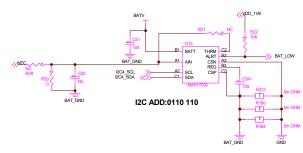


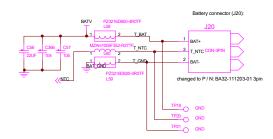
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USB3.0/2.0 TYPE-C/HOST

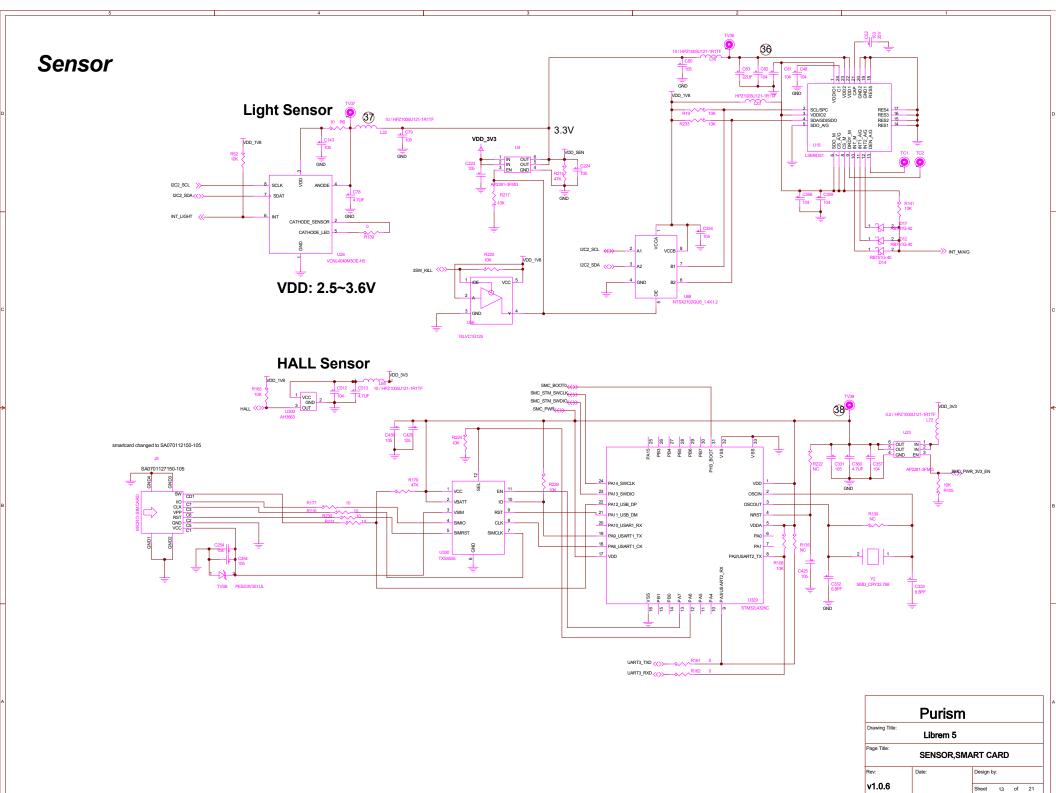


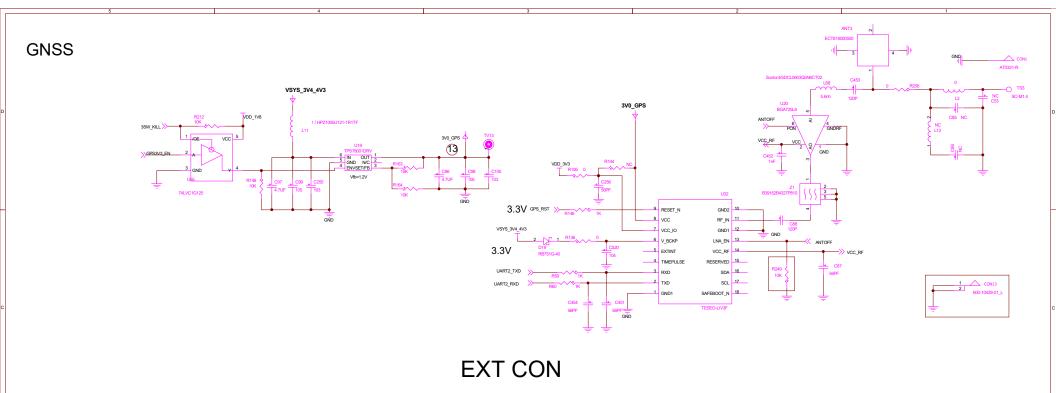


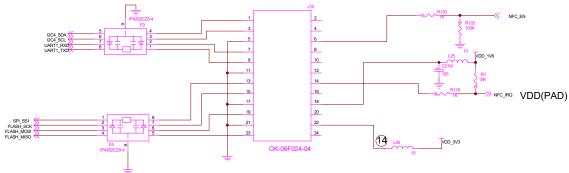




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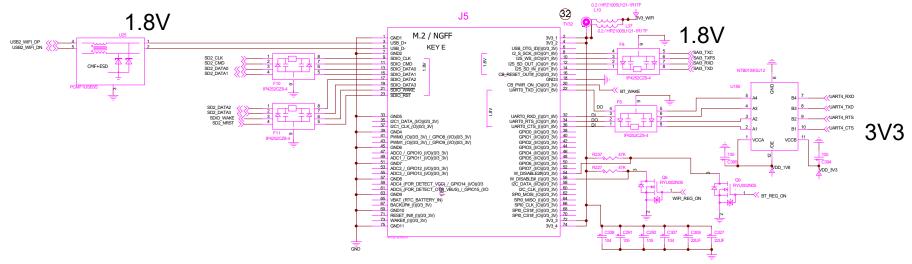


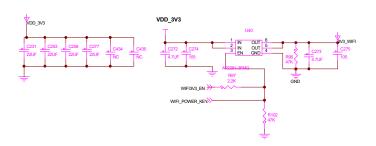


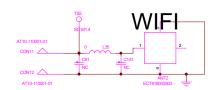


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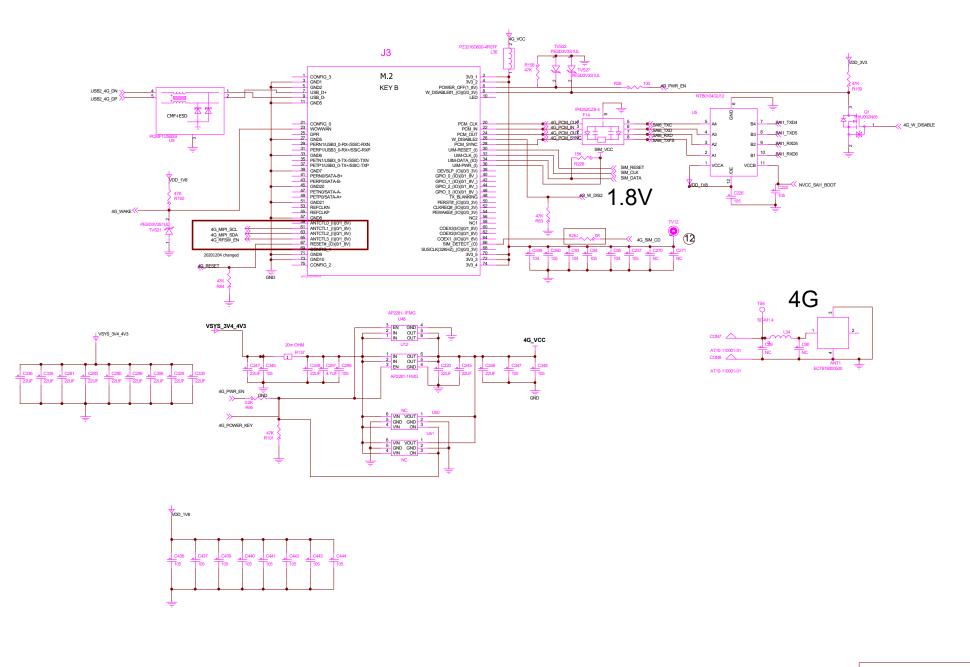
WiFi/BT 802.11a/b/g/n/ac + Bluetooth 4.1/ EDR



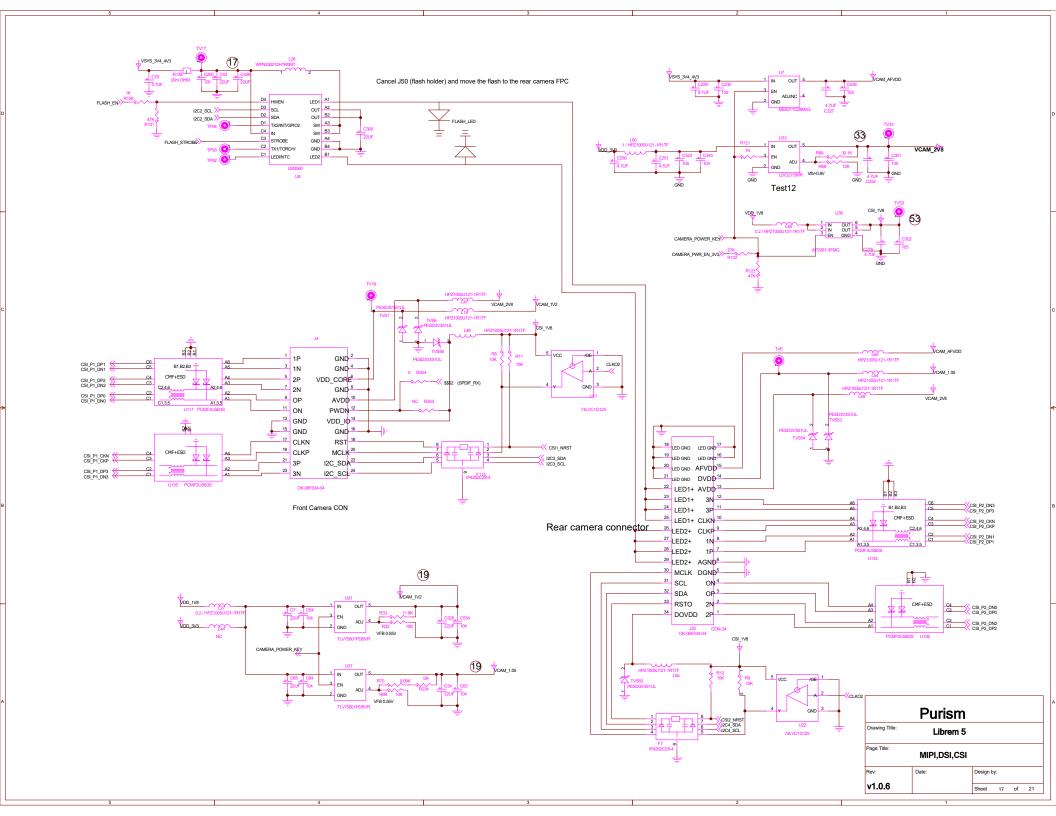




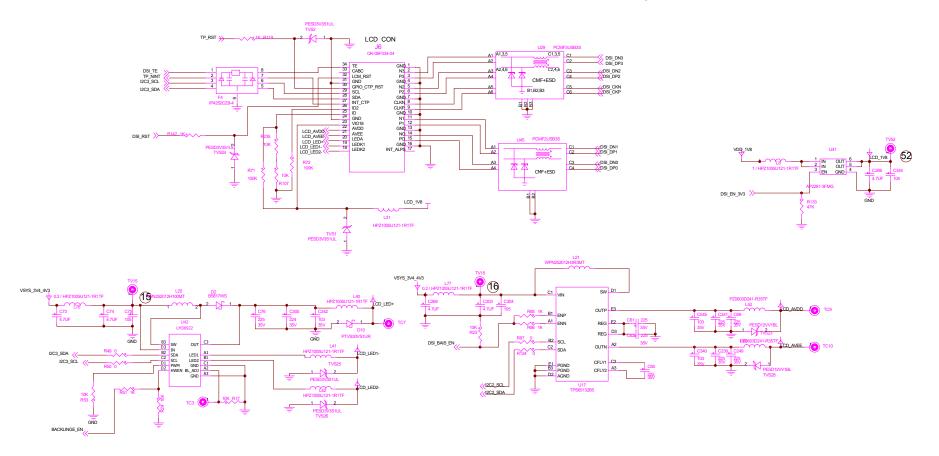
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v1.0.6		Sheet 15 of 2



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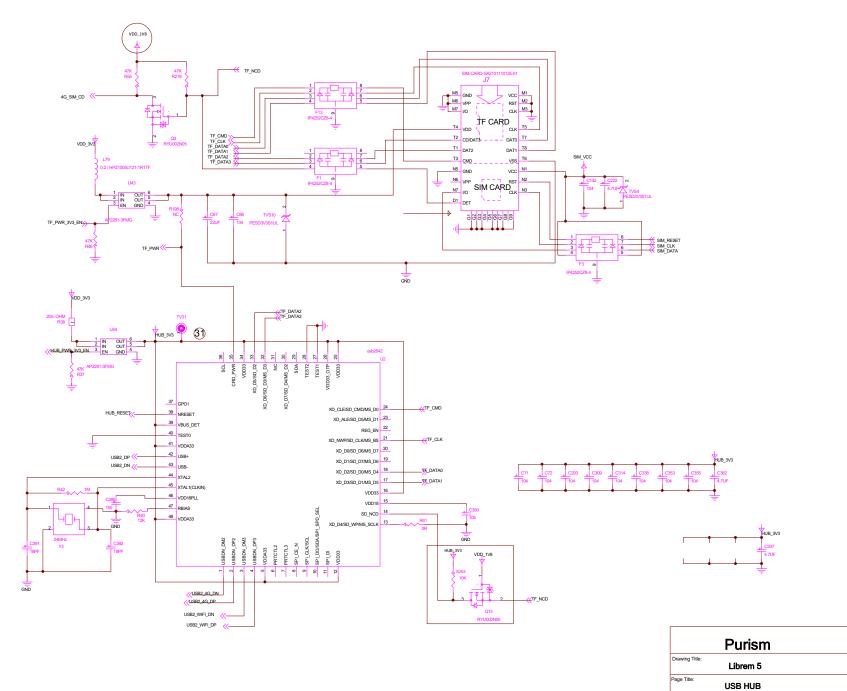


DSI LCD IF



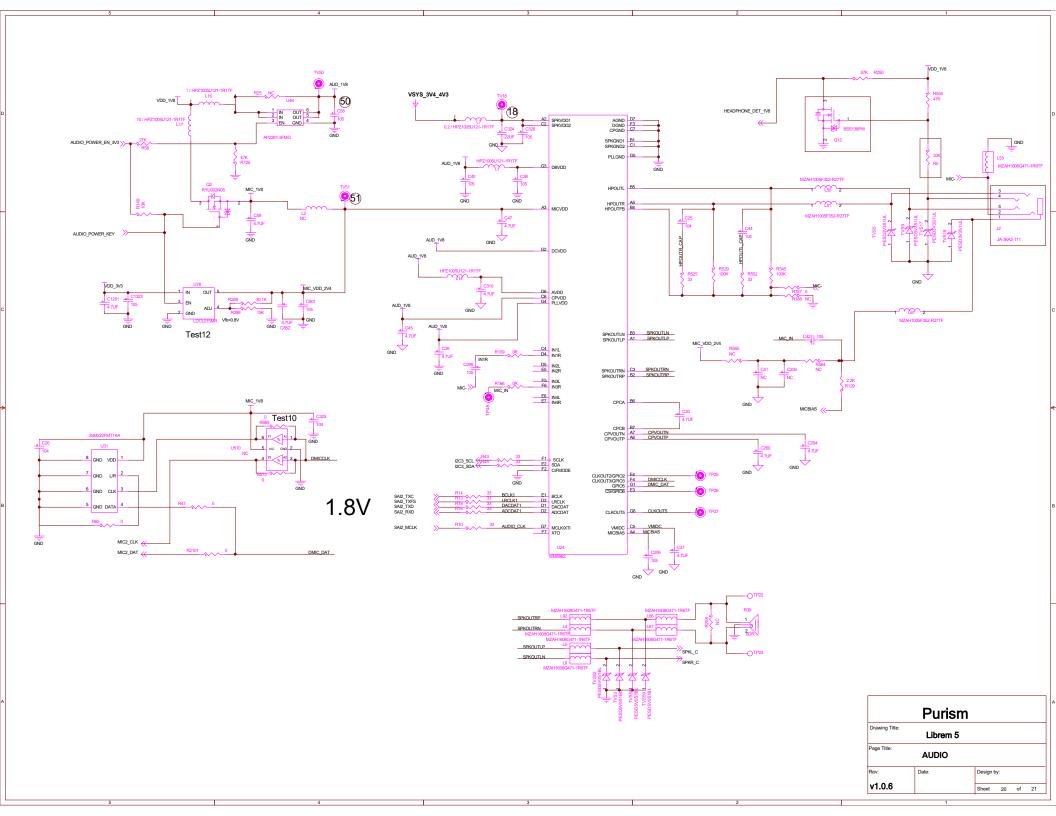
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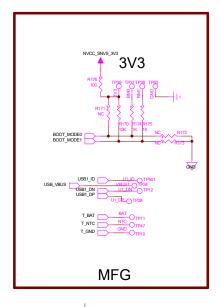
USB HUB + SDIO BRIDGE

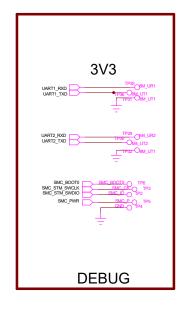


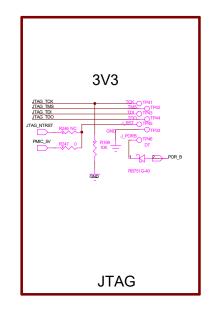
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M2 module SCREW

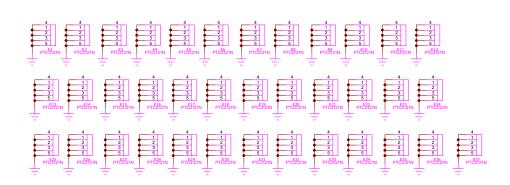
BOOT TYPE
Boot From Fuses
Serial Downloader
Internal Boot (Development)
Reserved

SCREW

Shielding Case

Shielding Case Hold





Purism									
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