(Used Table 48) CHECK TABLE 29/30!!! +3V3 PWR_FLAG M.2_Key_B CONFIG_2 70 CONFIG_1 SUSCLK SIM_Detect COEX1 COEX2 COEX3 69 68 Reset 66 64 ANTCTL3 62 ANTCTL1 ANTCTL0 60 ×58 ×56 ×54 59 REFCLKR <u>PEWake</u> PEWake CLKREQ PERST GPIO_4 GPIO_3 GPIO_2 GPIO_1 REFCLKN 52 50 PETp0/SATA-A+ 48 PETn0/SATA-A-46 44 PERpO/SATA-B-42 PERnO/SATA-B+ GPIO_0 40 DEVSLP 38 37 PETp1/USB3.0-Tx+/SSIC-TxP UIM-PWR UIM-DATA 36 35 PETn1/USB3.0-Tx-/SSIC-TxN 34 32 JIM-CLK UIM-CLK UIM-RESET GPIO_8 GPIO_10 GPIO_7 GPIO_6 GPIO_5 31 PERp1/USB3.0-Rx+/SSIC-RxP 30 29 PERn1/USB3.0-Rx-/SSIC-RxN 28 26 GPI0_12 GPI0_11 24 22 CONFIG_Q GPIO_9/DAS/DSS +3V3 XE.... C USB_D-X USB_D+X Full_Card_Power_Off 6 PWR_FLAG CONFIG_3 I

Unfortunately, it seems most WWAN modules don't explicitly support SSIC This will need to be looked into:

"SSIC brings 80% power savings using a MIPI

M-PHY and SSIC, as compared to a USB 3.0 PHY"

"HSIC supported on WWAN configuration 3"

3.2.5. SSIC Interface

SuperSpeed USB Inter-Chip (SSIC) is a chip-to-chip interconnect interface defined as a supplement to the USB 3.0 Specification. SSIC augments USB 3.0 in that the physical layer of the interconnect is based on the MIPI® Alliance M-PHYSM rather than the external cable-capable PHY of traditional SuperSpeed USB. This method better optimizes power, cost, and EMI robustness appropriate for being used for embedded inter-chip interfaces. All higher-layer aspects (software, transaction protocol, etc.) of SSIC follow the USB 3.0 specification.

SSIC – Inter-Chip Supplement to the USB 3.0 Specification, Revision 1.0 as of May 3, 2012; available from http://www.usb.org/developers/docs/ and located within the USB 3.0 Specification download

Huawei MU736 is an example of 3G M.2 card which supports SSIC The i.MX 8M does not explicity state SSIC support

MAIN 1 GND Conn_Coaxial GPS 1 GND Conn_Coaxial AUX 10

Conn_Coaxial ANT4

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