(Used Table 48) CHECK TABLE 29/30!!! +3V3 PWR_FLAG M.2_Key_ CONFIG_2 70 CONFIG_1 SUSCLK SIM_Detect COEX1 COEX2 COEX3 68 Reset 67 66 64 62 ANTCTL3 ANTCTL2 60 ×58 ×56 ×54 52 61 ANTCTLO 57 REFCLKP REFCLKN PEWake CLKREQ PERST 50 PETp0/SATA-A+ 49 GP10_4 48 PETn0/SATA-A-46 GPI0_3 GPI0_2 44 43 PERp0/SATA-B-GPIO_1 42 PERnO/SATA-B+ 41 GPIO_0 40 DEVSLP 38 37 PETp1/USB3.0-Tx+/SSIC-TxR 36 35 PETn1/USB3.0-Tx-/SSIC-TxN 34 ÙIM – DATA 32 30 UIM-CLK 31 PERp1/USB3.0-Rx+/SSIC-RxR ĴUIM−RESE1 29 PERn1/USB3.0-Rx-/SSIC-RxN GPI0_8 28 GPI0_10 26 GPI0_12 GPI0_7 GPI0_11 GPI0_6 GPI0_5 CONFIG_Q USB_D-W_DISABLE1 USB_D+ Full_Card_Power_Off PWR_FLAG CONFIG_3

Unfortunately, it seems most WWAN modules don't explicitly support SSIC This will need to be looked into:

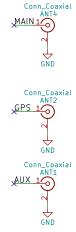
"SSIC brings 80% power savings using a MIPI M—PHY and SSIC, as compared to a USB 3.0 PHY" "HSIC supported on WWAN configuration 3"

3.2.5. SSIC Interface

SuperSpeed USB Inter-Chip (SSIC) is a chip-to-chip interconnect interface defined as a supplement to the USB 3.0 Specification. SSIC augments USB 3.0 in that the physical layer of the interconnect is based on the MIPI® Alliance M-PHYSM rather than the external cable-capable PHY of traditional SuperSpeed USB. This method better optimizes power, cost, and EMI robustness appropriate for being used for embedded inter-chip interfaces. All higher-layer aspects (software, transaction protocol, etc.) of SSIC follow the USB 3.0 specification.

SSIC – Inter-Chip Supplement to the USB 3.0 Specification, Revision 1.0 as of May 3, 2012; available from http://www.usb.org/developers/docs/ and located within the USB 3.0 Specification download package.

Huawei MU736 is an example of 3G M.2 card which supports SSIC The i.MX 8M does not explicity state SSIC support



GNU GPLv3 Copyright 2018

Purism SPC

Sheet: /

File: m2_key_b_3042_template.sch

Title:	M.2	Key	В	3	042	Tem	iplate	
C: A	,		D .		2040	0.7	4.5	

Size: A4	Date: 2018-03-15	Rev: 0.5.0
KiCad E.D.A. kid	ld: 1/1	
- 1.		