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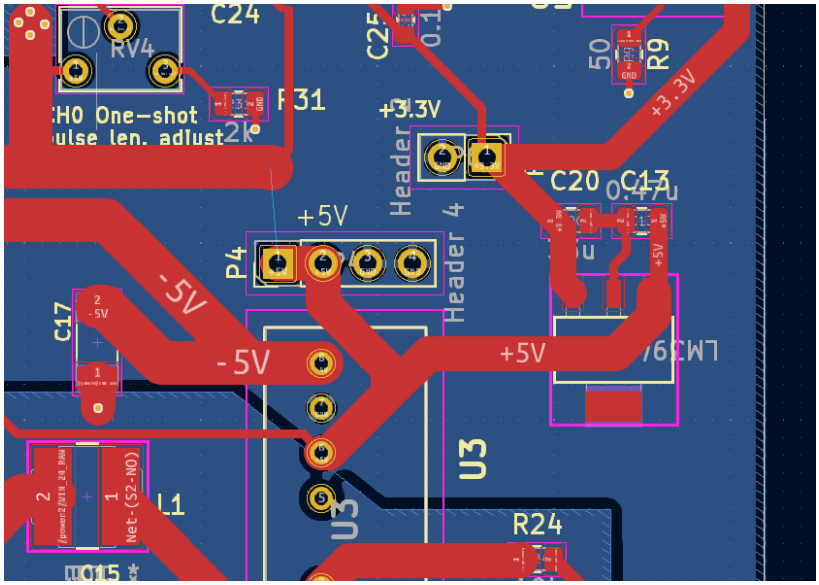
PMT DRIVER
12/19/2025

Summary:
PMT driver confirmed working, tested with oscope and PMT. If it isn't working try adjusting potentiometer values for integrating op amp (RV1 RV2) and comparator (RV3 RV4).

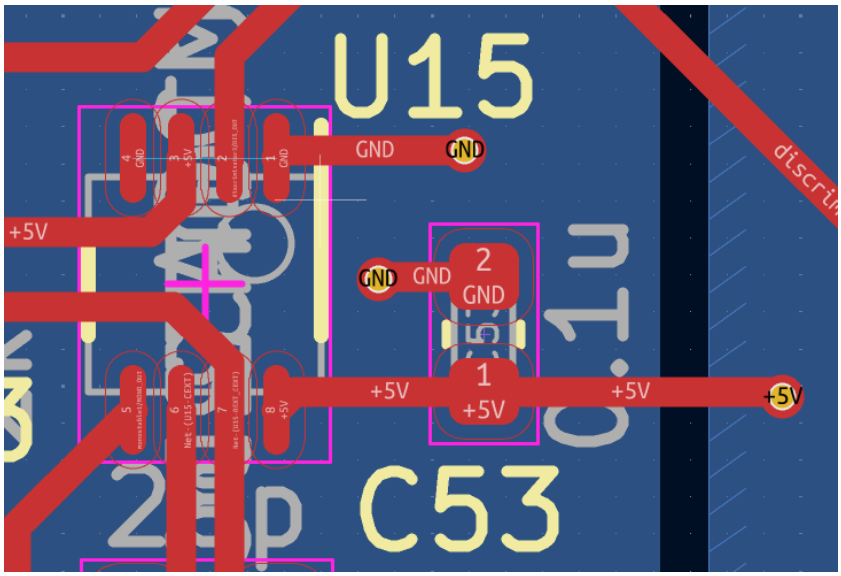
The PMT driver supplies 15V, GND, and adjustable bias to PMT. Reads in short low voltage pulses from PMT and amplifies them to 3.3V.
Pulse -> output:
Op amp chain (buffer, inverting, integrating)-> Comparator -> Monostable -> LVDS out, 3.3V out

Some errors in pcb needed to be corrected with jumpers / slight modifying of components. Correct traces have been added however component footprints have been kept the same.

ERRORS IN PCB: (FIXED)



LDO not connected to ground (right), missing trace (left). Issue with footprint and left floating in schematic.
On board:
Fixed with jumpers
On revision:
Placed GND via



Monostable GND pin left hanging. The pin that is grounded is for the configuration (hold that one to GND to trigger off some other pin or something). Measured with DMM during operation seems to be hovering around 1v, smaller negative jump with input pulse then goes higher after but it did work.
On Board:
Added jumper to GND now both read 0 functions the same as before from what I can tell
On revision:
placed GND via

C6 decoupling capacitor on op amp chain, connected near hdmi power.
Moved to the proper spot in the op amp chain on revision.

COMPONENTS LEFT UNSOLDERED:
Optional:
R19, C35 on ch 1 and R4 C1 (1st filter) soldered with jumpers. Not necessary but configurable if later desired
C42 C9 extra optional capacitor for filtering on Op Amp chain
R23, R8 50 ohm termination for pin headers currently left unsoldered.
LEFT UNCHANGED:
RV1 and RV2 (potentiometer 1k) are the wrong footprint for what was ordered. Ordered: legs are in a line
On PCB: legs are in triangle layout can be bend into shape to fit

Push buttons for power are the wrong footprint. Connections are incorrect and the current routing tries to use the mounting pads for signal.

Notes:
10/20/2025:
Power circuity seems operational, see expected voltages on all outputs.
The 5V to 3.3V converter isn't grounded (pins left floating) so there is currently a jumper wire to nearby ground pin
The on off switches for 5V, 15V have a footprint error, notes say that they shouldn't work/ should't be plugged in but this works for now (no real load)

Timon said test the circuit with a load and then run some calculations on expected power draw and report back with numbers.
10/25/2025
Stripped some pads and had the power input backwards for a bit also shorted something but we are back and it works, leaving off at power works and now need to start adding actual pmt driver stuff. Test with function generator a oscope as I add each piece (test incrementally :))

Question:
Amplifying and stretching out small ns pulses when we stretch out pulses can we accidentally stretch them out so that we can't detect two that are close tgt? Is this avoided through stretching just enough but not too much? Setting proper peak detection?
Need lemos :/
Green box: 10nf 16V 0805

Seeing same thing from buffer and inverting omp amp at the same time/?? What the shit

10/31/2025:

Seeing 20x gain as expected but only under certain inputs? Something about negative? Not 100%

See expected 180deg offset as well

Noisy, most of noise seems to be present when the 15v voltage source is turned on..

11/3/2025:

First two stages look good,

added ad8007 op amp: output is -4v flat, input is sinusodial.
Power looks correct, measured feedback resistance = 1.5k ohm

Input 1V sin wave -2v offset onto in pin , -4 V dc out 100us period
Bias op amp incorrectly -> results in clipping

11/5/2025

Most prev seen issues were due to input amplitude being to high -> op amp goes to rail before it can make a sin wave. Made input amplitude = 10mv and now everything up until stage 3 looks good.

Now focusing on the comparator

HYSTERESIS MODE AND TIMING (ADCMP601/ADCMP602 Only)						
Hysteresis Mode Bias Voltage		Current −1 µA	1.145	1.25	1.35	V
Resistor Value		Hysteresis = 120 mV	65	80	120	kΩ
Hysteresis Current		Hysteresis = 120 mV	−18	−12	−7	µA
Latch Setup Time	t_S	V_{OD} = 50 mV		−2		ns
Latch Hold Time	t_H	V_{OD} = 50 mV		2.6		ns
Latch-to-Output Delay	t_{PLOH}, t_{PLOL}	V_{OD} = 50 mV		27		ns
Latch Minimum Pulse Width	t_{PL}	V_{OD} = 50 mV		21		ns

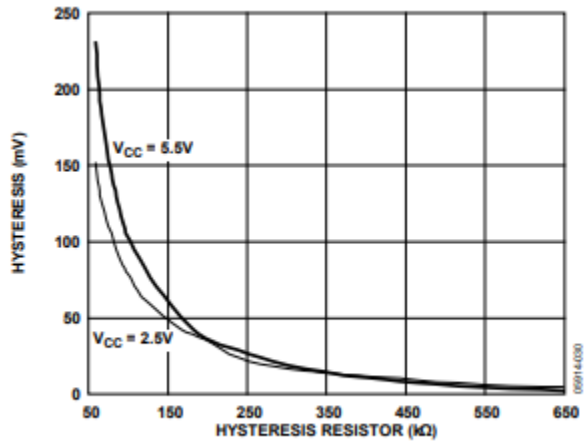


Figure 21. Hysteresis vs. R_{HYS} Control Resistor

Discriminator/Comparator no output hmmm ….
Fixed: had to adjust comparator threshold with potentiometer

Monostable:

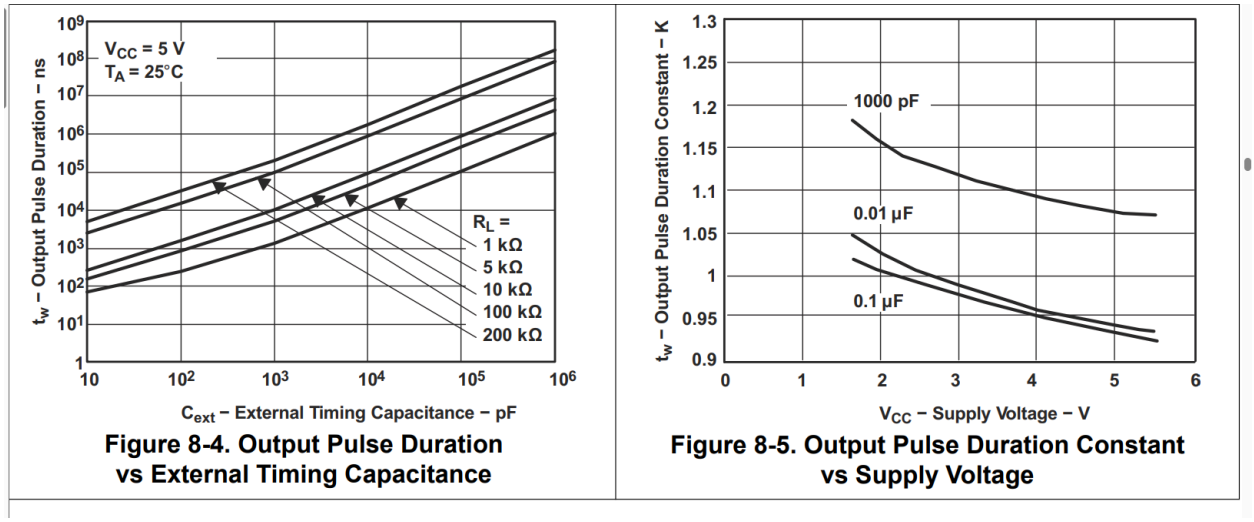
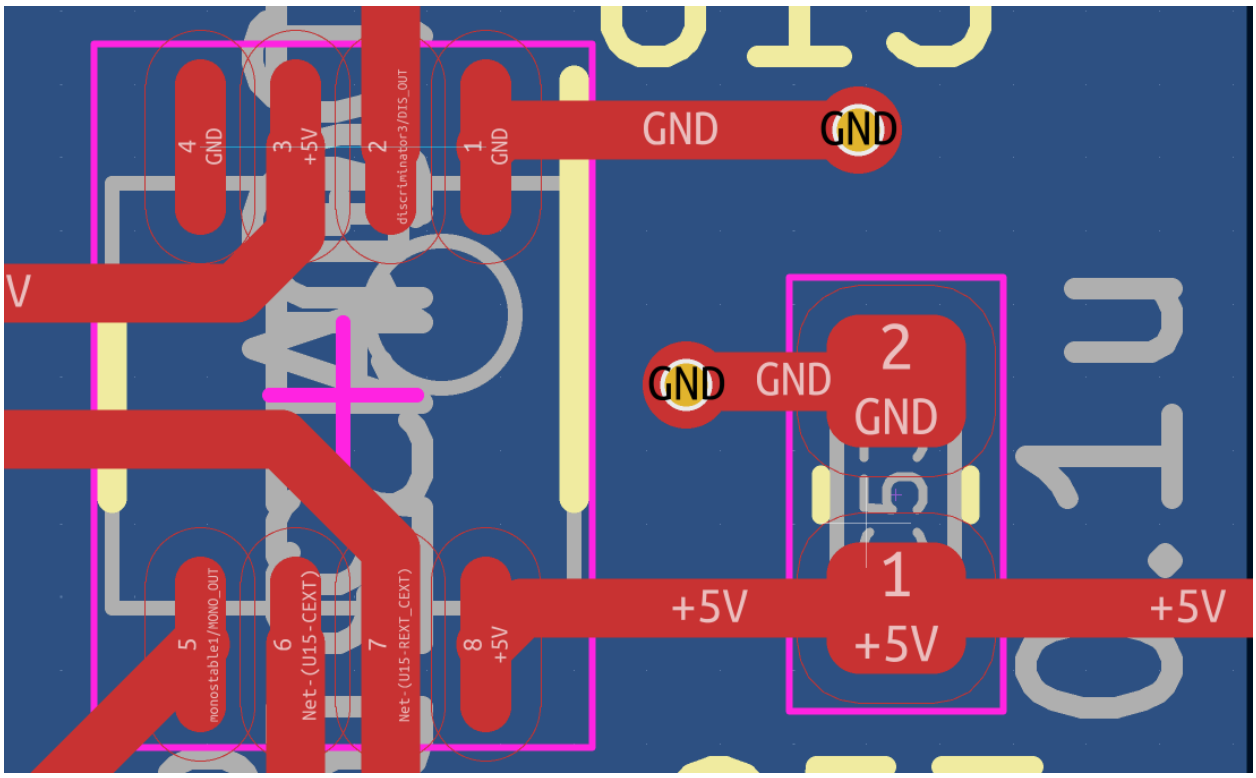


Figure 8-4. Output Pulse Duration vs External Timing Capacitance

Figure 8-5. Output Pulse Duration Constant vs Supply Voltage

Outputs same pulse width right now it is very small using joe's numbers but maybe thats okay?
Acts as expected though maybe get more details on expected output
All op amp parts down now just output + jumper + double check then same for ch1

11/17:
Both channels working as expected :)
U15 is missing a connection to ground on one of its pins



Output is same but should prolly add jumper!

Do not have sn65lvds1dbvr IC

Timon mentioned something about polarity out of comparator being inverted but everything seems good

Solder jumpers to output the monostable output

11/21/2025:
Some notes: at low freq monostable doesn't output anything. Worked at 1mhz not at 10k hz…
Explore more later

Using 0.010V for all testing

Got some pictures with small input pulse

12/1/2025:
Both channels work with 0.01V pulse. added jumper for U15

12/18/2025:
Now working on output circuitry:
Ch0:
3.3V lvds looks good correct voltage and differential (CMOS-VLDS)
Level shifter is config for 5V 3.3V but outputting 2.5V???
Ch1:
3.3V lvds looks good correct voltage and differential (CMOS-VLDS)