Floating Point Implementation
UKY EE 480

Grant Cox
University of Kentucky
grant.cox@uky.edu

Josh Carroll
University of Kentucky
Josh email

3rd
University of Kentucky
email

***Abstract*—The final component of the PinKY archetecture was to be a "mutant" 16-bit floating point module (FPU). The FPU performs conversions, multiplications, reciprocals, additions, and subtractions on floats with 1 sign bit, 8 exponent bits, and 7 mantissa bits. This is a multicycle design using a state machine in Verilog. It was simulated and tested in Icarus Verilog with GtkWave.**

I. Approach

A. FTOI

B. ITOF

C. MULF

D. RECF

E. ADDF

F. SUBF

II. Issues

It don't work yet