

COMPUTATION BOOK

NAME

Grant Abella

COURSE ECE 322 02 Lab Book C



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✓ Laboratory #3: Operational Amplifiers and Applications

Partner: ✓ Grant Abella
Brandon Lepert
9/11/18

✓ Advisor: Dr. Gutschlag
Advanced Preparation:

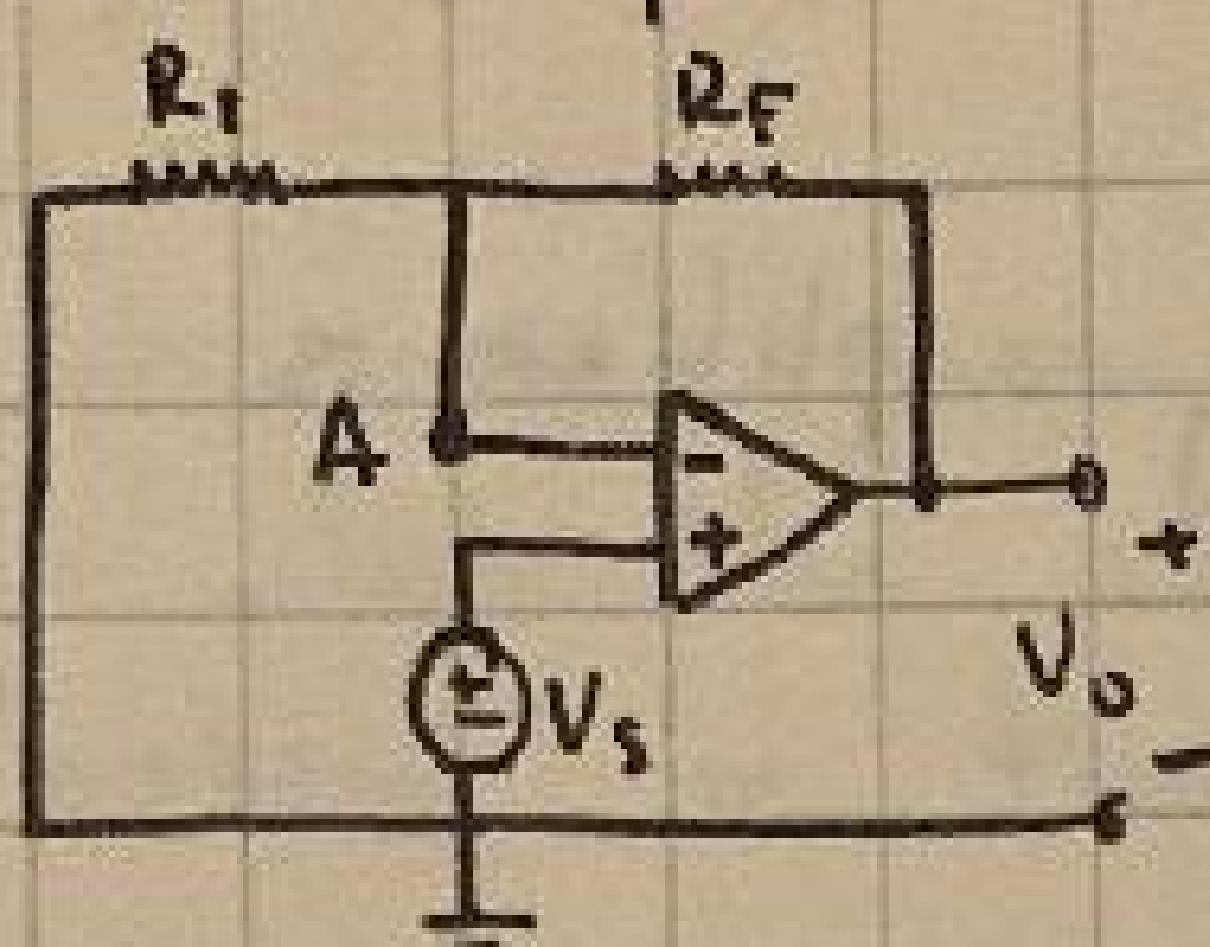


Figure 3-1: negative feedback op-amp circuit.

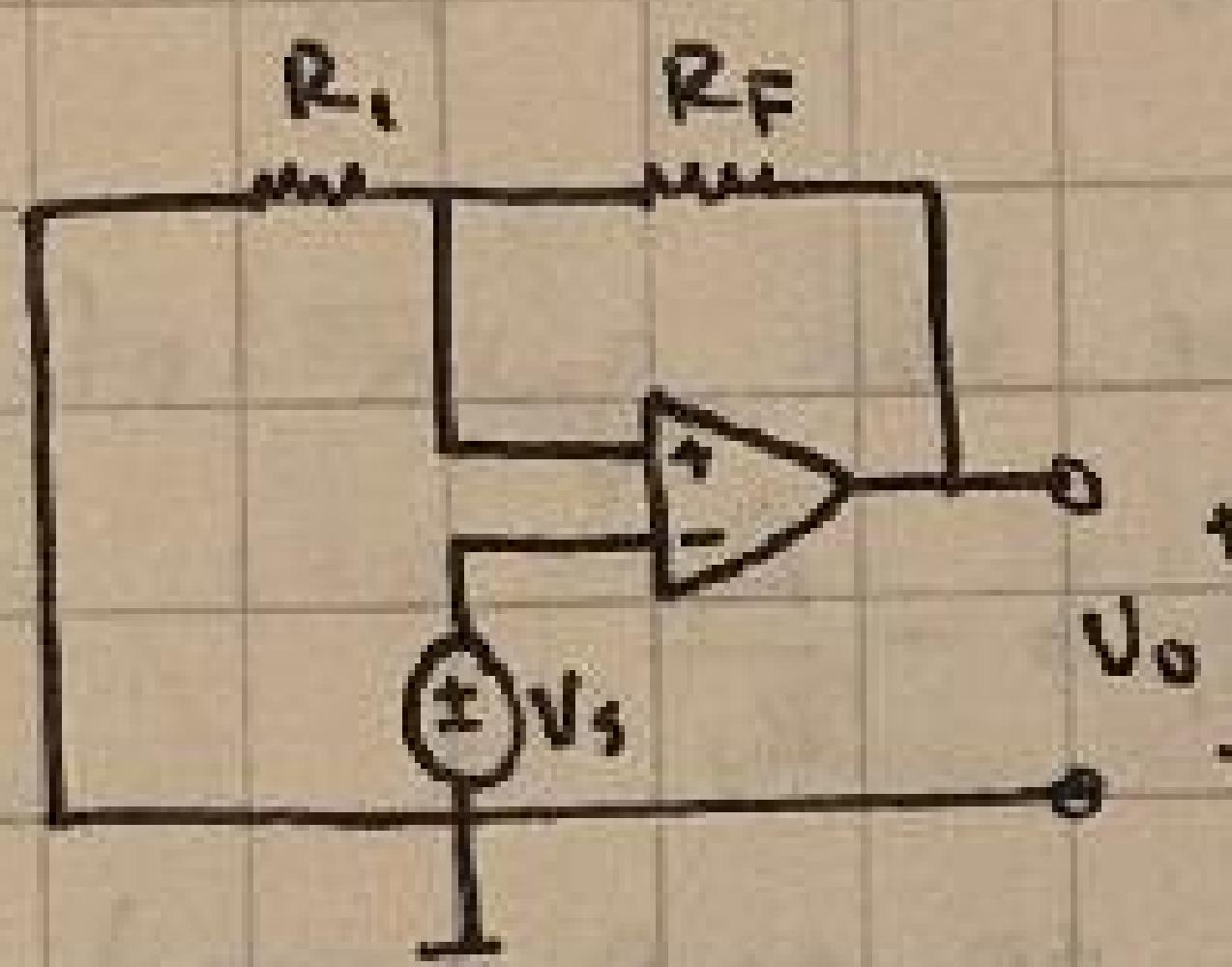


Figure 3-2: positive feedback op-amp circuit.

- ✓ 1. A virtual ground (or virtual short circuit) for an ideal op-amp used in a negative feedback configuration is a result of the voltage value at node A in Figure 3-1 getting continuously smaller as current flows through the circuit.

The formula for V_o is:

$$V_o = A_o (V^+ - V^-)$$

$$= (1E5) (0 - \frac{V_s}{2})$$

Very good in depth explanation!
+1
for an input of $V_s = 1V$: $V_o = (1E5)(0 - 0.5) = -50000V$, but the op-amp will try to adjust this value because it is too high, so the next iteration will be:

$V_o = (1E5)(0 - 0.25) = -25000V$, and so on until a value of $\approx -10V$ is reached for V_o . At this point, the voltage value at node A is around $100mV$ in order to make the following equation true:

$$V_o = (1E5)(0 - 100mV) = -10V$$

For this reason, the terms virtual ground and virtual short are commonly used when describing negative feedback op-amp circuits, because the value at the op-amp inputs is so close to zero that it is basically a ground. With this said, the term virtual short circuit might be a better description of what is occurring here since there is still a voltage present (although small).

- ✓ 2. Positive feedback configurations are unstable because their outputs are fed right back into their positive inputs. This creates a situation where the output value keeps rising until saturation is reached. Negative feedback configurations do not have this problem because their outputs are fed back into their negative input.

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3. The equation for computing the gain for a non-inverting amplifier

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configuration is

$$A_F = 1 + \frac{R_F}{R_1}$$

and the equation for the gain of an inverting amplifier is

$$A_F = -\frac{R_F}{R_1}$$

For a typical 741 op amp used in this lab,

$$\text{Unity-Gain-Bandwidth} = UGB = A_{of}f_o = A_F f_F$$

$$A_0 = \text{open-loop-gain} \approx 200000 \text{ V/V}$$

$$A_F = \text{closed-loop-gain at } f=0$$

$$f_o = \text{open-loop } 3\text{-dB down frequency} \approx 5 \text{ Hz}$$

$$f_F = \text{closed-loop } 3\text{-dB down frequency}$$

a) For a configuration with a gain = -2 and $R_{in} = 1k\Omega$:

$$-2 = -\frac{R_F}{1k\Omega} \rightarrow R_F = 2k\Omega$$

b) For a configuration with a gain = -2 and $R_{in} \geq 1k\Omega$:

$$\text{with } R_{in} = 2k\Omega:$$

$$-2 = 1 + \frac{R_F}{2k\Omega} \rightarrow R_F = 2k\Omega$$

c) For a configuration with a gain = -100 and $R_{in} = 1k\Omega$:

$$-100 = -\frac{R_F}{1k\Omega} \rightarrow R_F = 100k\Omega$$

d) For a configuration with a gain = +100 and $R_{in} \geq 1k\Omega$:

$$\text{with } R_{in} = 1.1k\Omega:$$

$$100 = 1 + \frac{R_F}{1.1k\Omega} \rightarrow R_F = 108.9k\Omega \approx 100k\Omega$$

For a non-inverting amplifier configuration, the closed-loop 3 dB small signal bandwidth is calculated as

$$f_F = \frac{UGB}{A_F}$$

and for an inverting amplifier configuration as

$$f_F = \frac{UGB}{(1-A_F)}$$

Using these equations, the f_F values for each configuration above were calculated and placed in the table below:

OpAmp	Inverting	$R_1 [ohm]$	$R_F [ohm]$	$A_0 [\text{v/v}]$	$A_F [\text{gain}]$	$f_0 [\text{Hz}]$	$f_F [\text{Hz}]$	UGB
A	Y		1	2	200000	-2	5	333333.3
B	N		1	1	200000	2	5	500000
C	Y		1	100	200000	-100	5	9900.99
D	N		1.1	100	200000	100	5	10000

Table 4-1: Gain and 3-dB down frequency values for the four OP-amp configurations above.

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These values are significant because with frequencies beyond these, op-amp outputs will begin to distort.

For an input signal $v_{in}(t) = V_i \sin(2\pi 200t)$, the maximum value of V_i at which the output begins to clip is ± 14 V. This was found by looking in the 741 datasheet at figure 5 on page 7.

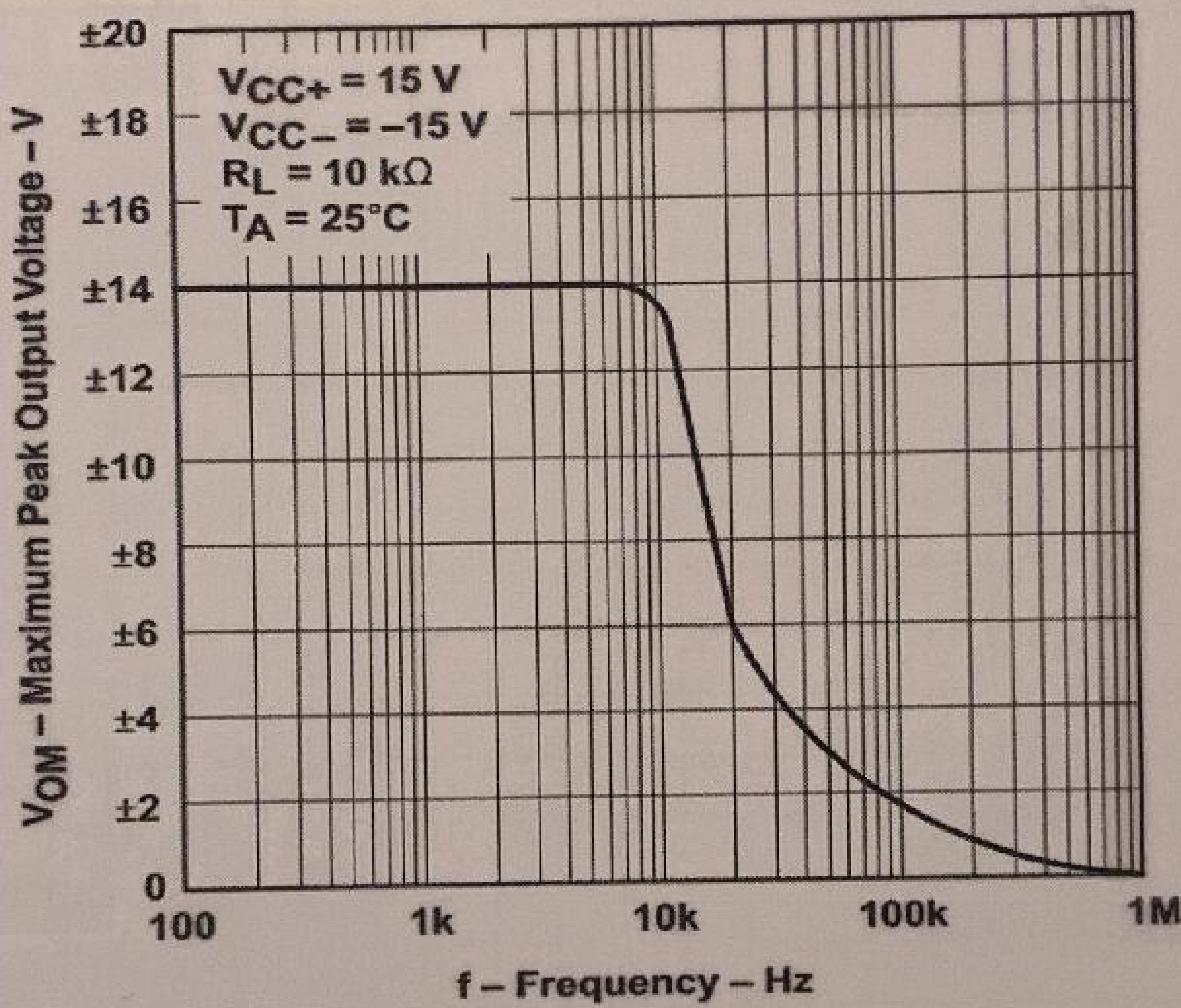


Figure 5-1: Maximum Peak Output Voltage vs. Frequency for the 741 op-amp.

good job!

Laboratory:

offsetNC	1	8	N/C
IN-	2	7	V _{CC+}
IN ⁺	3	6	OUT
GND	4	5	OFFSETN2

Equipment Used:

- Tektronics Oscilloscope EQ-3017
- HP DC PSU EQ-2082
- Fluke 45 DMM EQ-2195
- Agilent Waveform generator EQ-2618
- 741 Op-Amp

Figure 5-2: Pin configuration for u741 op-amp.

1. For all four configurations, the bias voltage inputs V_{CC+} and V_{CC-} will come from the HP DC PSU listed above. Input voltage will be provided by the signal generator, and the signal will be a periodic sine wave with a peak-to-peak value of 2 volts. We will measure output voltages using the oscilloscope, and these values will be recorded in an Excel spreadsheet.

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As we take samples of the output voltage (and gain), we will

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increase the frequency of the input signal.

Gain Magnitude vs. Frequency for Configuration A:

The configuration for A is as follows:

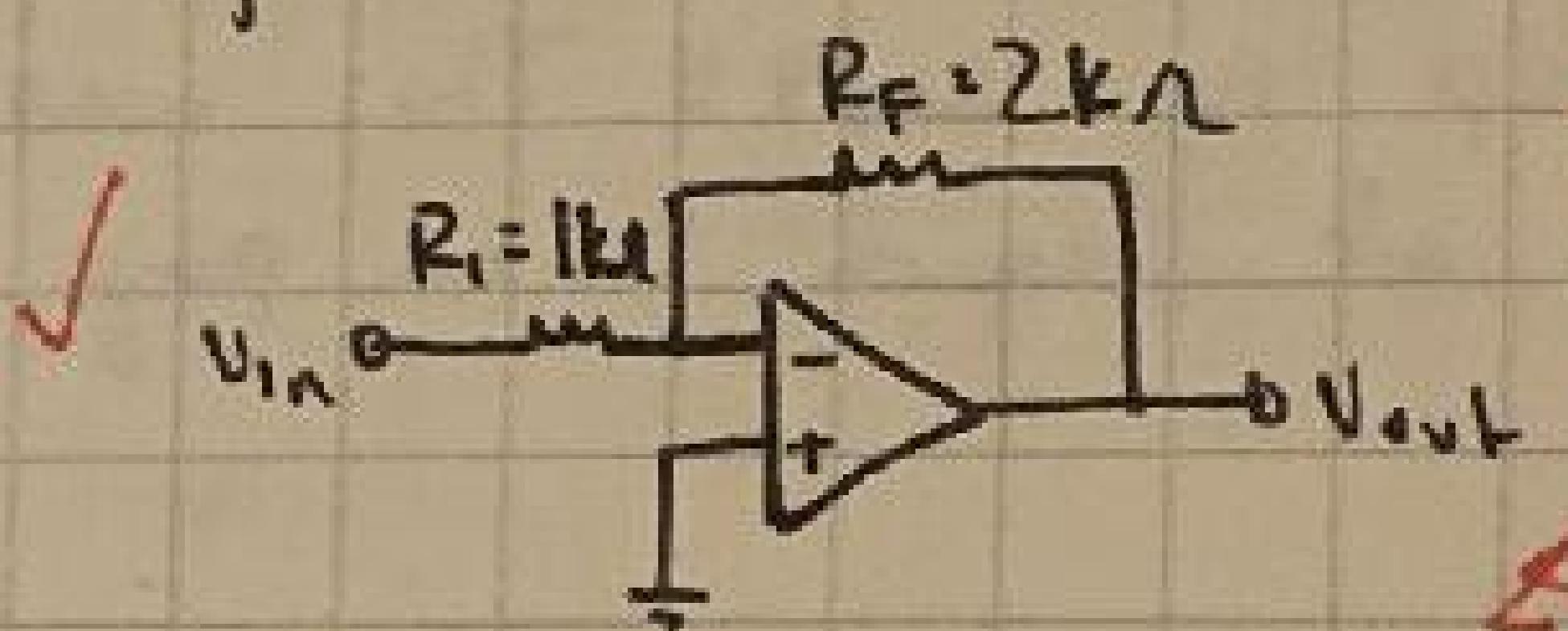


Figure 6-1's
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Figure 6-1: Inverting Op-Amp configuration with gain of -2.

On the breadboard, we implemented this circuit like so:

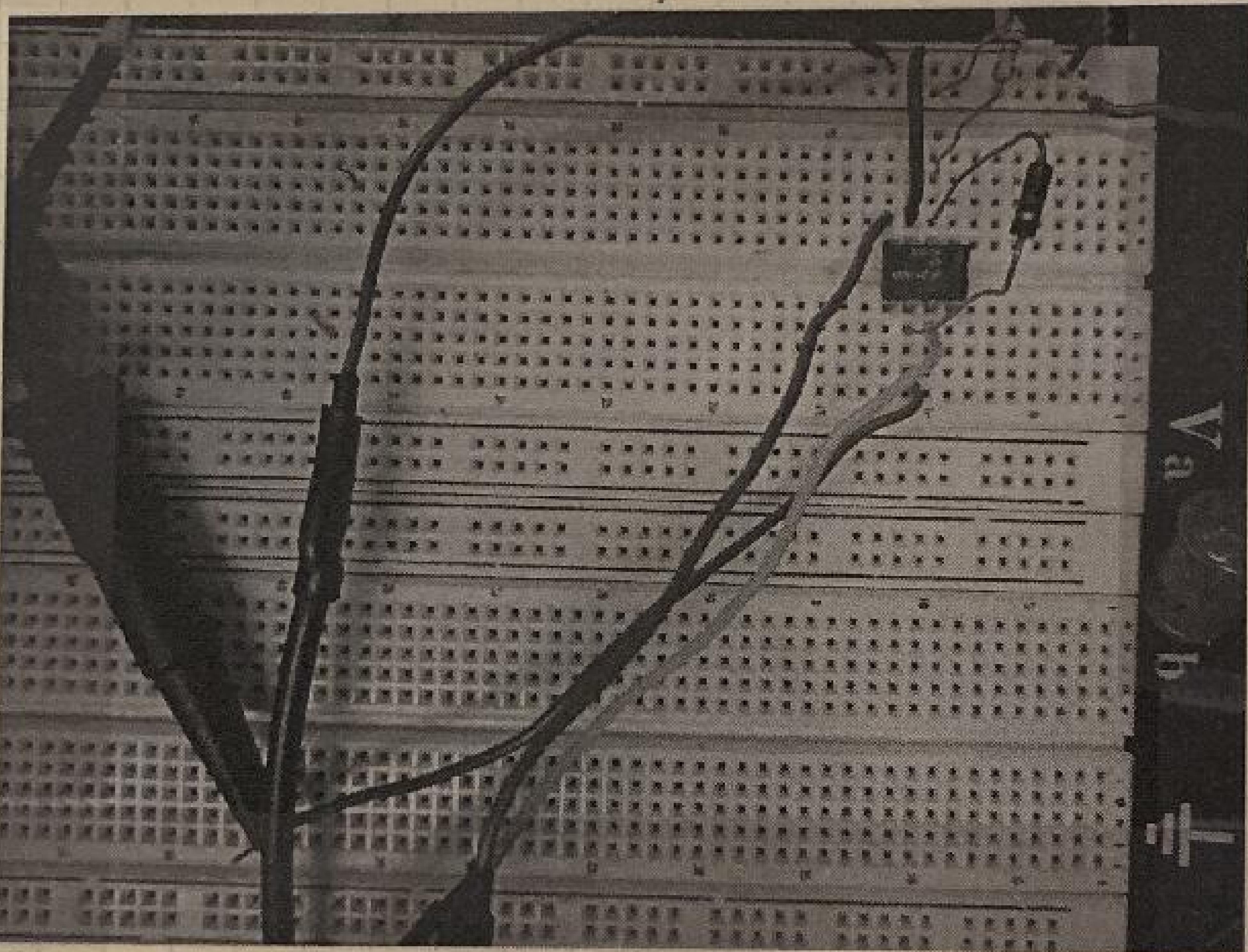


Figure 6-2: Implementation circuit of Op-amp Configuration A.

After taking samples of the output voltage in order to calculate gain at different input frequencies, we generated the table shown below.

Vin (V)	Vout (V)	Gain (V/V)	Frequency (Hz)
0.99	-2.1072	-2.12848	0
1	-2.05	-2.05	10
1	-2.02	-2.02	100
1	-2.04	-2.04	500
1	-2.02	-2.02	1000
1	-2.08	-2.08	5000
1	-2.06	-2.06	10000
1	-2.08	-2.08	15000
1	-1.54	-1.54	100000
1	-1.04	-1.04	150000
1	-0.8	-0.8	200000
1	-0.36	-0.36	500000
1	-0.22	-0.22	1000000
1	-0.12	-0.12	2000000
1	-0.1	-0.1	3000000

Tables
go on top

Table 6-1: Data gathered from Op-amp Configuration A at frequencies ranging from 0Hz to 3 MHz.

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To get a visual representation of this data, we generated a gain magnitude vs. frequency plot in Excel. Because of the large range of values, the plot is on a log scale.

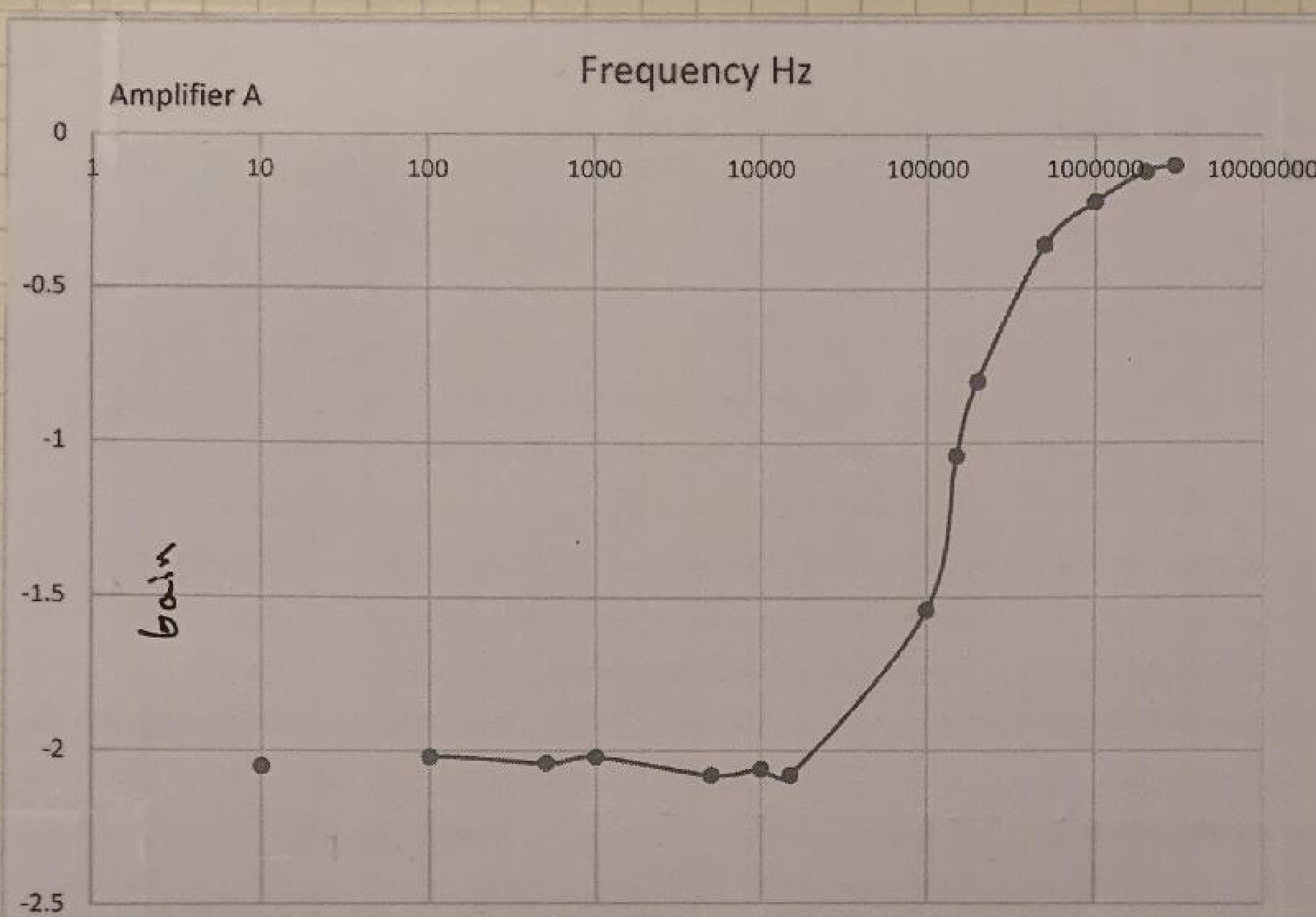


Figure 7-1: Gain Magnitude vs. Frequency plot (log scale) for Op-Amp configuration A. X-axis: Frequency (Hz), Y-axis: Gain .

As you can see, the expected gain value was present for about half of the samples. Around an input frequency of 100 kHz is when gain begins to decrease. It keeps ~~decreasing~~ decreasing as frequency grows, and nearly reaches a value of zero when our sampling ends.

We calculated the 3dB ~~at low~~ small signal bandwidth for this circuit to be 333 kHz, which lines up fairly well with our plot. Some small discrepancies exist, but these are to be expected as not every Op-Amp is perfect and the resistors are $\pm 10\%$.

Gain Magnitude vs. Frequency for Configuration B:
 The circuit for configuration B is as follows:

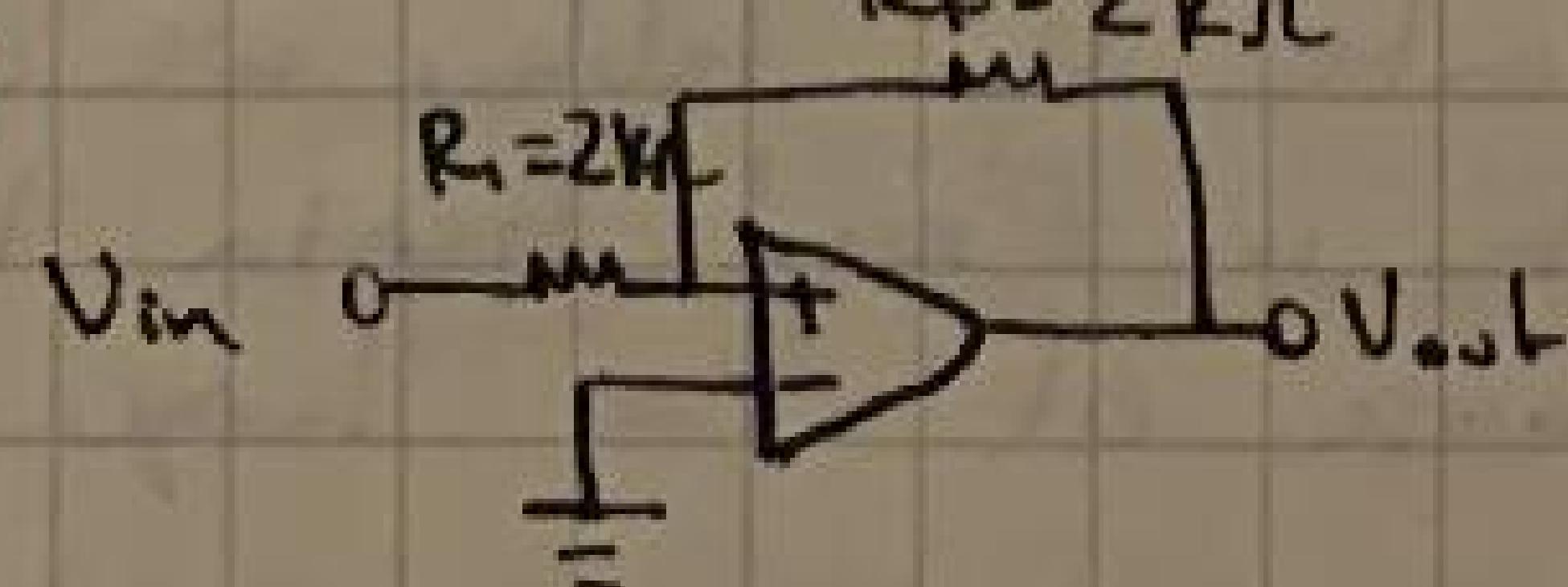


Figure 7-2: Non-inverting Op Amp configuration with gain of +2.

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We implemented the circuit on our breadboard and took the following picture to document it:

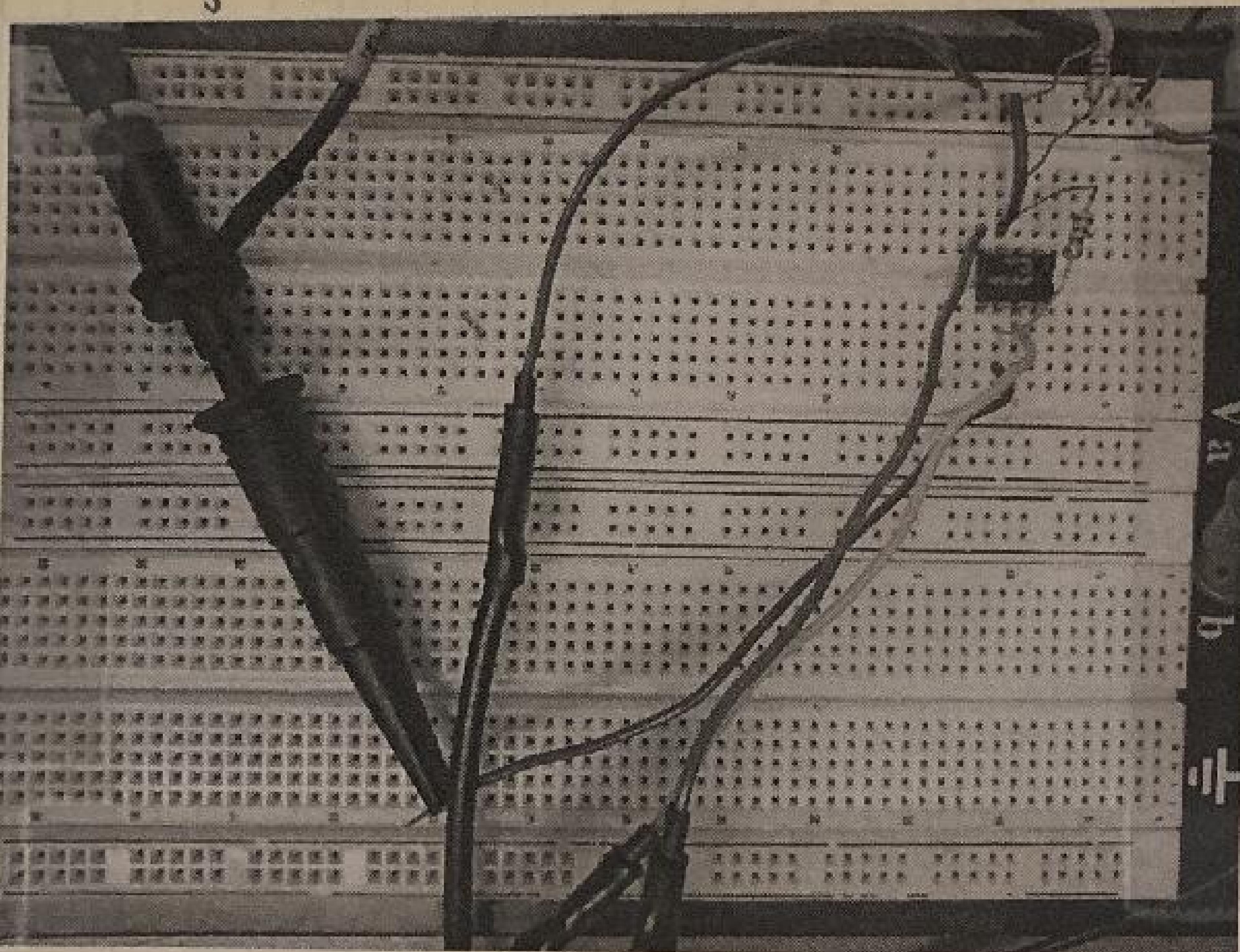


Figure 8-1: Implementation of circuit for Op-Amp configuration B.

Again, we took samples of V_{out} in order to calculate the gain at different frequencies. All of this data was gathered and entered into the table below.

V_{in} [V]	V_{out} [V]	Gain (V/V)	Frequency [Hz]
1	2.0084	2.0084	0
1	2.04	2.04	10
1	2.04	2.04	50
1	2.04	2.04	100
1	2.04	2.04	500
1	2.04	2.04	1000
1	2.08	2.08	10000
1	2.04	2.04	50000
1	1.96	1.96	70000
1	1.84	1.84	80000
1	1.72	1.72	90000
1	1.64	1.64	95000
1	1.56	1.56	100000
1	0.78	0.78	200000
1	0.3	0.3	500000
1	0.148	0.148	1000000
1	0.054	0.054	3000000

Table 8-1: data gathered from Op-amp configuration B at frequencies ranging from 0 to 3 MHz.

After this data was gathered into the table, we created a gain-magnitude vs. frequency plot in Excel. Again this plot was on a log scale because of the large range of frequencies.

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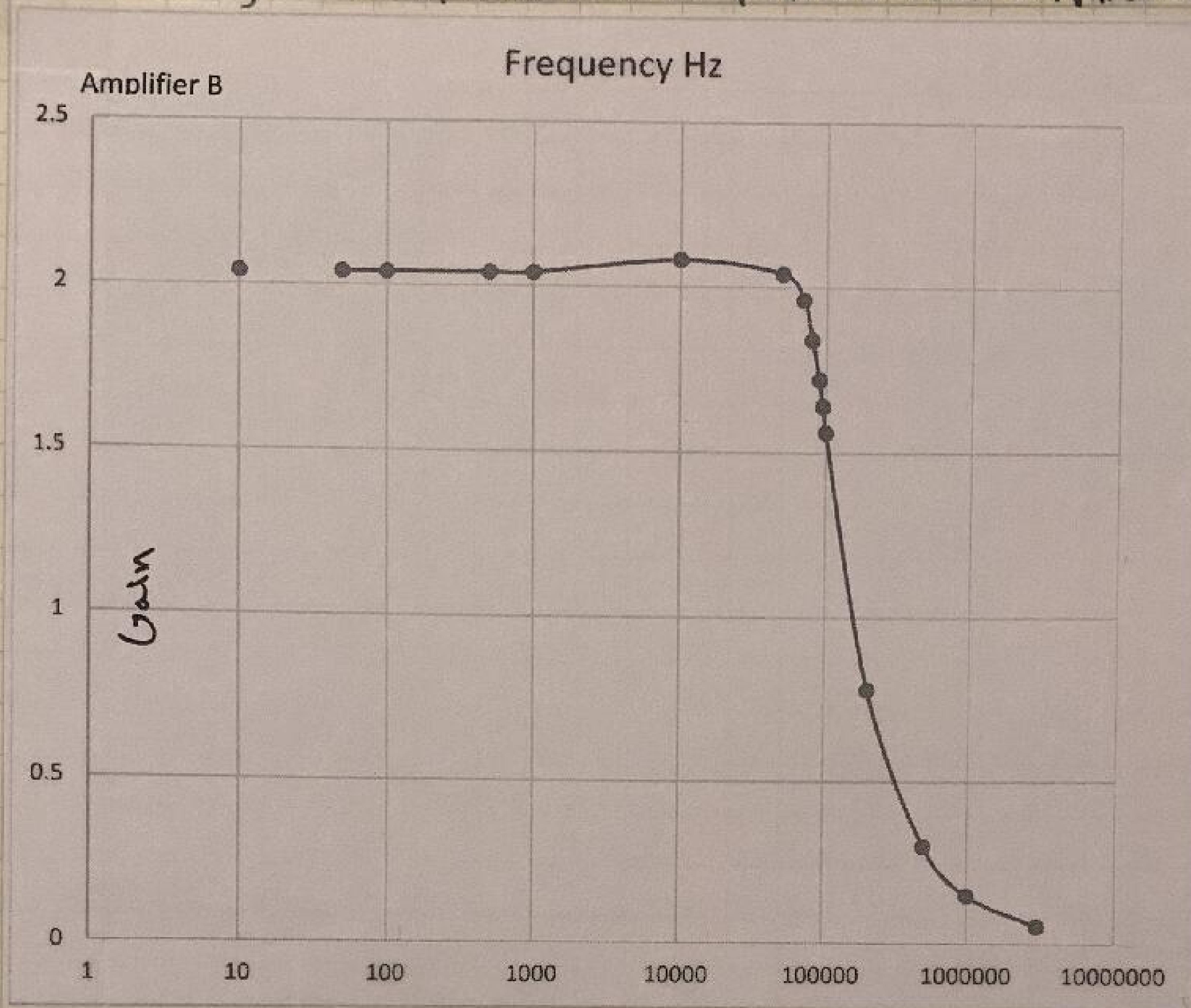


Figure 9-1: Gain-Magnitude plot for op-amp configuration B.

This plot shows pretty much the same shape as the plot for configuration ~~B~~ A, only inverted Gain (which is to be expected). The expected gain of +2 is present until around a frequency of 100 kHz and then gain begins to drop off.

Again, by the time the input frequency is 3 MHz, the gain is nearly zero. This is expected because 3 MHz is too high of a frequency for the op-amp to perform reliably.

Gain-Magnitude vs. Frequency for configuration C:

The circuit for op-amp configuration ~~B~~ C is the following:

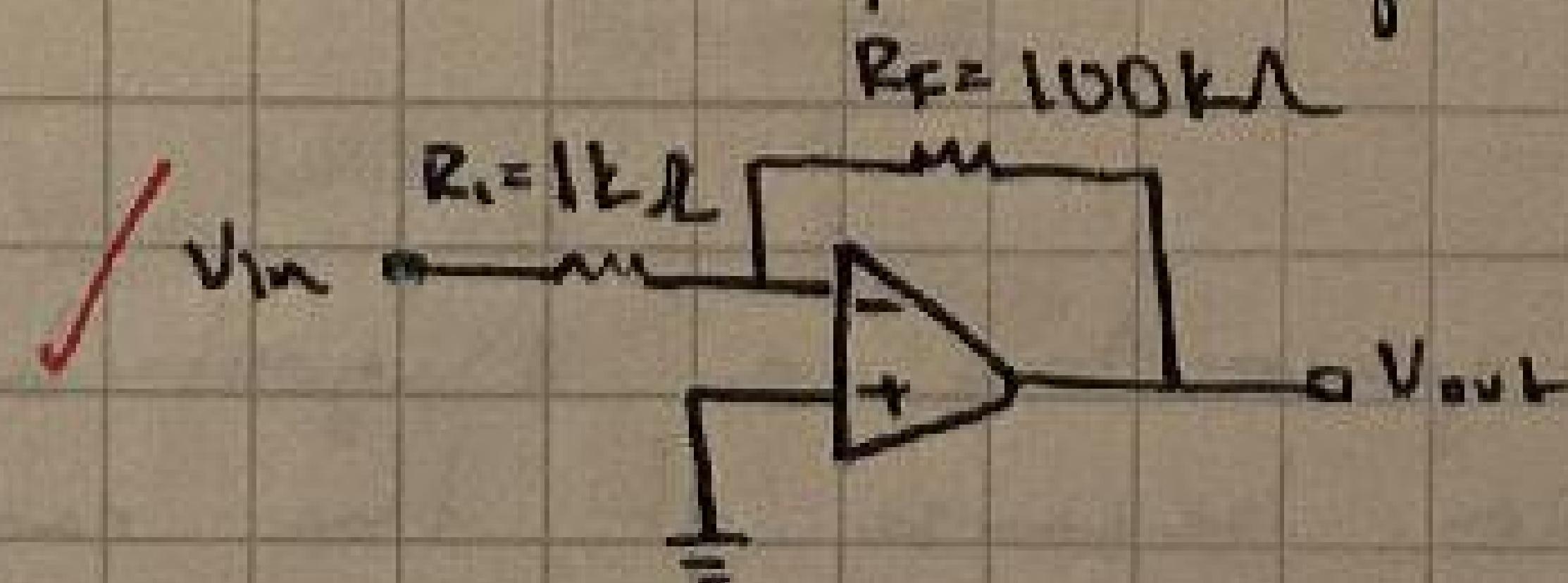


Figure 9-2: Inverting Op-Amp configuration ~~B~~ C with a gain of -100.

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This was implemented on the breadboard just as the other circuits were. A picture has again been included

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Brandon L
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To show our setup:

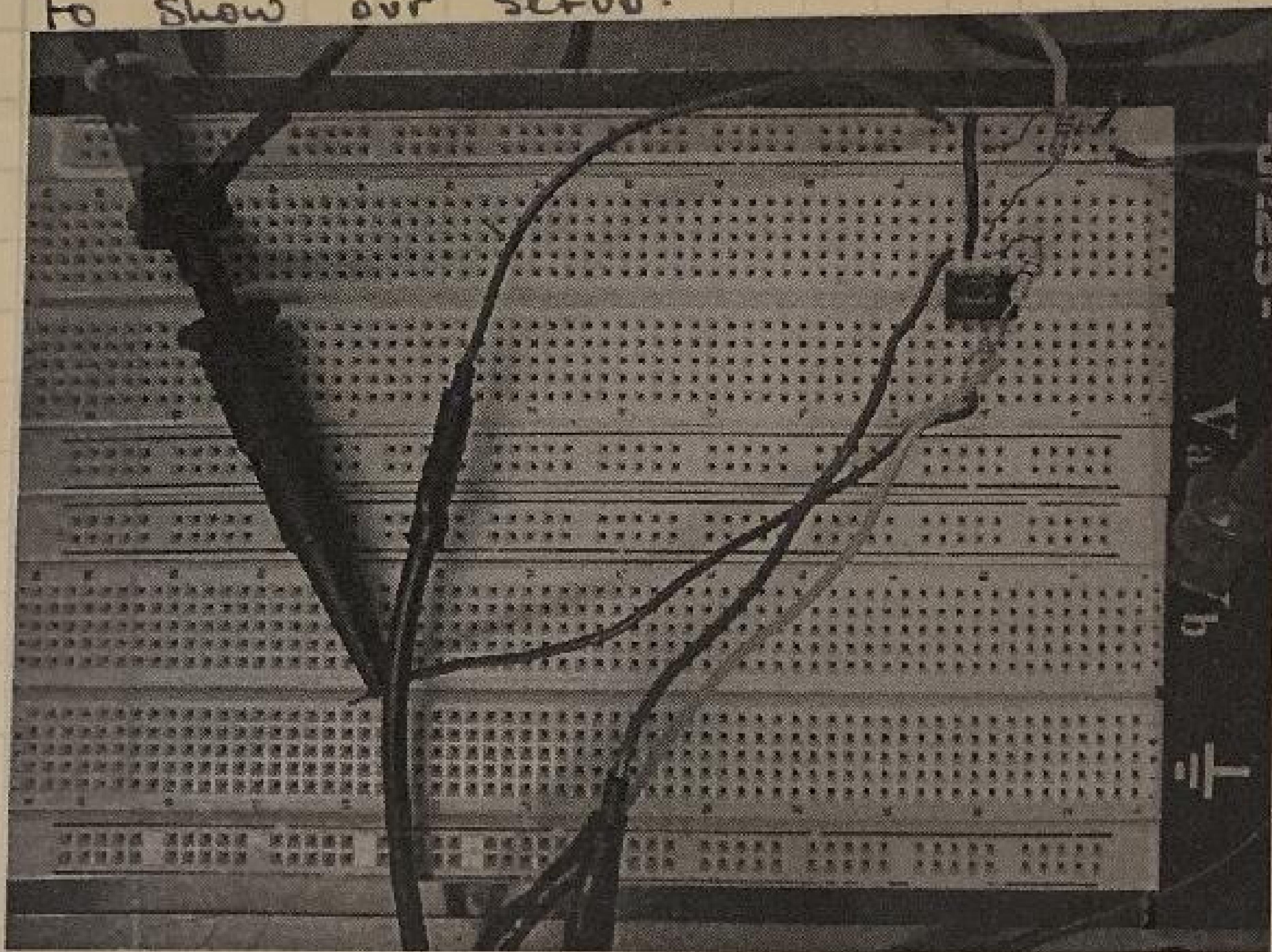


Figure 10-1: Implementation of circuit for op-amp configuration C.

Samples of V_{out} were taken at increasing frequencies for V_{in} . Gain was calculated, and all data was recorded in table 10-1.

V_{in} (V)	V_{out} (V)	Gain (V/V)	Frequency (Hz)
0.005	-5.139	-1027.8	0
0.01	-1.1	-110	10
0.01	-1.1	-110	50
0.01	-1.1	-110	100
0.01	-1.1	-110	500
0.01	-1.1	-110	1000
0.01	-1	-100	5000
0.01	-0.78	-78	10000
0.01	-0.4	-40	25000
0.01	-0.22	-22	50000
0.01	-0.16	-16	70000
0.01	-0.14	-14	80000
0.01	-0.13	-13	90000
0.01	-0.12	-12	95000
0.01	-0.116	-11.6	100000
0.01	-0.06	-6	200000
0.01	-0.03	-3	500000
0.01	-0.026	-2.6	1000000
0.01	-0.01	-1	3000000

Table 10-1: Data gathered for op-amp configuration C for V_{in} frequencies ranging from 0 to 3 MHz.

Using this data, we generated a magnitude-gain vs. frequency plot. Again, because of the range and distribution of frequencies, a log scale was used.

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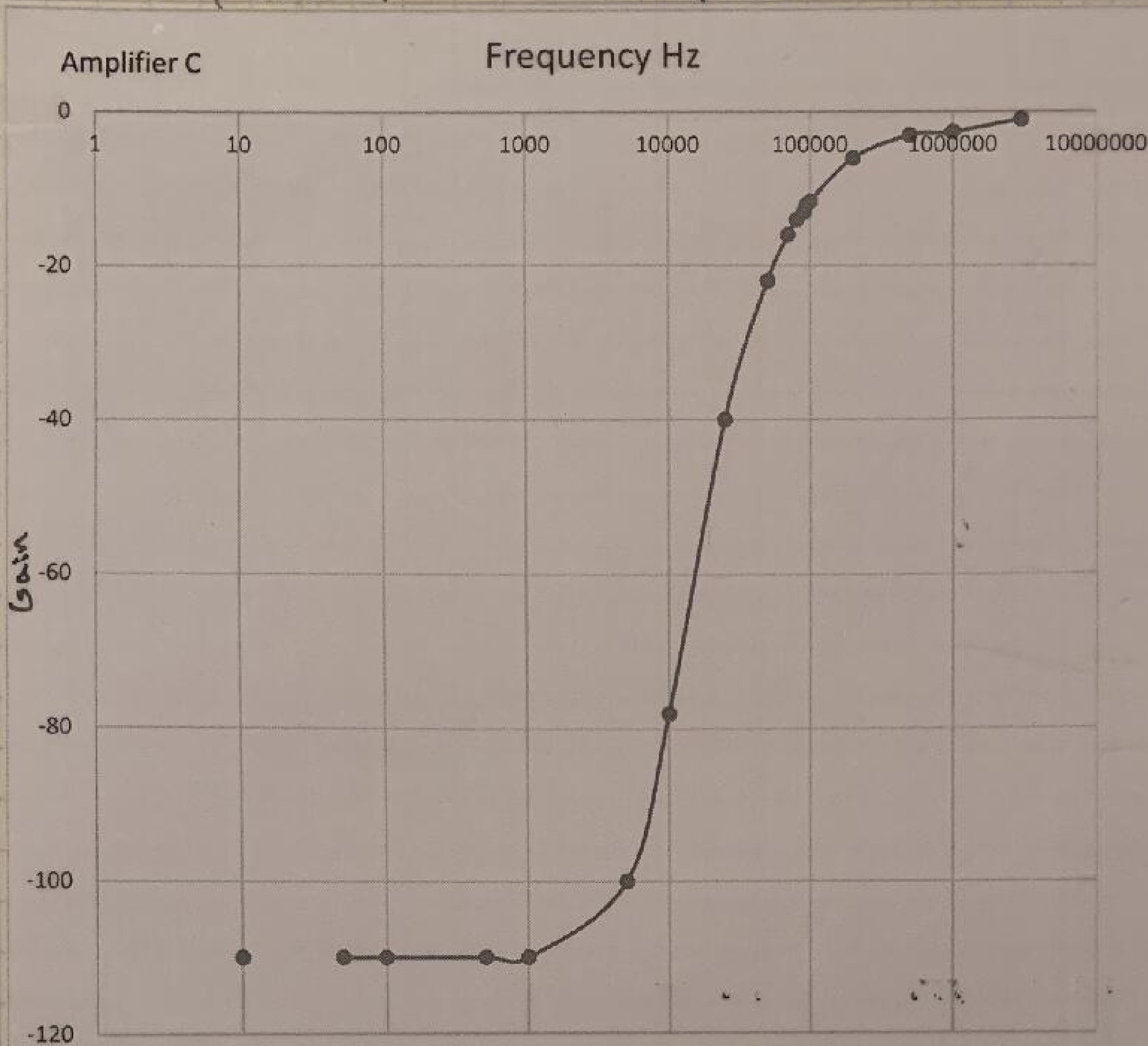


Figure 11-1: Magnitude-gain vs. Frequency plot for op-amp configuration C (log scale).

As expected, the shape of this plot is similar to the one for configuration A because they are both inverting. Gain begins to waiver near the 1kHz range which is much sooner than the other two. This is because the higher the gain, the lower the frequency at which performance begins to falter. With a gain of -100, this setup begins failing much sooner than the previous two.

Gain Magnitude vs. Frequency for Configuration D:

The circuit for op-amp configuration D is as follows:

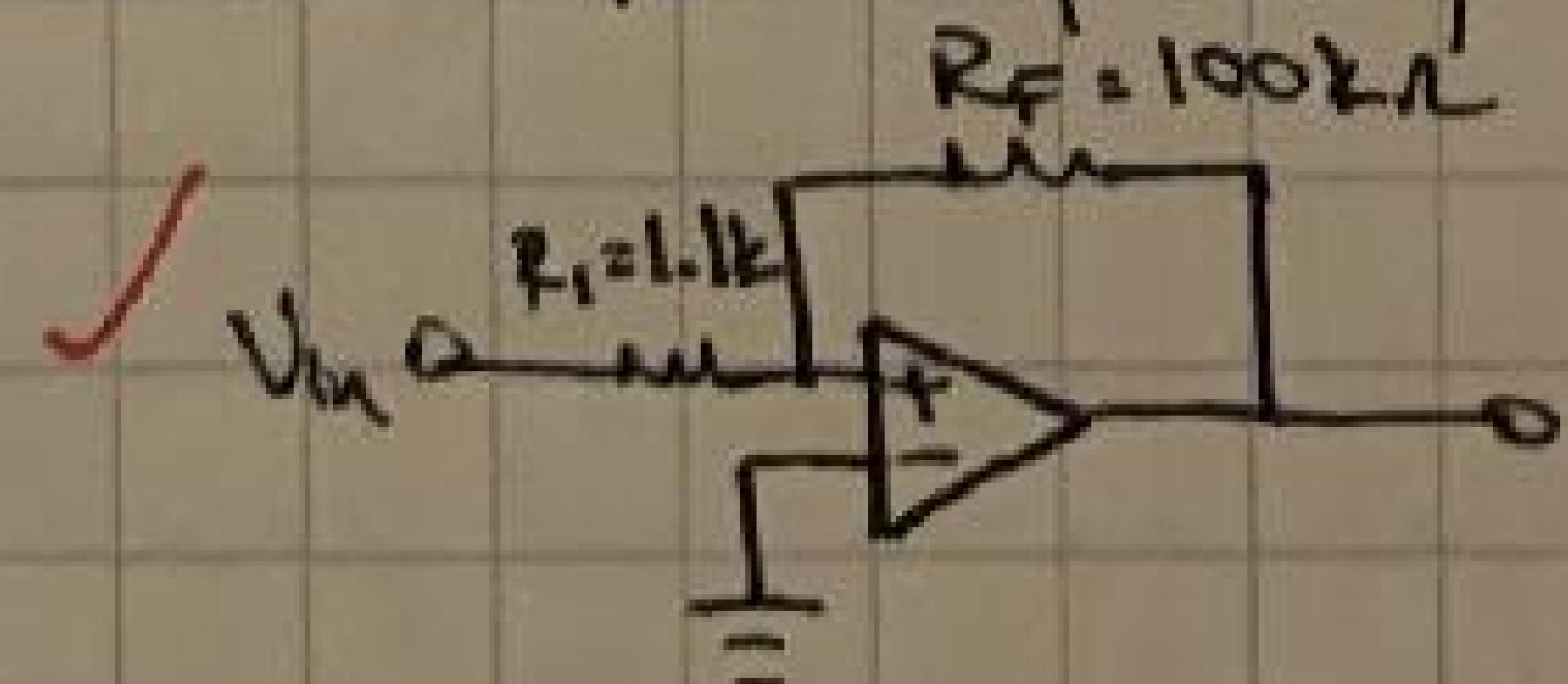


Figure 11-2: Non-Inverting Op-amp configuration for a gain of +100.

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3:44 PM A picture is included on the next page showing our implementation.

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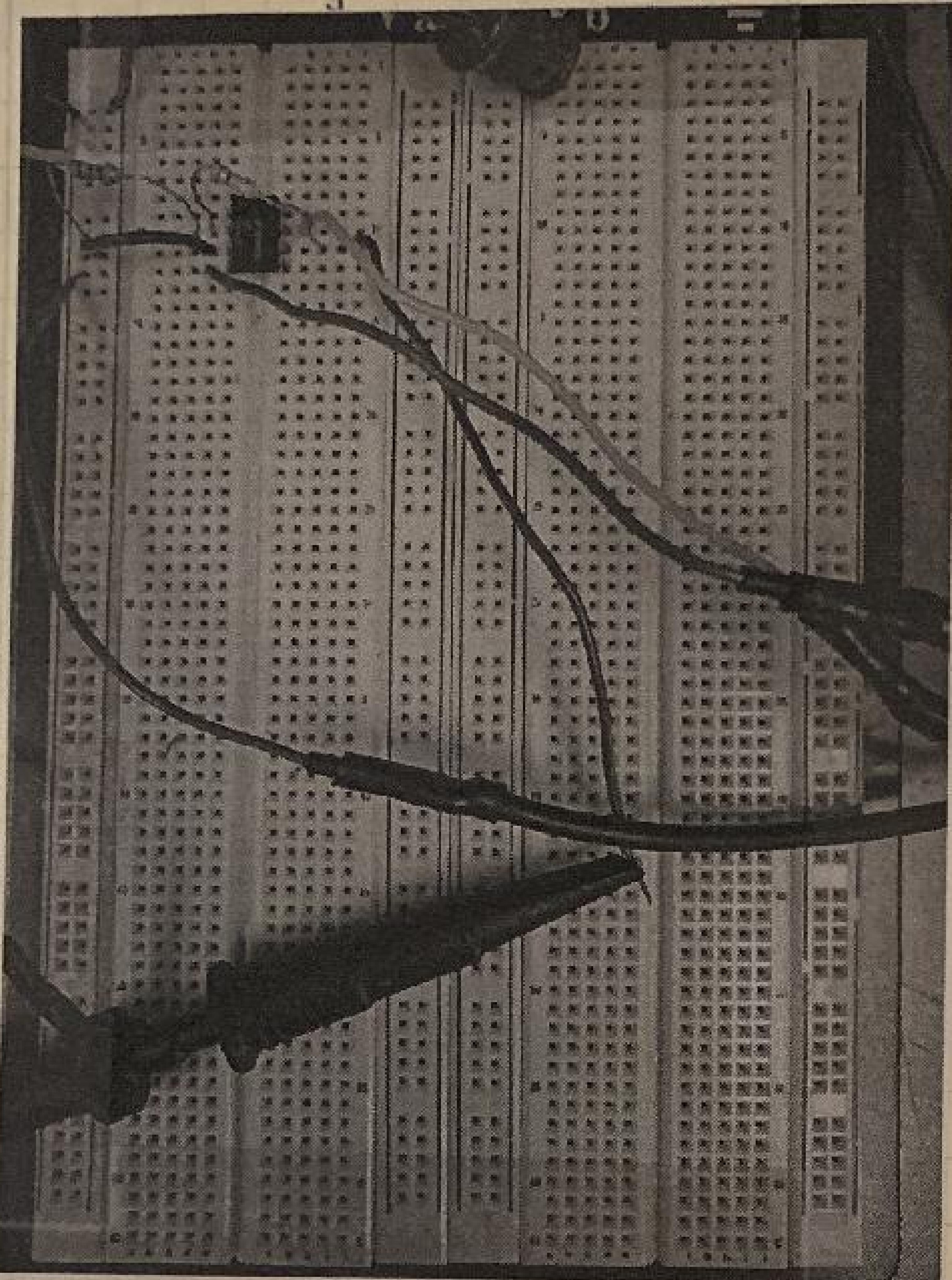


Figure 12-1: Implementation of op-amp configuration D.

Samples of V_{out} were taken at different frequencies of V_{in} in order to calculate gain. This data was recorded and placed into the table below:

V_{in} (V)	V_{out} (V)	Gain (V/V)	Frequency (Hz)
0.005	4.745	949	0
0.01	1.06	106	10
0.01	1.06	106	100
0.01	1.06	106	800
0.01	1.06	106	1000
0.01	1.04	104	3000
0.01	1	100	4000
0.01	0.98	98	5000
0.01	0.86	86	8000
0.01	0.78	78	10000
0.01	0.12	12	100000
0.01	0.064	6.4	200000
0.01	0.034	3.4	500000
0.01	0.027	2.7	1000000
0.01	0.011	1.1	3000000

✓

Table 12-1: Data gathered for op-amp configuration D for V_{in} frequencies ranging from 0 to 3 MHz.

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3:45pm We generated a gain Magnitude vs. frequency plot with this data and set it to log scale.

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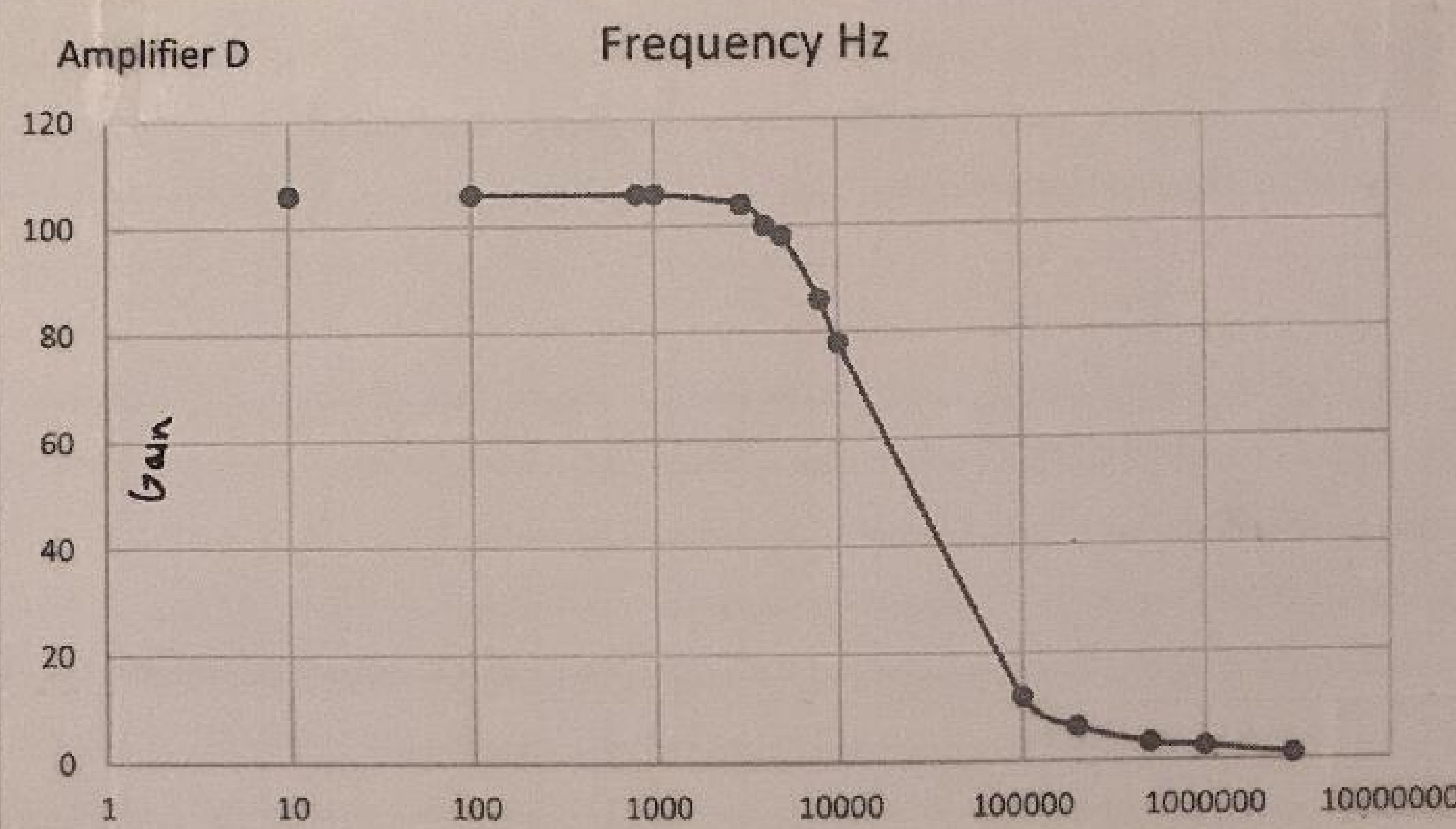


Figure 13-1: Gain - Magnitude vs. Frequency plot (log scale) for op-amp configuration D.

This plot takes on a general shape similar to that of the one generated for op-amp configuration B. This makes sense because they are both non-inverting configurations. One difference between these is the slope in the transition band of these plots. The slope in configuration B is much greater than the slope for D. This is most likely because of the differences in gain for each configuration. It appears that with a configuration that has a larger gain, the slope in this section of the plot will be lesser than that of one with a lower gain. This could be because the increase in input frequency has a damped effect due to the increased impedance of the feedback resistor R_F .

Gain for this configuration appeared to drop off much sooner than the other non-inverting configuration. Just after the 1 kHz frequency, gain begins to decrease. This is due to the initial gain being 100, causing later gains to continuously decrease as frequency of the input increases.

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2. The process for measuring the input resistance of inverting and non-inverting amplifier configurations is simple, but several things must be taken into account.

The first thing to consider is the natural resistance of the DMM. This is important because for one of the configurations we will be dealing with values that are very small, and for the

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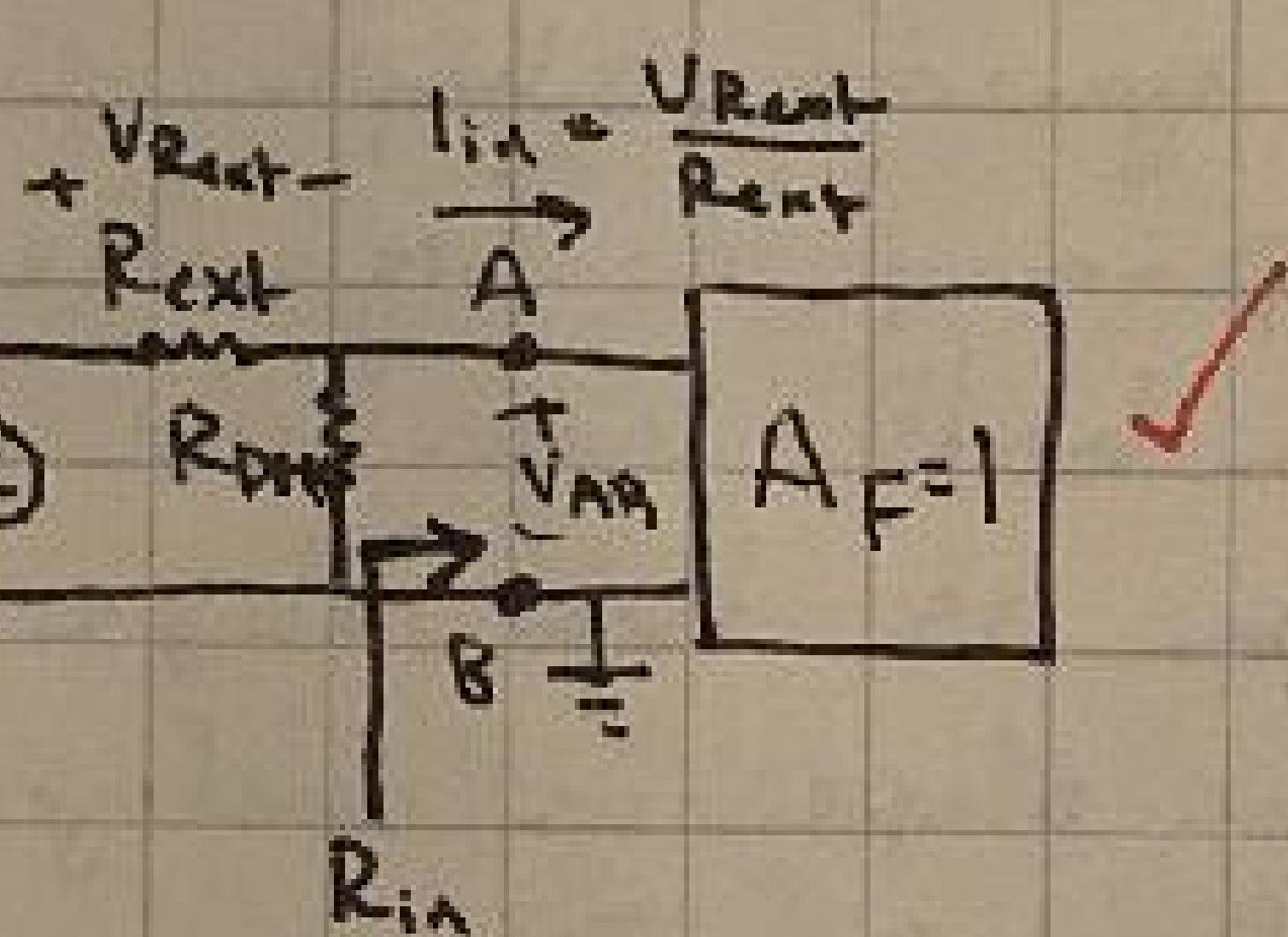
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Brandon L
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other, very large. Since the tool used to measure many of the values necessary for this calculation will be the DMM, we will need to take its resistance into consideration. This value is about $10\text{ M}\Omega$.

Another thing to consider is the expected input resistance for each configuration. This is important because it will determine the value for the external resistor we use during measurement. For an inverting configuration, an expected input resistance is zero (ideal) or a very very small value. Because of this, an external resistor will need to be a very large value (around $20\text{ M}\Omega$). For a non-inverting op-amp, an expected input resistance is infinity (ideal) or very large. This means that a small external resistor will need to be used (around $2\text{ k}\Omega$).

The circuit used to measure input resistance is as follows:

Figure 14-1: Circuit for measuring input resistance of inverting and non-inverting operational amplifier configurations.



The basic procedure for measuring the input resistance is as follows:

1. Set V_s to a 1V DC signal.
2. Measure the voltage across the external resistor.
3. Calculate I_{in} using V_{ext} and R_{ext}
4. Calculate R_{in} using Ohm's Law.

good.

We first calculated the input resistance for a non-inverting op-amp. We measured the voltage across R_{ext} to be $.002$ volts.

This leads to an input current I_{in} of $\frac{V_{ext}}{R_{ext}} = \frac{.002}{20000} = .0000001\text{ A} = 1 \times 10^{-7}\text{ A}$
 In this calculation, R_{ext} is essentially just the resistance of the ~~resistor~~ external resistor.
 Using $V=1\text{V}$, $\frac{V_{in}}{I_{in}} = R_{in} = 10\text{ M}\Omega$ → This value is consistent with what we expected. Although ideally this value should be infinite, this is obviously not realistic in a lab setting.

QA

9/20/18 For the inverting use, we measured the voltage across R_{ext} to be .99V.
 4:30 PM From this, we can calculate an input current I_{in} of → (continued on next pg)

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$$I_{in} = \frac{V_{out}}{R_{out}} = \frac{.99V}{R_{out} \parallel R_{load}} = \frac{.99V}{6.6 \times 10^6} = 1.5 \times 10^{-7} A$$

Using $V=IR$, we can calculate R_{in} : *Should be whatever your R_1 is!*

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{(1-I_{in})} = \frac{.99V}{(1-1.5 \times 10^{-7})A} = 0.99 \Omega \rightarrow \text{This value is consistent with what we expected. Ideally, it should have been a value of zero but that is not realistic in a lab setting.}$$

3. For this part, we began by setting the signal generator to the following:

- 1 kHz frequency
- 2 V peak-to-peak
- 5 V DC offset

Since we already had the inverting configuration set up on the breadboard, we began with that circuit. We attached the positive end of the signal generator output to the red rail of the breadboard, and the negative end to the blue rail, sharing a common ground with two oscilloscope probe grounds, and the ground from the DC PSU used for V_{in} and V_{cc} inputs to the op amp. Channel 1 on the oscilloscope was attached to the input in order to show V_{in} , and channel 2 was attached to the circuit output. The input and output signals for this configuration were captured.

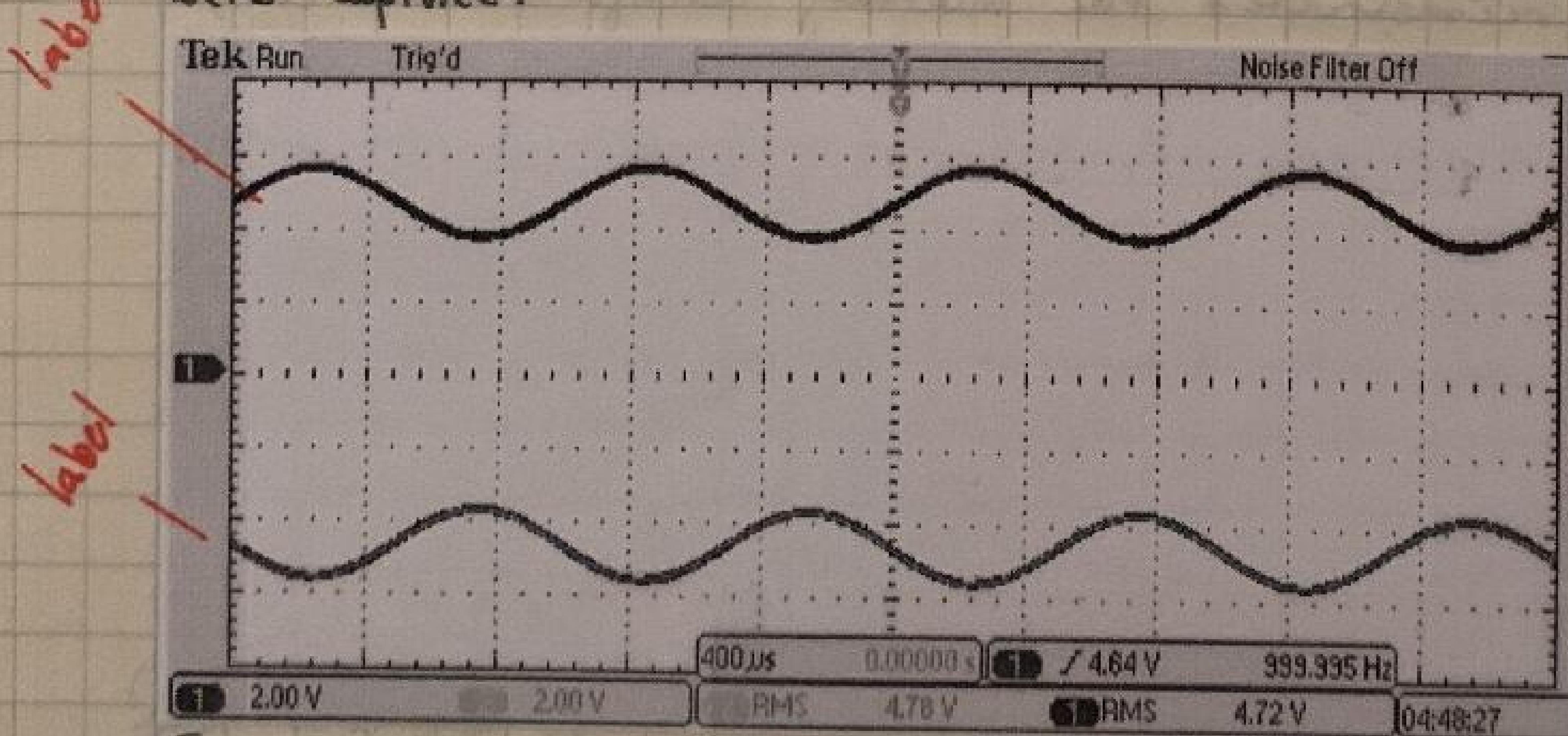


Figure 15-1: Input (ch1) and output (ch2) signals of an inverting op-amp circuit with $V_{in} = \sin(2\pi 1000t) + 5$.

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The image above was what we expected. Channel 1 showed the sinusoidal input with the vertical shift of +5 from the DC offset, while channel 2 showed the same signal mirrored over the x-axis (due to the inverting configuration).

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- good job
Explaining the
labels,
however
you should
put them
on the
Figure for
Simplicity

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Next we reconfigured the circuit for the non-inverting case. Channels 1 and 2 remained connected to the input and output signals respectively. The result was captured on the oscilloscope.

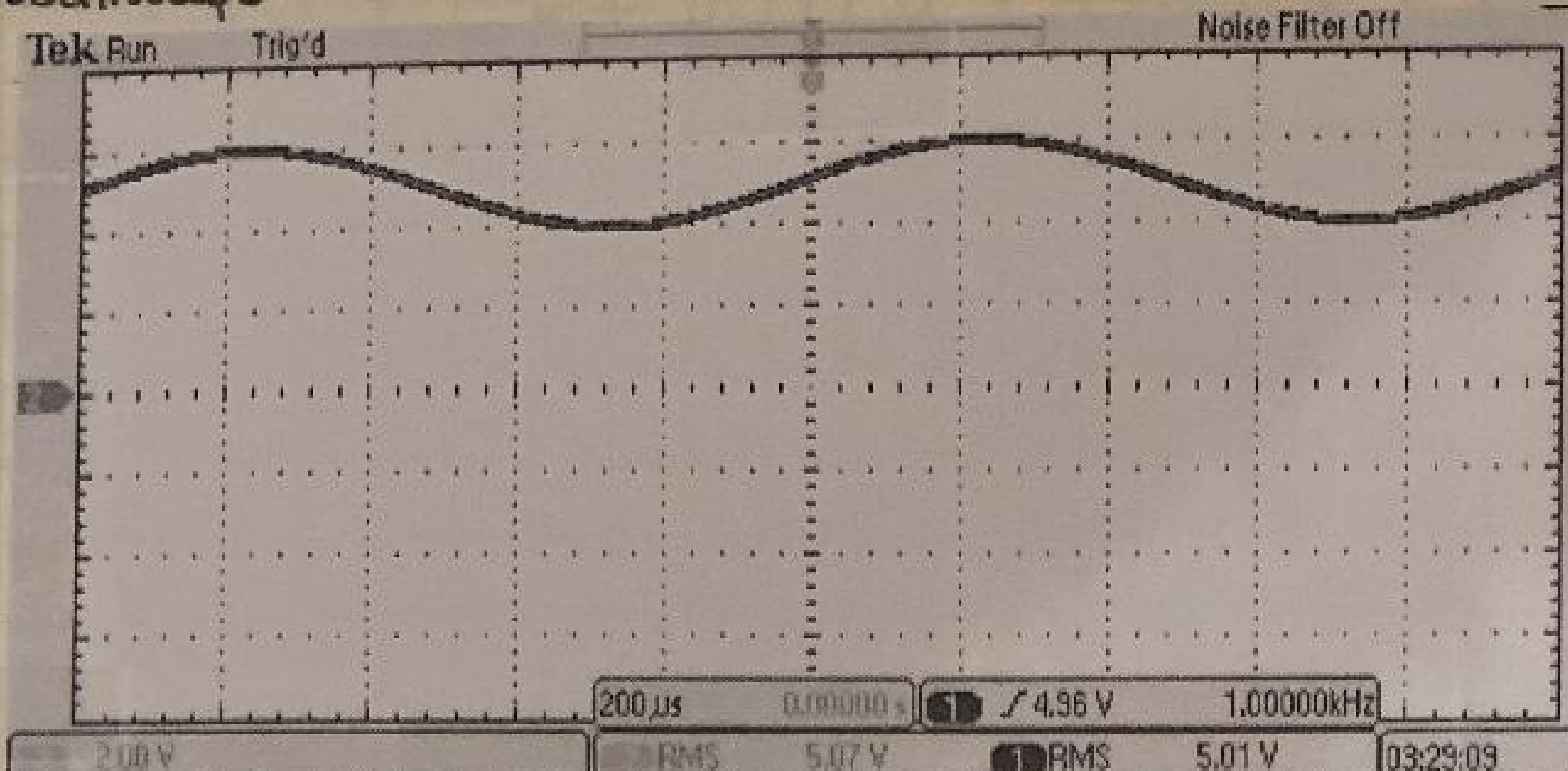


Figure 16-1: Input (Ch1) and output (Ch2) signals of ~~an~~ a non-inverting OP-amp circuit with an input $V_{in} = \sin(2000t) + 5$.

At first glance this may look like one single signal, however it is both input and output signals overlapping because of the gain of +1. These signals are what we expected to see, both having a frequency of 1000Hz, 2V peak-to-peak voltage, and vertical shifts of +5 V.

After this, we reconstructed the inverting configuration circuit, this time with 0.1μF non-electrolytic capacitors at the op amp inputs to block out the DC component of the input signal.

Initially what we saw on the scope was pretty much what we had seen earlier (shown in Figure 15-1), however, soon the output signal began to drop and flatten. The following two figures show this behavior in action:

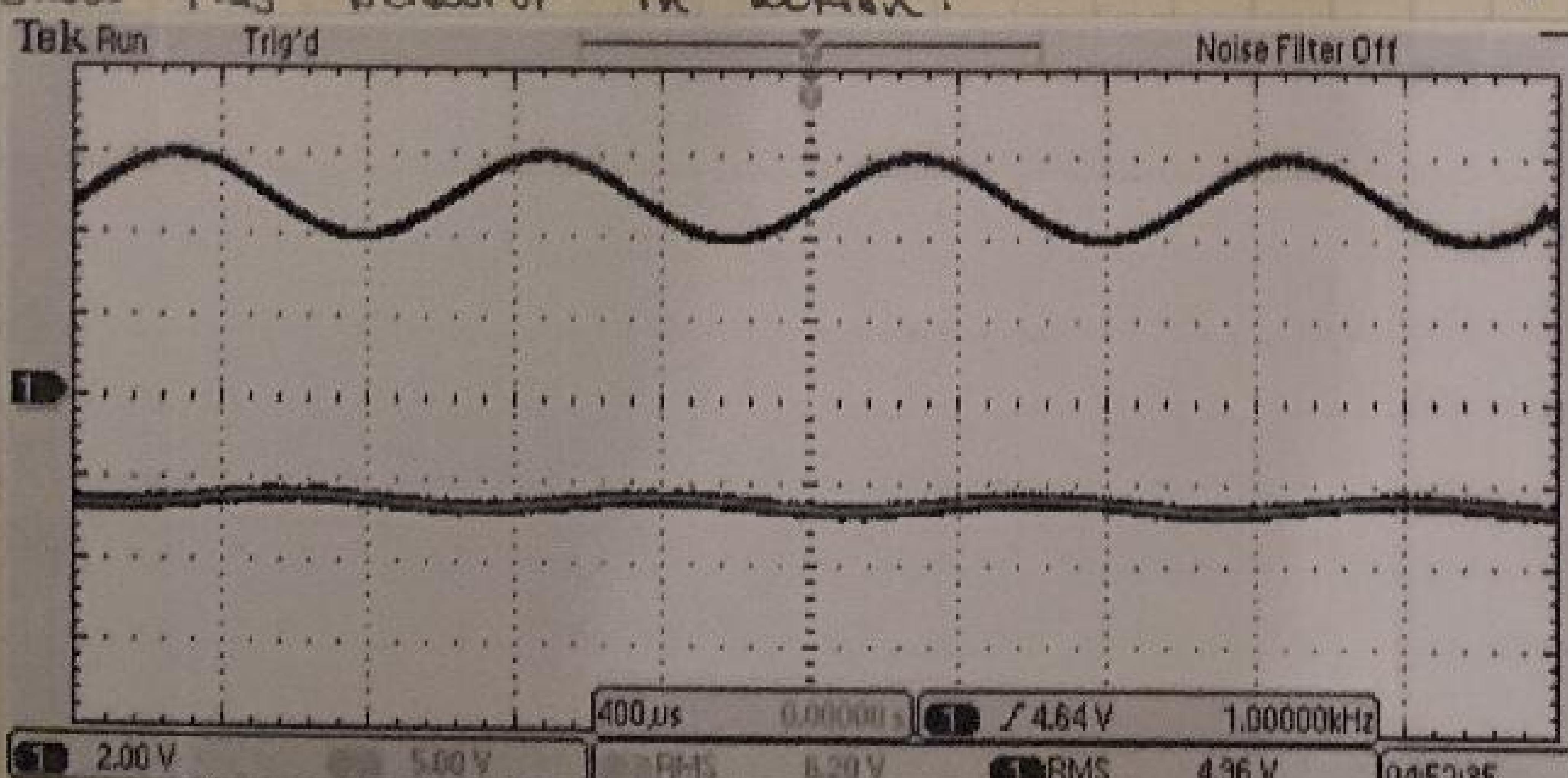


Figure 16-2: Input (Ch1) and output (Ch2) signals of an inverting OP-amp circuit with an input $V_{in} = \sin(2000t) + 5$, and 0.1μF non-electrolytic capacitors placed at the inputs. In this capture, output is decreasing and flattening.

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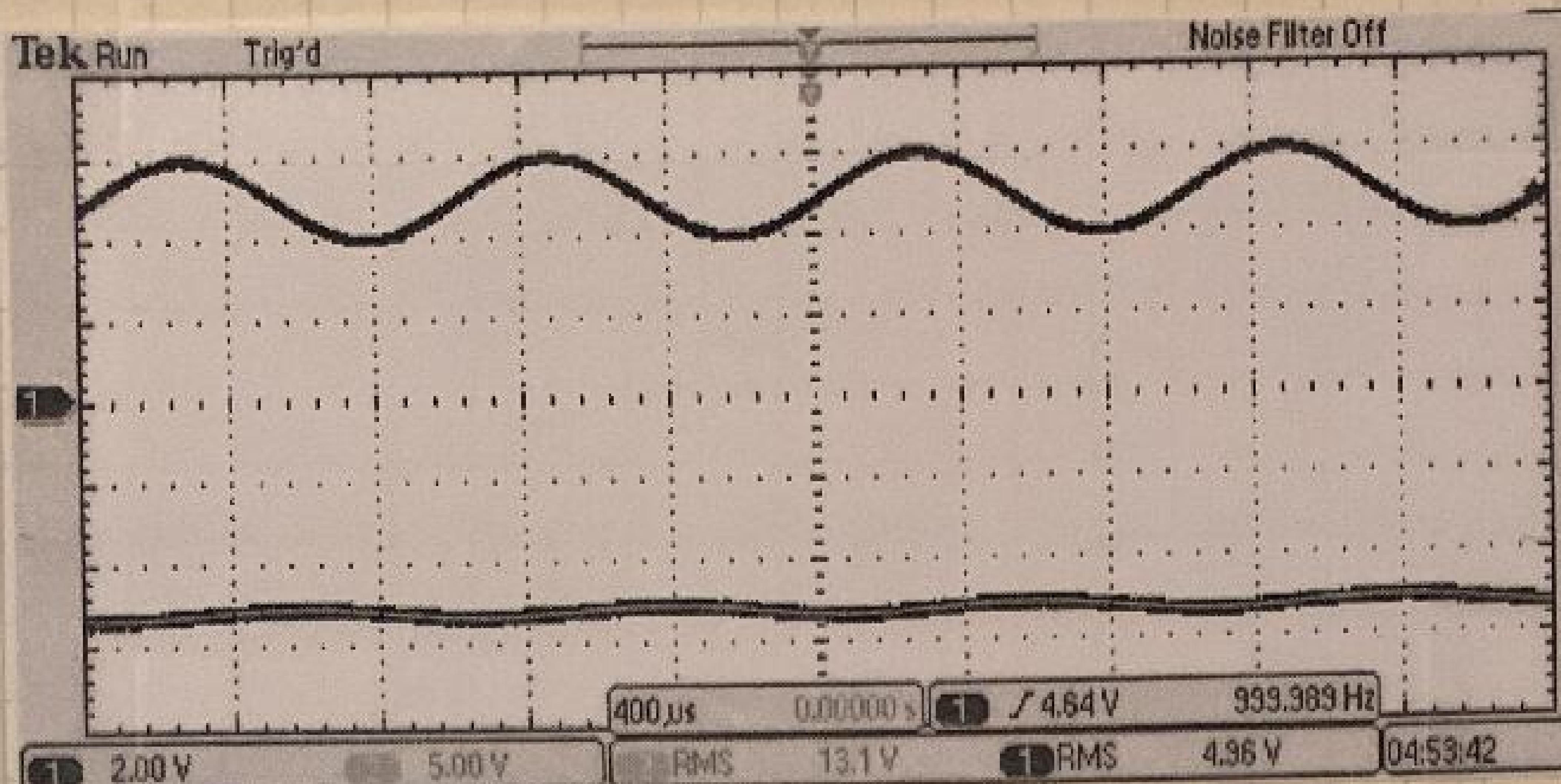
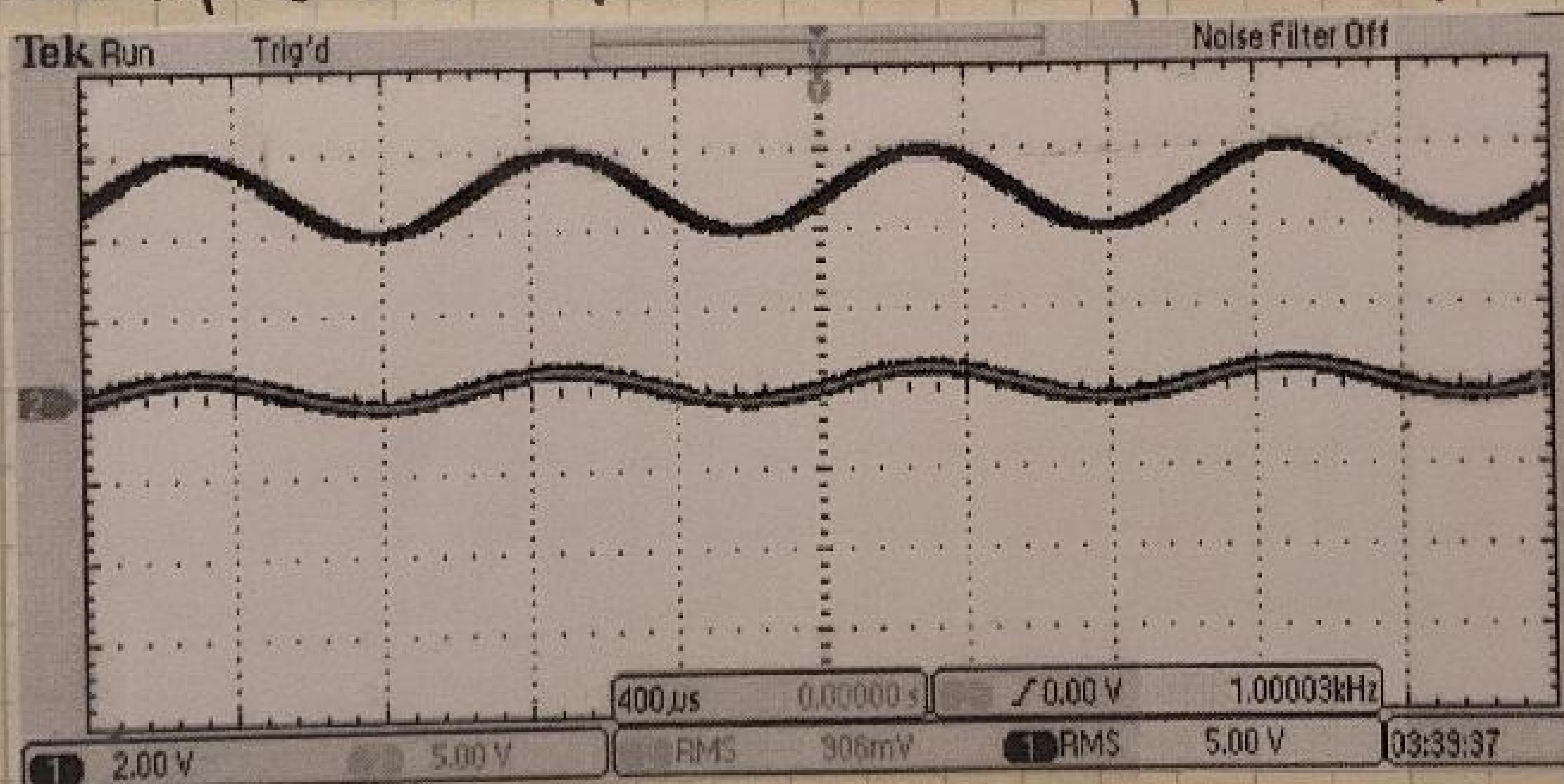


Figure 17-1: Input (ch1) and output (ch2) signals of an inverting op-amp circuit with an input $V_{in} = \sin(200\pi t) \cdot 5$ and $0.1\text{ }\mu\text{F}$ non-electrolytic capacitors placed at the inputs. In this capture output has stabilized.

Similarly, we configured the non-inverting op-amp circuit on our breadboard with $0.1\text{ }\mu\text{F}$ non-electrolytic capacitors placed at the two inputs and captured the following oscilloscope readings:



No Circuit Schematic?
- I "

Figure 17-2: Input (ch1) and output (ch2) signals of a non-inverting op-amp circuit with an input $V_{in} = \sin(200\pi t) \cdot 5$ and $0.1\text{ }\mu\text{F}$ non-electrolytic capacitors placed at the inputs. In this capture, output is decreasing and flattening.

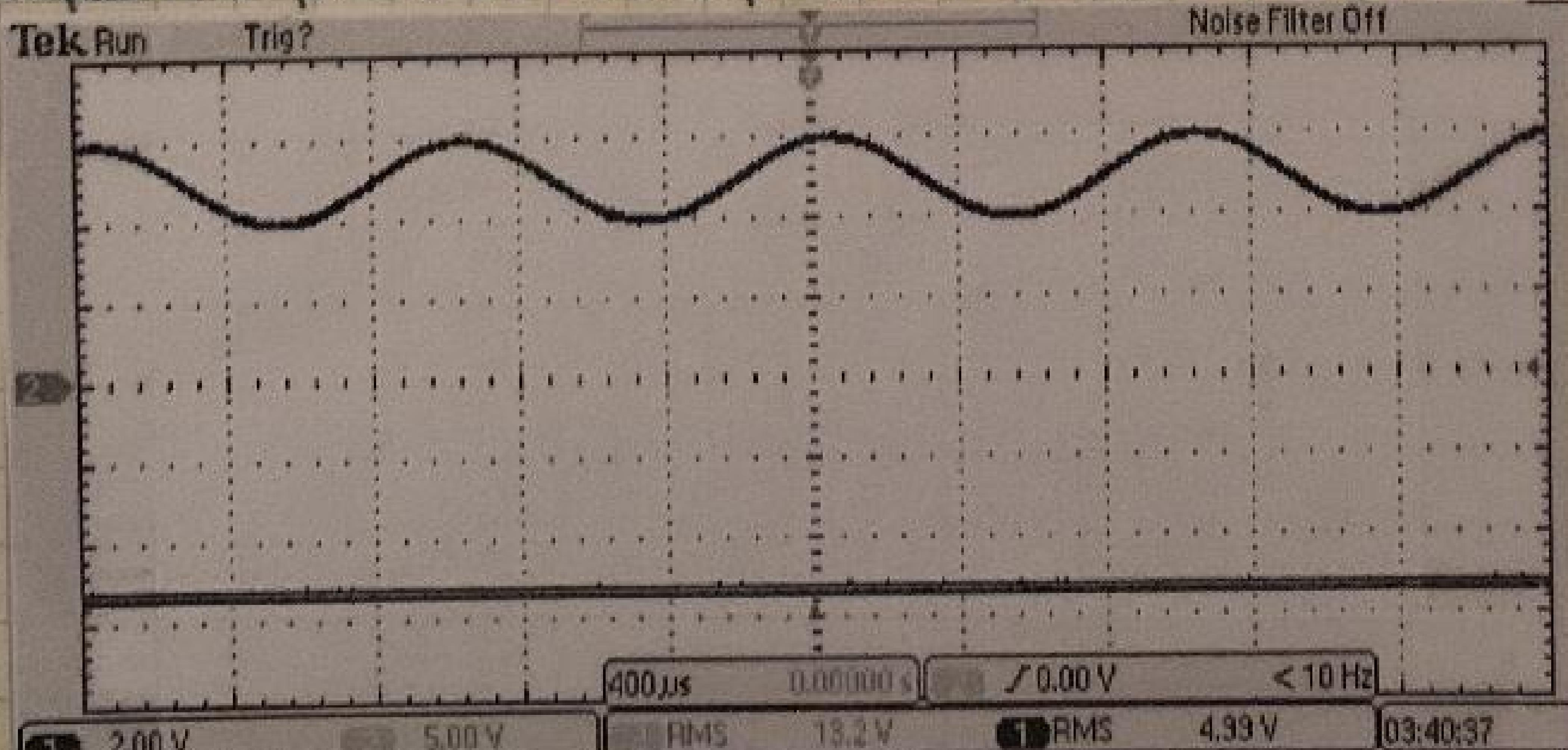


Figure 17-3: Input (ch1) and output (ch2) signals of a non-inverting op-amp circuit with $0.1\text{ }\mu\text{F}$ capacitors placed at the inputs. In this capture, output has stabilized.

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Laboratory #3: Operational Amplifiers and Applications

Grant Abeler
Brandon L
9/25/18

The reason why this odd output occurs for both configurations is because the capacitors being placed at the op-amp inputs keeps the voltage level at a high enough value each time feedback occurs that output voltage keeps rising (or decreasing) until saturation is reached (~ 13.5 V).

This occurrence takes time to reach saturation, which is why the output shifts vertically over time.

4. In order to rectify an AC signal, we first constructed the following circuit:

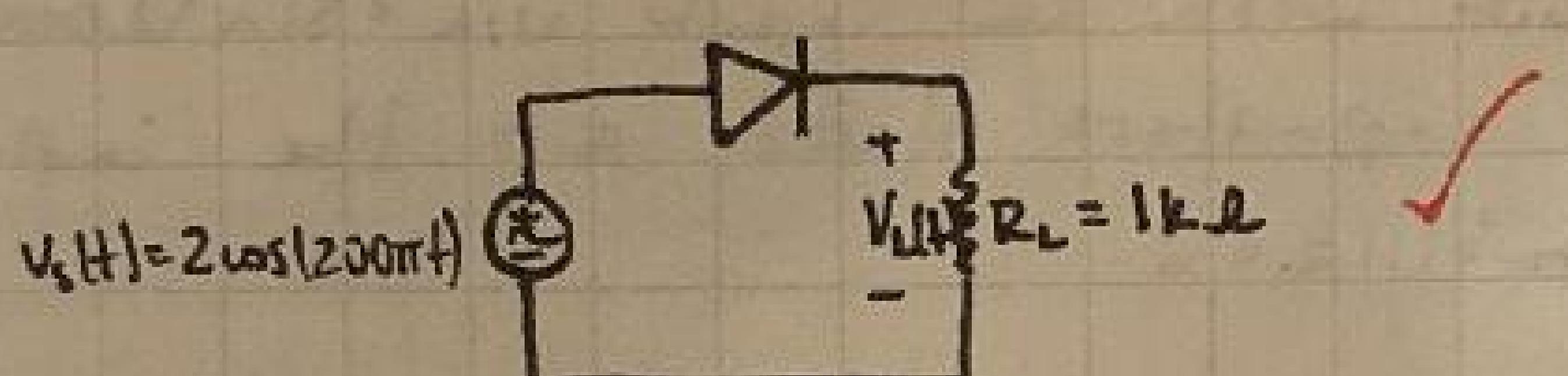


Figure 18-1: AC signal rectifier circuit with diode and no op-amp.

We implemented the circuit above and attached channel 1 of the scope to the source V_s (which was generated by the signal generator), and channel 2 to the load resistor R_L .

The following reading was captured on the oscilloscope:

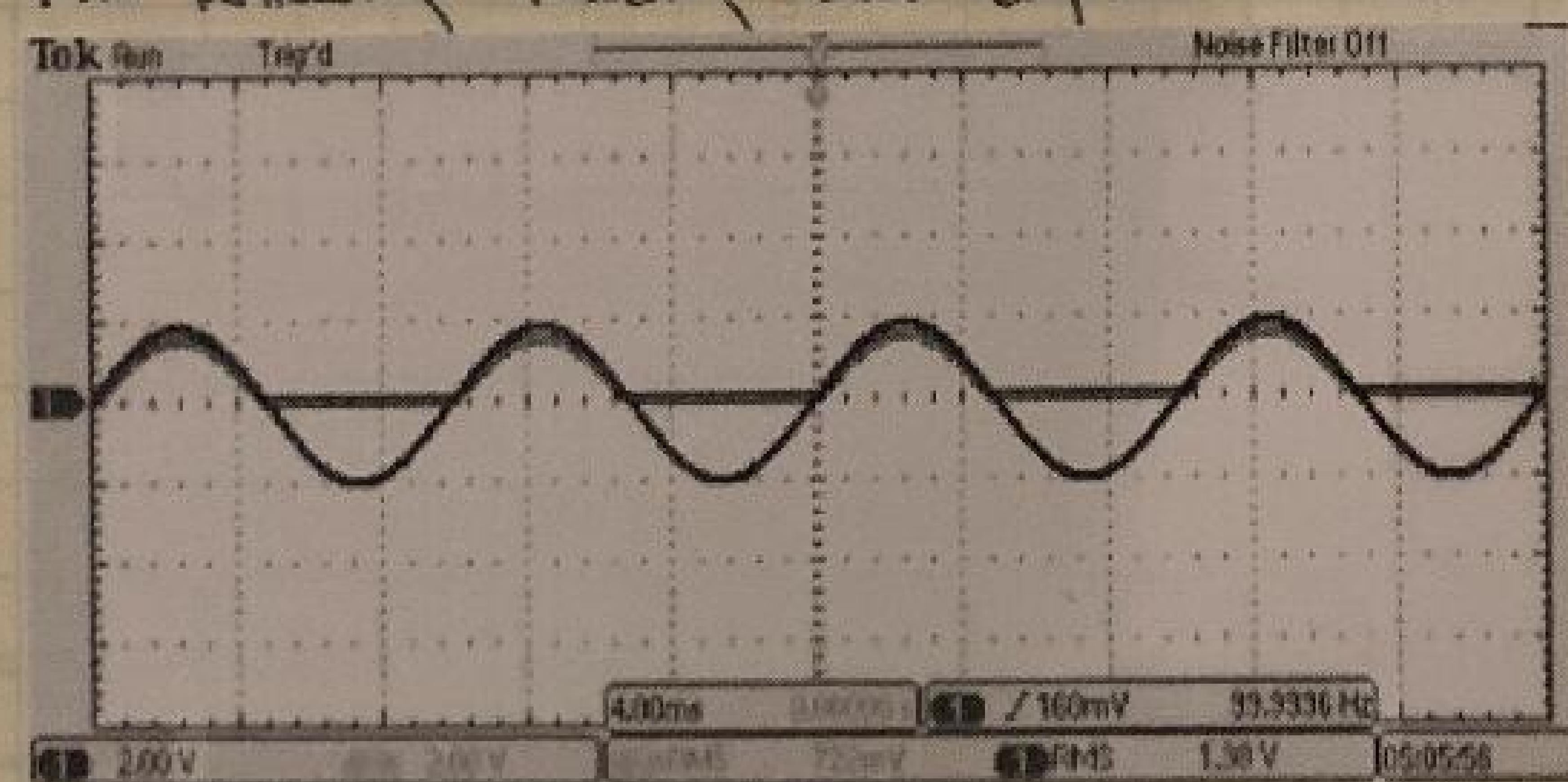


Figure 18-2: Input (ch1) and output (ch2) signals for the circuit in figure 18-1.

For the rectifier circuit, we can see that the output signal is being rectified as no portion of the signal is passing below the x-axis. This is what we expected to see due to the nature of current flow in diode circuits.

After this, we next constructed an AC Rectifier circuit with both an op-amp. The circuit diagram for this set up is shown on the following page.

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Dr

9/25/18

Laboratory #3: Operational Amplifiers and Applications

Graef Blaha
Braxton L
9/25/18

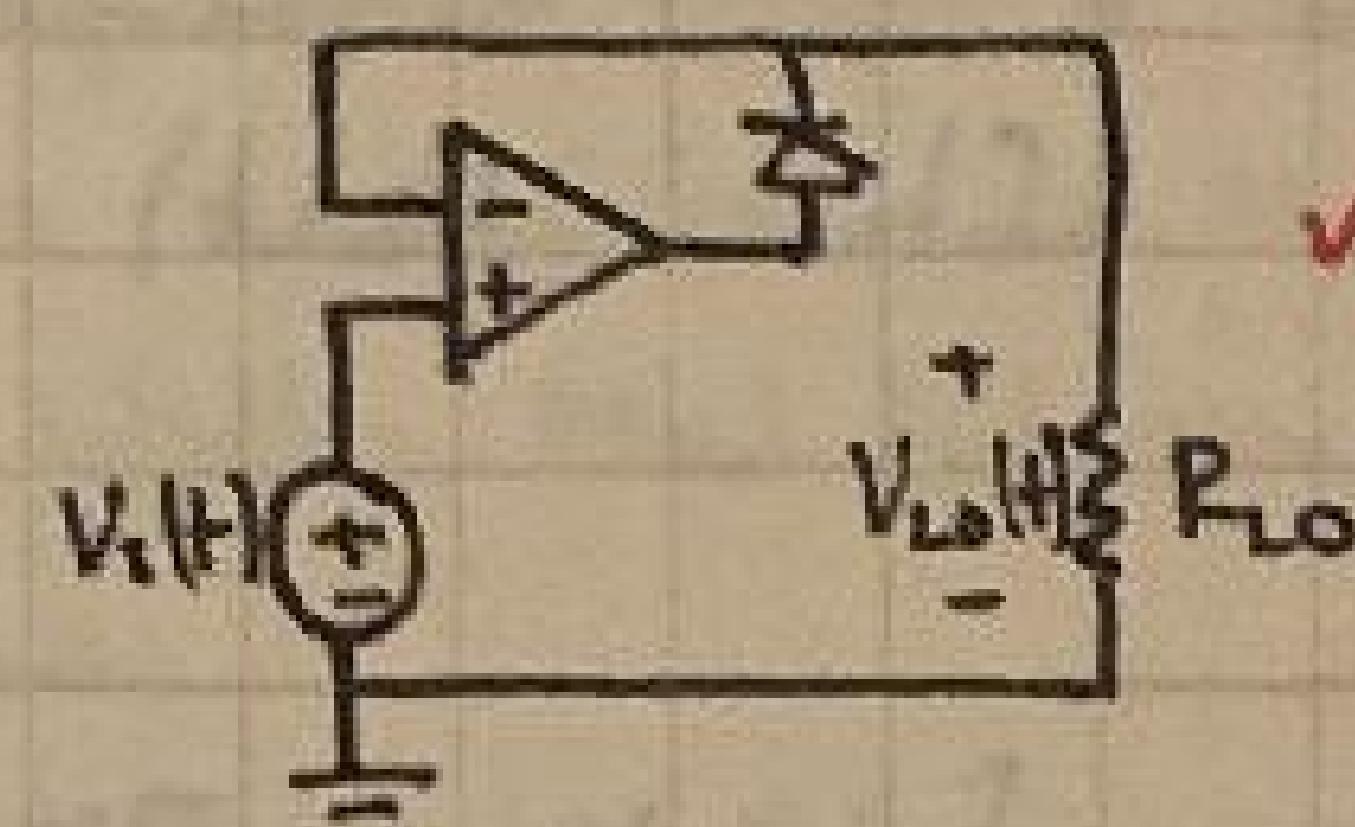


Figure 19-1: AC Rectifier Circuit with diode and op amp.

We implemented this circuit with channel 1 of the oscilloscope attached to the input signal $V_i(t) = 2\cos(200\pi t)$, and channel 2 attached to the output load R_o .

The following reading was captured on the oscilloscope:

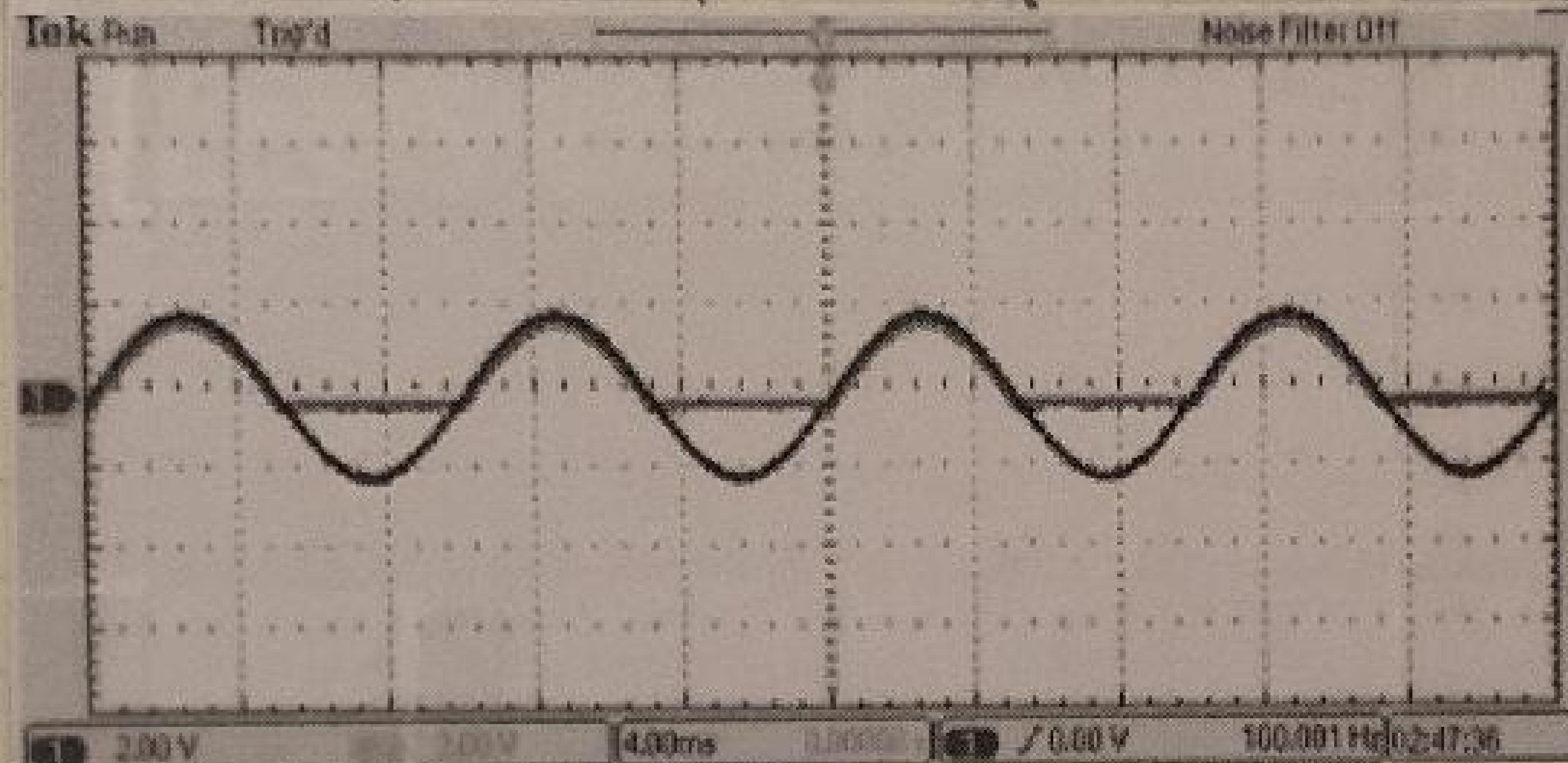
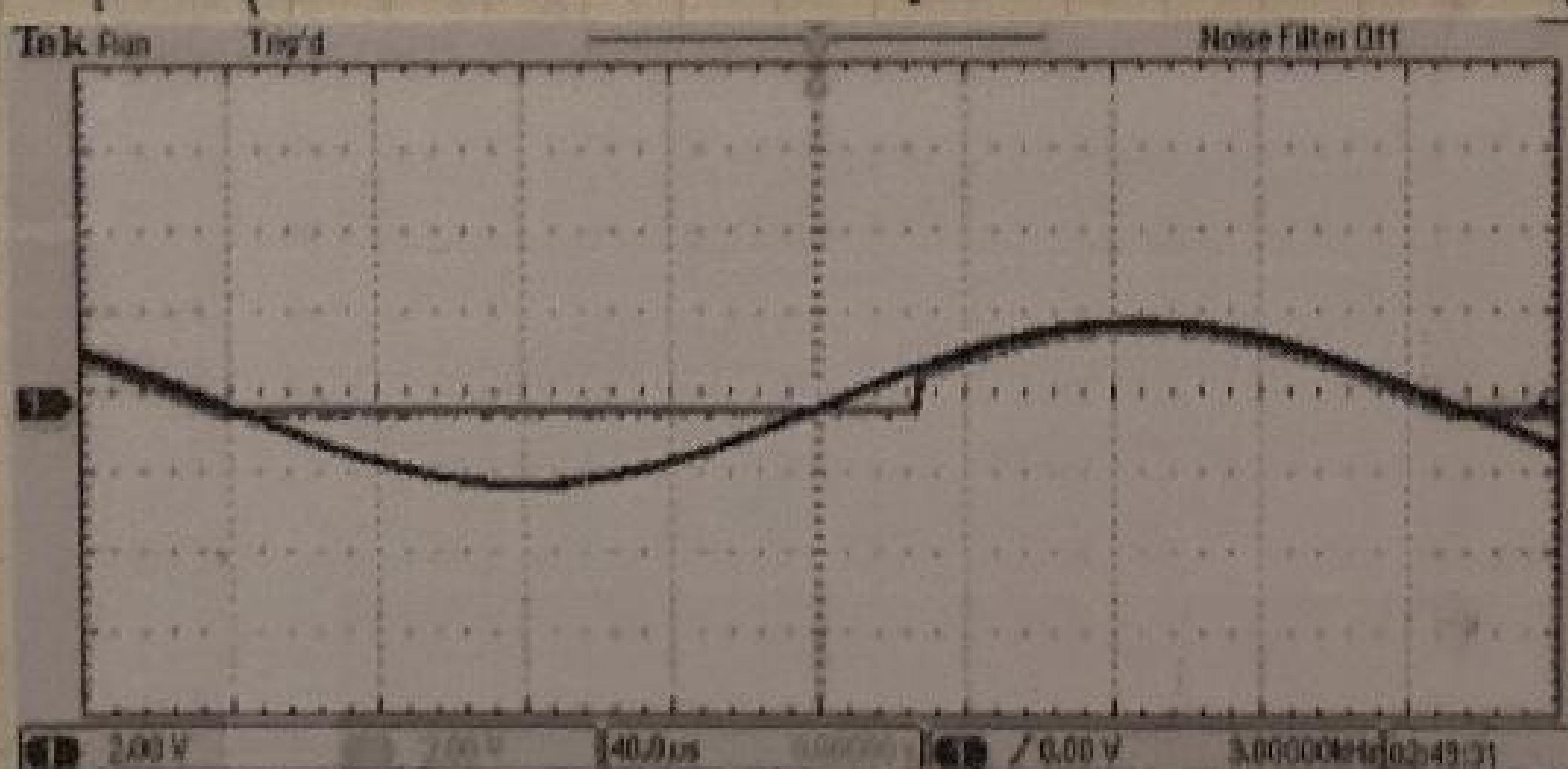


Figure 19-2: Input(ch1) and Output(ch2) signals for the circuit in figure 19-1.

The above capture was what we expected to see, almost identical to the previous rectifier results. The reason for this is because of the way that the current flows after passing through the diode and then to the load resistor R_o .

We were curious to see how the output would behave when the frequency of the input signal was higher, so we increased the frequency to 3kHz and captured the following screenshot on the scope:



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Figure 19-3: Input (ch1) and output (ch2) signals for the circuit in figure 19-1 with frequency of $V_i(t)$ at 3kHz.

Laboratory #3: Operational Amplifiers and Applications.

Grant Allen
Brandon L
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As you can see from the capture, although the output of the circuit is rectified, there is a distinct jump in the output signal a little time after $V_{in(t)}$ changes from negative to positive.

This is a result of the slew rate of the 741 op-amp not being high enough for this circuit to perform as intended when input frequencies are high.

The easiest ways to correct this would be to either utilize a different op-amp with better specifications or to swap the op amp from the circuit entirely and opt instead for the simpler diode circuit shown in figure 18-1.

Conclusion:

In this lab, we tested and viewed the effects of different input frequencies on the gain of both inverting and non-inverting op-amp configurations. Through the gathering of data to create gain-magnitude vs. frequency plots, we created a visual representation of this relationship, and saw the differences in outcome for both configurations.

In addition to this, we also gained more experience in circuit design for a given gain, as well as experience with measuring input resistance for op-amp configurations.

Finally, we saw the effects of slew rate on op-amp output with capacitor-at-input circuits, and AC signal rectifier circuits.

- Your notebook is perfect!

Prelab: 10/10

Diagrams: 8/9

Content: 12/12

Discussion: 9/9

- Very good job on this lab!

Your explanations of things show you have a good understanding.

+2 for Extreme in-depth discussion
+1 for Conclusion

[43/40]

amazing!

- Put labels on your scope plots. it's easier to read.

better fellin

SA
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5:20pm

Laboratory #7: Timers and Pulse Width Modulation: Part 1

Advisor: Dr. Gutschlag

Laboratory Objective: Develop techniques to control the various timer/counter options available on the Atmega128A-based Starter Kit to obtain Pulse Width Modulation signals commonly used to control various devices.

Equipment Used: Atmega 128 starter kit #18
 MSO 2014B oscilloscope EQ-3011

1. Although this board supports a PWM mode, for this section of the lab we will be using a Timer/counter that is not in this mode. We are to use the mode known as Clear Timer on Compare Match. The output of this will be visible on the OC0 pin, also known as PB4.

In order to achieve a signal frequency of 300 ± 15 Hz, we will have to take into account which prescaler we will use, and what value we want the counter to reset or clear to. In doing this, we are essentially dividing the system clock into the frequency that we want.

For a waveform generated in CTC mode, the waveform frequency is defined by the equation below:

$$f_{\text{out}} = \frac{f_{\text{oscillator}}}{2 \cdot N \cdot (1 + \text{OCR}_n)}$$

Equation 21-1: definition of CTC waveform frequency.

where N represents the prescale factor (1, 2, 32, 64, 128, 256, or 1024). For a frequency $f_{\text{out}} = 300$ Hz, we can choose a prescaler of 256, and after some trial and error, an OCRn value of 103 to garner the following:

$$16\text{MHz} \cdot \frac{1}{2 \cdot 256(1+103)} = f_{\text{out}} = 300.48 \text{ Hz}$$

Equation 21-2: calculation of waveform frequency.

A frequency of 300.48 Hz is well within the frequency range we are looking for. After this, it is simply a matter of configuring the board's register values for interrupts/timers to achieve what we need.

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A flowchart describing our procedure for configuring the

Laboratory #7: Timers and Pulse Width Modulation: Part 1
 Grant Aebel
 Brandon Lampert
 11/29/19

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~~there is a direct from~~

board to output a PWM signal that starts at a duty cycle of 1% and increases by 1% every 100ms is shown below:

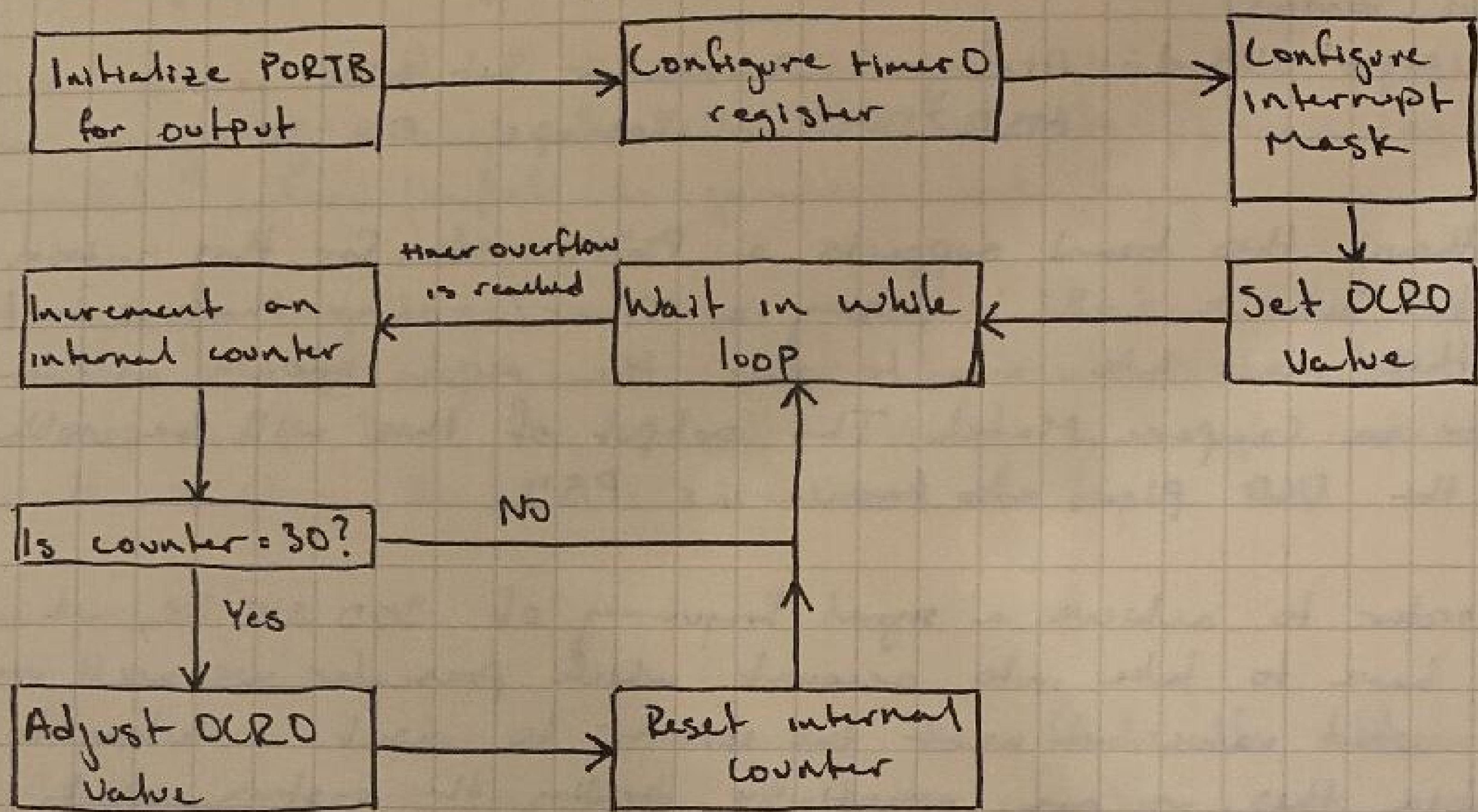


Figure 22-1: Flowchart describing the configuration of 800 Hz PWM signal with 1% duty cycle increments every 100 ms.

The difficult part of this will be the adjusting of the OCR0 value. We will want to initialize it to 204 to denote a 1% duty cycle to begin with. The purpose of the internal counter is to achieve the correct timing of 100ms when increasing the duty cycle.

Finally, we will need to reset OCR0 once we achieve a duty cycle of 99%, as written in the laboratory document. With this in mind, we will begin working on this. Our code for this program is as follows:

```

/* main.c program file: where the
   program begins */

#include "main.h"
int main(void)
{
    init_ports();
    interrupts();
    sei();

    while (1)
    {
    }
}
  
```

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3:07PM Figure 22-2: main.c program file containing initialization calls and an infinite while loop.

Laboratory #7: Timers and Pulse Width Modulation: Part 1

```

/* main.h header file: contains macro definitions,
   global variable declarations, and function
   prototypes.

#ifndef MAIN_H_
#define MAIN_H_
#define F_CPU 16000000UL

#include <util/delay.h>
#include <avr/io.h>
#include <stdio.h>
#include <avr/interrupt.h>

// Bit shifting macro
#define BV(bit) \
(1<< (bit))

#define top 206

// Global variables for handling duty cycle shifts
static uint8_t counter;
static uint8_t edge;

// Function prototypes
void init_ports(void);
void interrupts(void);

#endif

/* ports.c program file: contains function
   definition for init_ports().           */
#include "main.h"

void init_ports(void)
{
    DDRB = 0xFF; //set PORTB as an output
    PORTB = 0x00; //PORTB off
}
  
```

Figure 23-1: main.h header file and ports.c program file containing code logic for the PWM signal generation.

Before looking in the final interrupts file, I will explain the code thus far. Our main.c file simply calls the functions ~~init_ports()~~ defined in the other files. It then enables global interrupts with a call to sei(). After this, the program simply sits in an infinite while loop awaiting interrupt triggers.

The main.h header file contains macro definitions and declares global variables to be used inside the ISR. Finally, function prototypes are declared.

Finally, the ports.c program file contains the function definition for the init_ports function. This function simply configures the PORTB data direction and pullup resistors.

The final section of our code is shown and explained on the next page.

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Laboratory #7: Timers and Pulse Width Modulation: Part 1

Grant Abell
Brandon Laiptor
12/4/18

```
/* interrupts.c program file: contains definition
   of interrupts function as well as the timer ISR. */

#include "main.h"

void interrupts(void)
{
    counter = 0;
    edge = 0;
    TCCR0 = (1<<WGM01)|(1<<COM00)|(1<<CS02)|(1<<CS01);
    OCR0 = top-2;
    TIMSK = (1<<OCIE0)|(1<<TOIE0);
}

ISR(TIMER0_COMP_vect)
{
    if (edge)
    {
        if (OCR0 >= 204)
        {
            OCR0 = 0;
        }
        if(counter < 30)
        {
            OCR0 = top - OCR0;
            counter++;
        }
        else
        {
            OCR0 = top - OCR0 - 2;
            counter = 1;
        }
    }
    else
    {
        OCR0 = top - OCR0;
    }
    edge = !edge;
}
}
```

Figure 24-1: interrupt.c program file containing code for PWM generation logic.

This file is where the main logic of this program resides. We will first begin with the interrupts function. We start by initializing the counter variable and edge boolean to zero. After this, we set the timer control register. This register is configured to set three key waveform attributes:

- ① set mode to clear Timer on compare match, AKA CTC mode. WGM01
- ② Set OC0 to toggle on compare match. COM00
- ③ Set prescaler to 256 CS01:02

SA

12/4/18

3:46 PM All of these attributes are what we desire for our PWM signal. After this, we set the initial value for OCR0 at 204.

Laboratory #7: Timers and Pulse Width Modulation: Part 1

Finally, we set the timer interrupt mask to enable timer0 for CTC mode, and set the trigger to be an overflow.

OCIE0

T0IED

This interrupt function is called in the main program function, so all of these settings are set before waiting in the while loop.

Now for the ISR itself. Every time this ISR is entered, the edge boolean is toggled and the counter is incremented. When counter is under 30, OCRO is set to 206-OCRO to achieve an overall length of 206 no matter the duty cycle. When the counter is equal to 30, we adjust the duty cycle by roughly 1%, and reset the counter.

The reason we count to 30 to perform a change in the duty cycle is because it is needed in order to achieve the 100ms time between duty cycle adjustments.

Finally, we check the OCRO register for a value of 204, which is a duty cycle of 99% at which time we reset OCRO to zero and begin the process again.

When testing this program, we had to adjust some of the logic inside of our ISR but after that everything worked as intended.

Conclusion:

Because we have reached the end of the semester, we were forced to cut this lab short. However, despite this we did learn a lot about generating a PWM signal using only a simple 8-bit counter. This could be useful in the future if we need to drive motors and such.

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