Lab 5: 3 Stage Amplifier
EECS 311

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1 Introduction

To meet the requirements and specifications for this three stage amplifier, I opted to use, in order, CE and CC stages to increase input resistance/achieve high gain and lower output resistance respectively. I had thought that CB was good for increasing input resistance, but this did not seem to to be the case. My final circuit ended up looking like this:

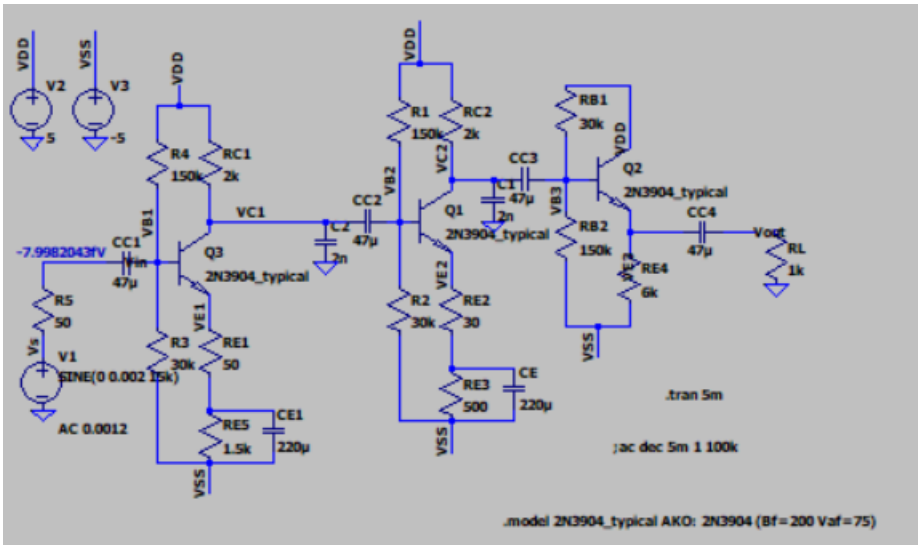

Figure 1: Circuit Schematic

Here we cascade the amplifiers as we learned them in lecture/lab, adding coupling capacitors between each to keep individual bias points and also loading capacitors to tweak the high and low cutoff frequencies independent of load. We also include degeneration on the CE amps for more stability. For all the coupling capacitors I just used 47 μF and for the degeneration capacitor 220 μF like in lab. f_H will be controlled by our loading capacitors between stages.

2 Common Collector: Low Output Impedance

We'd like out output resistance to be less than 100 Ω. From lecture, we have output impedance (factoring in an additional RB):

$$R_o = r_o||R_E||(r_e + \frac{R_{B1}||R_{B2}||R_{sig}}{\beta + 1})$$

$$r_o = V_A/I_C$$

$$r_e = V_T/I_E$$

As well as gain:

$$v_o/v_i = \frac{R_E||r_o||R_L}{r_e + R_E||r_o||R_L}$$

$$R_E, R_L \approx 10^3, r_o = V_A/I_C \approx 10^4, r_e = V_T/I_E \approx 10^1 \implies v_o/v_i \approx 1$$

We want $R_o \leq 100\Omega$, but we have some freedom with biasing. The gain will invariably sit around 1, so R_{out} is really our only constraint (aside from being power conscious and being careful with loading and voltage swing as described later). We will use this freedom to limit currents to keep our power down. The parameters we are using in our transistor model are $\beta = 200$, $V_A = 75$. We have not analyzed our CE amp, but we can make a liberal estimate of $R_{out,CE} = 5k\Omega$ to be safe and try to undershoot output resistance. Doing the biasing calculations:

Need op pt far enough away from VSS to get 0.8 V amplitude swing:

$$V_B = V_E + 0.7 = 10\frac{R_{B2}}{R_{B1} + R_{B2}}$$

$$100 = r_o||R_E||(r_e + \frac{R_{B1}||R_{B2}||5k}{201})$$

Try to maximize Rin for low loading

$$R_{in} = R_{B1}||R_{B2}||(\beta + 1)(r_e + (R_E||r_o||R_L))$$

Rather than trying to simultaneously solve all of these equations, I targeted high bias resistors for high input resistance, then used voltage division to set V_B to 3.3 volts to give us lots of room to swing. This worked out to $R_{B1} = 30k$, $R_{B2} = 150k$. Then I appropriately picked R_E get our output resistance low. I played with R_E and found that I could increase it all the way up to $6k\Omega$ and still have enough swing, achieving $R_o = 20$. Testing these values in this stage alone:

We see $R_o = 1m/50\mu = 20\Omega$, which is lower than we wanted and probably an overestimate since we deliberately guessed high for R_o of the CE stage. It draws around 1.25 mA bias current which is good. Also simulating reveals 23 $k\Omega$ input impedance not seen here, which should be plenty high. Also, it handles an input with full swing just fine, so we can call this stage good!

3 Common Emitter: High Gain

The primary consideration of our CE stage is the 600 V/V gain we'd like to achieve, as well as the 1.6 V peak to peak voltage swing we want. We will partition this gain between two CE stages. For both we can try and make them identical for ease of design, with gain about 25 to overshoot a

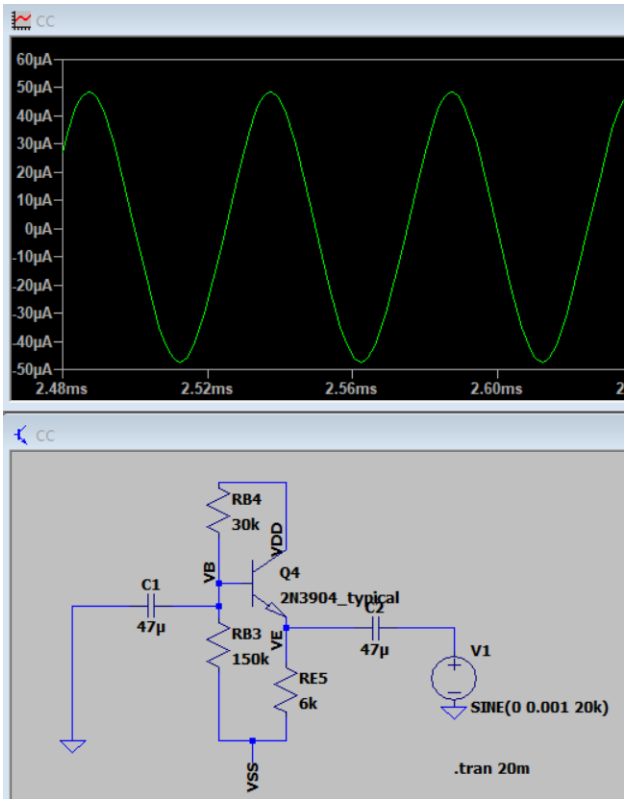

Figure 2: Measuring Rout For CC

bit. The gain of a CE amplifier (with degeneration) is as follows (taken from lab 4 notes where we designed a CE amp):

$$A_V = \frac{-g_m R_C}{1 + R_{E1}/r_\pi + g_m R_{E1}} = -25$$

We also need to respect:

$$V_E + V_{CE,sat} + 0.8 < V_C < V_{DD} - 0.8, V_{CE,sat} \approx 0.3V$$
$$\implies V_E + 1.1 = V_B + 0.4 < V_C < V_{DD} - 0.8$$

First lets set the bias resistors to give us some room on the output. Lets just set $V_B = 3.3$ V, fixing $R_{B1} = 150k\Omega$ just like before so we get $R_{B2} = 30k\Omega$. Now lets worry about gain, keeping in mind we want small R_C to prevent output resistance and thereby loading:

Let $R_C = 2k\Omega$

$$\frac{-g_m R_C}{1 + R_{E1}/r_\pi + g_m R_{E1}} \approx -R_C/R_{E1} = -25 \implies R_{E1} = 80\Omega$$

R_{E2} is just for biasing purposes, so if we want to drop a volt with around 1 mA of bias current we should make it like a $k\Omega$. Checking the bias in LT spice shows promising results. I then played around with it and the initial gain was around 17, which is probably because our approximation broke down for small values. I dropped R_{E1} a bit and found that 40 ohms was perfect. I set my degeneration capacitor to $220\mu F$ like in lab 4. Now testing gain and input impedance (output impedance is just R_C): Gain is great here. Checking the current from our source, the input

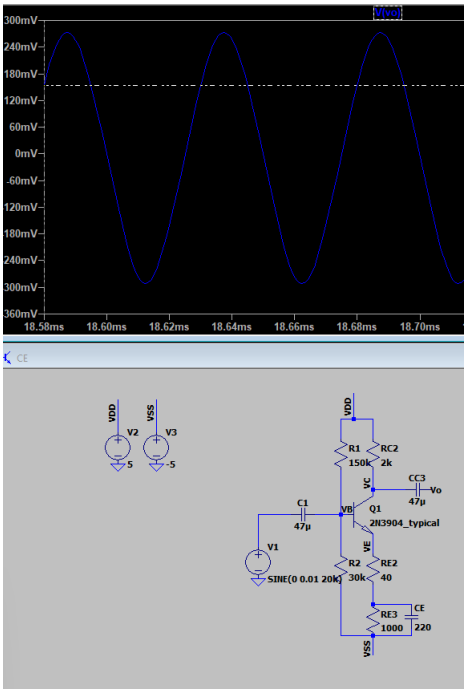

Figure 3: Measuring Gain For CE

resistance is $0.032/3.2\mu = 10k\Omega$. This is right on the spec, and should be enough to prevent loading. The output resistance measures out to 2 $k\Omega$. This is a little bigger than I'd like, but its hard to get good gain with much smaller R_C, and we overshot gain a bit to compensate. We'll run with it. Onto cutoff!

4 Setting Cutoff Frequencies

Since we know Rin and Rout of our stages, we can find the equivalent resistance to be the sum of the two in between two stages. Fix one of the capacitors to be 1 nF and use OCTC. We will only consider our loading caps since they are the main contributors to f_H, and f_L is more or less given by our 47 μF coupling capacitors and larger degeneration capacitors. For 30 kHz cutoff and a cap in between our CC and second CE stage, we have $30E3 = 1/(2/pi * C_1 * (23k + 2k) + 2/pi * C_2 * (10k + 2k))$. Fixing $C_1 = 0.1nF \implies C_2 = 0.23nF$. These did not set it sharply enough, so I increased both to 2 nF and it worked perfect, but chopped off some gain. This discrepancy was probably borne of neglecting other caps and the approximation not being perfect. To remedy this I put both emitter resistors down to 30 ohms and got my gain back.

5 Cascading and Final Results

My capacitors chopped a bit more off of my gain than I had anticipated, so I had to drop my emitter resistances a bit to compensate. This also lowered the input resistance of my first stage below spec, so I had to partition it and drop RE and thereby gain a bit more on the middle stage and increase the first one a bit. After making these small changes, everything worked great! Below is my final circuit and simulation results:

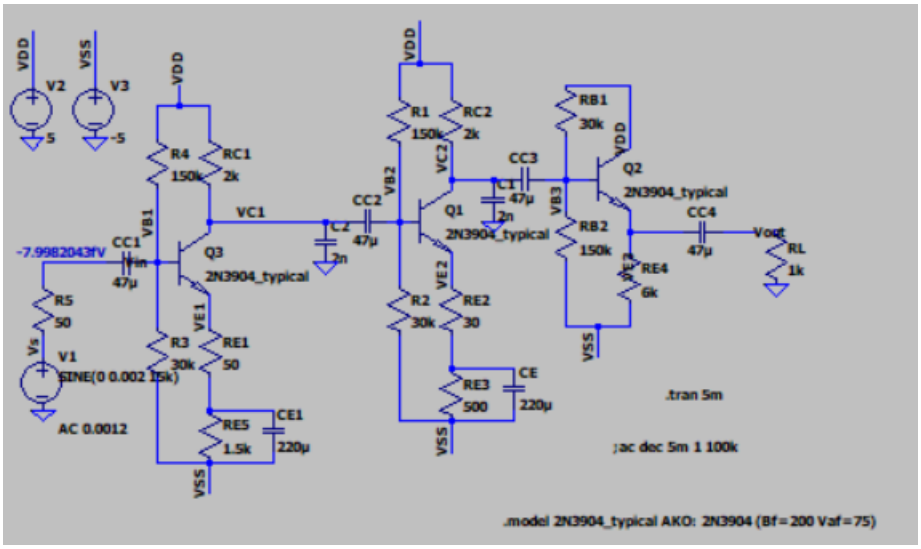

Figure 4: Circuit Schematic

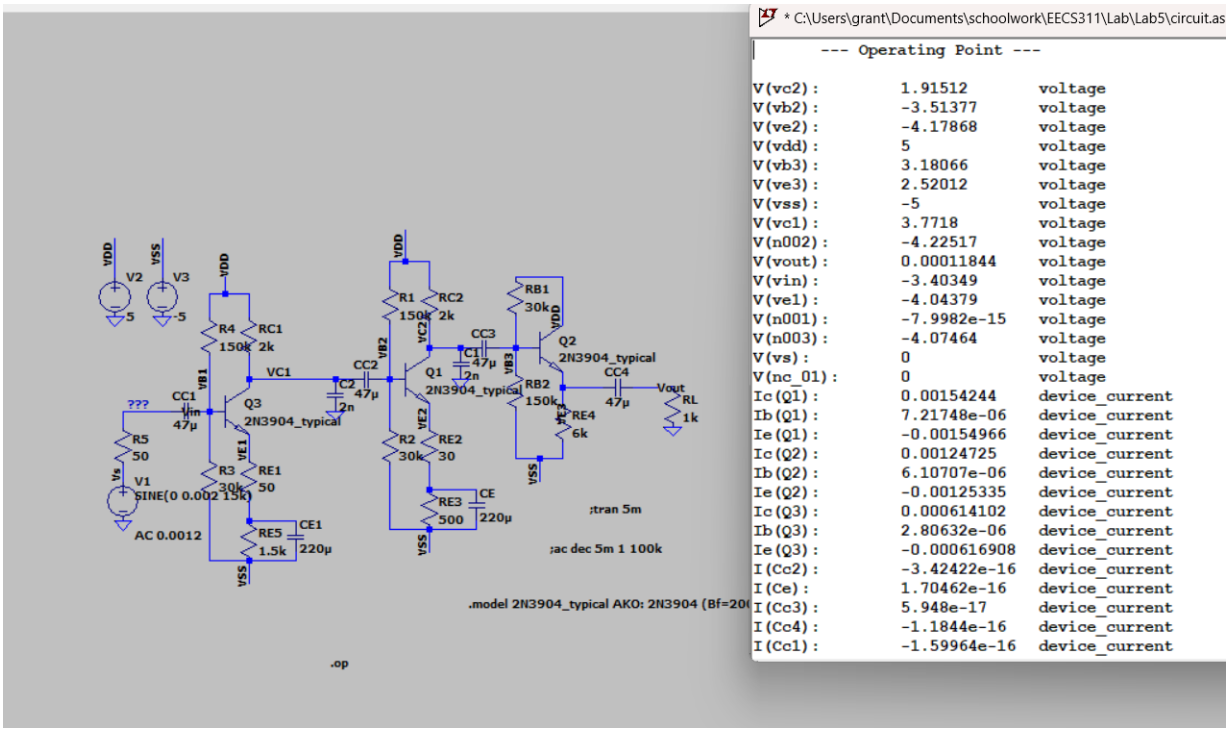

Figure 5: DC Operating Point First Part

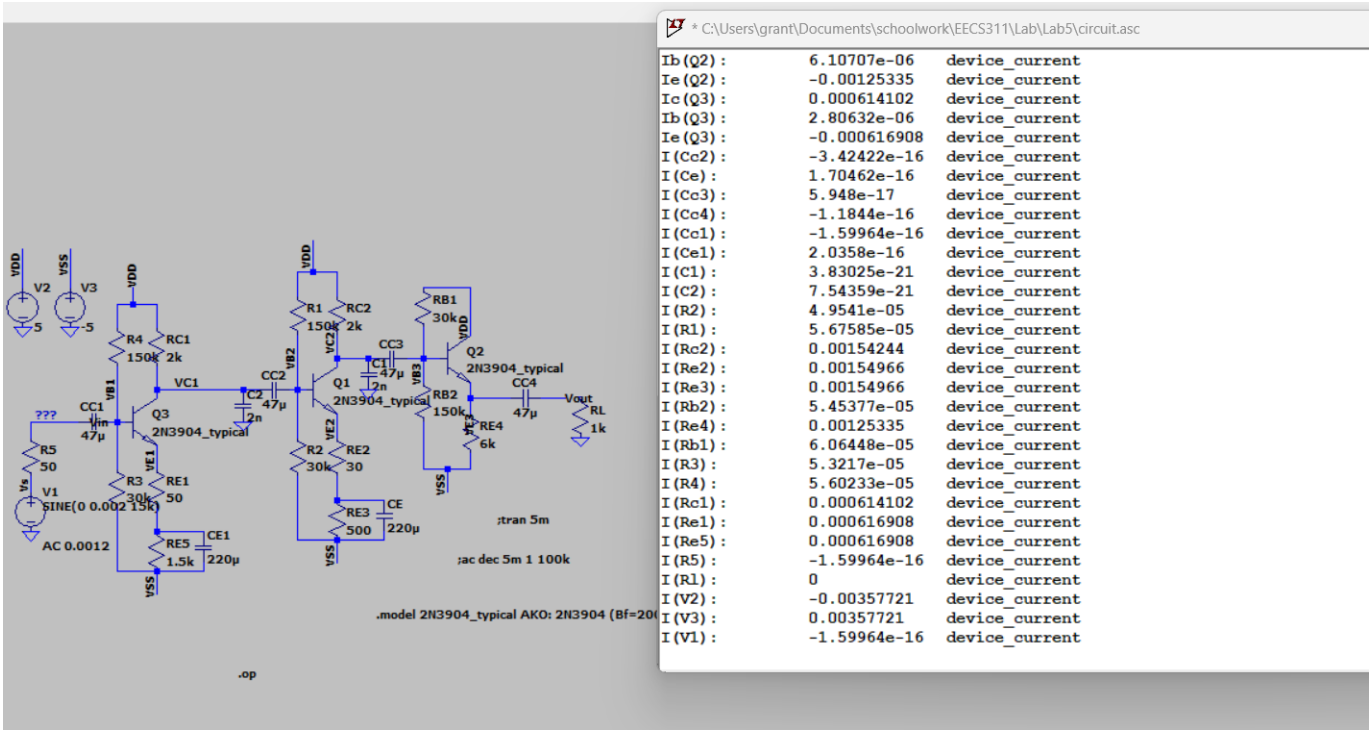

Figure 6: DC Operating Point Second Part: This gives us bias currents 0.6 mA, 1.56 mA, and 1.25 mA reading from left to right in staging order. These are all reasonable current values. It also shows the current through our power supply is 3.6 mA, which means we only use 36 mW of power!

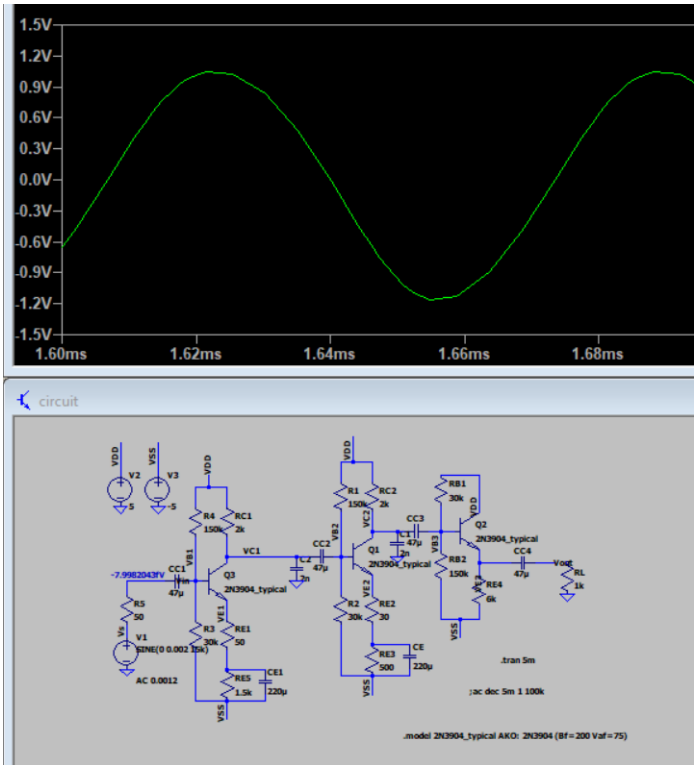

Figure 7: Max Swing: We see we are right at about 2 V of swing.

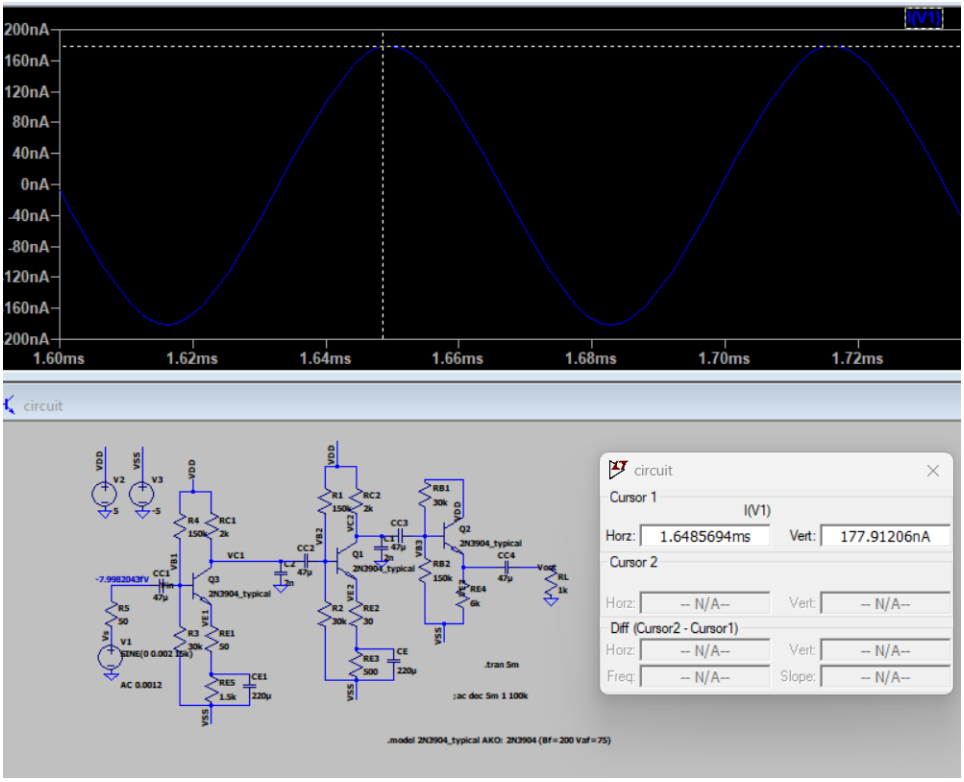

Figure 8: Current at Input Showing Rin: Here Rin is $0.002V/177nA = 11.32k\Omega$, right above the spec.

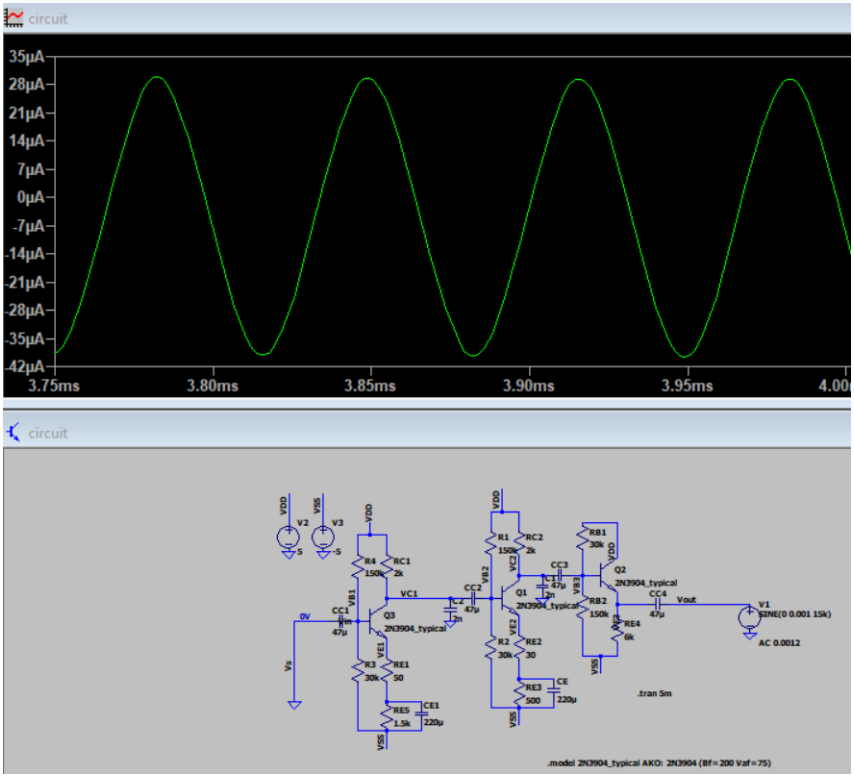

Figure 9: Current at Output Showing Rout: Here Rout is $0.001V/34\mu A = 29\Omega$, plenty low enough.

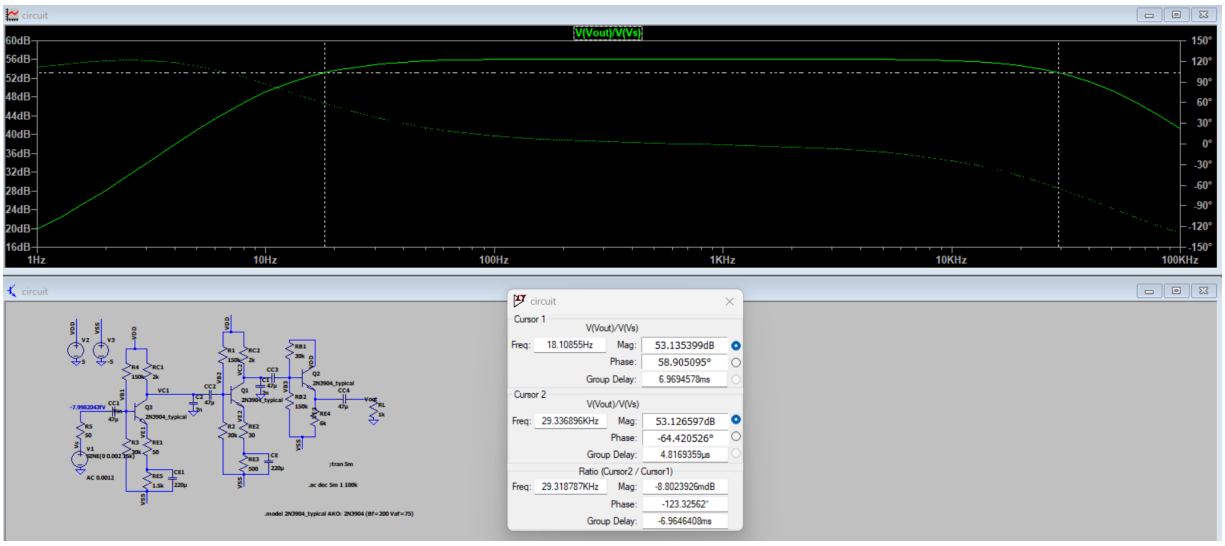

Figure 10: Frequency Response: We see our low cutoff is at about 18 Hz, and our high cutoff at 29 kHz. Our midband gain is at 56 dB which evaluates to $10^{56/20} = 631$. This satisfies every requirement!