ECE 557- Analog Test and Product Engineering

Winter Quarter 2016-2017

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Course Information

Meeting Times: Class: M, T, F 3rd hour in B105
Lab: W, 1st- 3rd hour in B105

Prerequisite: ECE351, ECE300

Prerequisite Skills: Analysis and Understanding of Fundamental Analog Circuits: (Diff Amps, Op-Amps, and Current Mirrors)
Basic Bench Testing Techniques (DC and AC Measurements)
FFTs
Sampling Theory

Required Text: Gordon Roberts, Friedrich Taenzler, and Mark Burns, An Introduction to Mixed-Signal IC Test and Measurement. Oxford University Press, 2012. or previous addition.

Required Hardware: 1 datastick for transferring your test program from your computer to the test computer.

Course Description

This course teaches the fundamental skills necessary to be a industrial integrated circuit test engineer or product engineer. In this course, you will learn (i) the economics associated with testing and how fabrication limitations lead to the need for testing each device, (ii) the instrumentation associated with industrial testing, (iii) how to turn a data sheet into a test plan (iv) industrial testing techniques, focused on minimizing test time, (v) the statistical analysis of the data and statistical process control, and (vi) the use of interface boards necessary to control device loading for different tests. Labs will give you hands-on experience programming an industrial grade automatic tester (ATE) and interpreting results from an actual chip.

General Policies

Homework: Homework assignments will be assigned weekly. Late homework will only be accepted with a penalty, unless prior arrangements have been made. Once solutions are posted, late homeworks cannot be accepted. I must be able to follow your work easily. Your grade is not just a function of knowing the material, but also in being able to communicate it clearly. Sketches, schematics, and plots must be neat and labeled clearly.

Laboratory: In prelabs, you will turn the datasheet and device interface board into a detailed test plan with all resistor values and relays clearly indicated. The first part of lab will be spent writting test code and the last part will be spent debugging test code on the tester. In the initial labs, we will write test code as a group led by the instructor to teach the fundamentals of the language and the program environment. Subsequent labs will be written individually or in pairs, depending on the number of students in the class. A brief lab memo describing your test procedure and resulting data will be expected for each lab.

Exams: There will be 2 quarterly exams and a final exam. The first exam will occur either 4th or 5th week and the 2nd exam will occur either 9th or 10th week. The exact dates will be decided as a group later in the quarter.

Make-up Exams / Homework: Make-up exams will only be given in the case of a properly excused absence. Late homework will not be graded.

Project: You will be responsible for a project to be completed during the last half of the quarter. This project will involve the design of the minimal set of tests necessary to complete the production testing for

a commercially available analog device. This set of tests will be derived from the devices's data sheet.

Grading Policy:		
	Homework:	10%
	Prelabs	5%
	Laboratory:	10%
	Exams:	40% (2 at 20% each)
	Final:	20%
	Project:	15%

Course Outline

A. Introduction to Test and Product Engineering (1 week - notes and 1.3)
   - A.1. Description of a Test and Product engineer (notes)
   - A.2. Fabrication process and typical fabrication errors (notes and 1.3)
   - A.3. Characterization versus production testing (1.3)

B. ATE instrumenation (1 week - 5.2, 5.3, 5.4, 6.2)
   - B.1. ATE test equipment (I/V sources, Kelvin connections, multimeters, PGAs, quantization noise, AWG's, digitizers, relay control lines)
   - B.2. High precision measurement techniques
   - B.3. Measurement accuracy versus test time

C. Typical DC tests (3 weeks - Chapt 3)
   - C.1. Methods presented for both op-amps requiring feedback to stabilize and instrumentation amps/PGAs not requiring feedback
   - C.2. Continuity
   - C.3. low precision tests: I_Q current and impedence
   - C.4. high precision tests: leakage current (I_B), open-loop gain, offset, PSRR, CMRR (included are the use of nulling amps and false-summing amplifiers)

D. Typical AC tests (3 weeks - Chapt 6, 7, and 8)
   - D.1. generation of multi-tone signals and sampling theory (6.3, 6.4, Chap 7)
   - D.2. Single Tone Tests: Absolute gain, gain tracking error, THD, (8.2)
   - D.3. Multi-tone tests: frequency response, phase response, Intermodular Distortion (Chapt 8)
   - D.4. Noise tests: crosstalk, idle channel noise, SFDR (Chapt 8)

E. Measurement accuracy and data analysis (2 weeks - Chapt 4 and 15)
   - E.1. Accuracy, repeatability, reproducibility (Chapt 4)
   - E.2. Test equipment calibration (4.2)
   - E.3. Variability distributions / statistical analysis (Chapt 15)
   - E.4. Guardbanding and impact on yield (Chapt 4 and Chapt 15)
   - E.5. Six sigma statistical process control: GRR, Cp, Cpk (Chapt 15)
   - E.6. Product engineering tools: Pareto charts, Scatter Charts, Control Charts (Chapt 15)

Topics Covered in Lab

A. Lab 1 - ATE demonstration: device-interface-board example and schematic, creating a program in the ETS system, analog resources, UserInit

B. Lab 2 - Continuity: Purpose of the continuity function, how to create a function, use of analog resources, datalogging, running test on ATE and receiving results. Prelab presents the creation of a test plan.

C. Lab 3 - I_Q: Let the students develop a new function on their own to obtain practice using the resources, datalogging, and using the ATE.

D. Lab 4 - V_{OS}: Test the offset voltage using the false-summing junction.

E. Lab 5 - Gol: Test open-loop gain using a nulling amp. Shows an alternative method to performing similar tests.

F. Lab 6 – CMRR and PSRR: Test common-mode rejection ration and power-supply rejection ratio using pattern-based testing. A pattern to modify the rails will be used to test both of these tests (and the offset test) to see another alternative test method.

G. Lab 7 - AC Test: Prelab: Students create a multi-tone signal in matlab to use in a gain- bandwidth test. Lab: Students use an AWG to drive multi-tone signal, digitize results, FFT results, and perform calculations on results. Students learn about ETS clocking scheme, mapping ATE clocking and storage capability to multi-tone signal, AWG, and digitizer.

H. Lab 8-10 - Projects: Students are given a new op-amp datasheet and asked to develop all the production-level DC tests and 1 AC test. Students must consider the time-accuracy trade-offs in their solutions. Students perform a repeatability study on the results, calculating GRR, to determine if their program measurement accuracy is sufficient. If not, the program must be modified to obtain full credit. Students then do a minor reproducibility study on two sites and two DIBs using 5 different chips. Students use line charts to see if the measurements for the same chips are tracking for different testing conditions. Students present results and discuss testing strategies to obtain the performance.

Lab Safety Policies

B 105 Lab

Solid sole footwear must be worn at all times while in the lab for any reason. Glove or finger footwear is not considered as closed toe or solid sole and thus is not permitted at anytime within the lab.

No food or drinks are permitted within 4 feet of any lab bench. Food and drinks are allowed to be placed on the front table. Anyone with drinks and/or food stuffs must remove or dis- pose of the material at the conclusion of their lab period(s). Food and/or drinks contained in backpacks and/or closed or sealed containers/packages may be kept on the floor during the lecture/lab period but ***MAY NOT*** be opened or consumed within 4 ft. of lab benches, food and drinks allowed on front table and tables in center of room.

No soldering, drilling, sawing, and/or non-circuit fabrication allowed. Electrical and wiring connections of components using "breadboards", wire wrap, and/or chip sockets are permit- ted.

At least two students must be present within the lab at anytime lab equipment is being used or testing is being conducted. Devices, circuits, systems under test may NOT be left unattended unless all test equipment has been turned off. Any material left unattended in the lab is done so at the individuals own risk. The ECE department is not responsible for material left unattended in the lab.

B 104 Lab

Solid sole footwear must be worn at all times while in the lab for any reason. Glove or finger footwear is not considered as closed toe or solid sole and thus is not permitted at anytime within the lab.

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No soldering, drilling, sawing, and/or non-circuit fabrication allowed. Electrical and wiring connections of components using "breadboards", wire wrap, and/or chip sockets are permit- ted.

Lab usage permitted testing available between 7:00 AM and 6:00 PM Monday through Friday. Lab usage at other times must be approved in writing by the ECE department chair or ECE department faculty member.

ESD Protection

This quarter, we will be using integrated circuits (i.c.'s), which can be destroyed by electrostatic discharge (ESD). Humans can create ESD, what you may recognize as a static electric shock, that is up to several thousand volts. This voltage may be discharged into the i.c. if you touch it without grounding your body first. There are ways to prevent ESD from destroying your i.c. chips. In this lab, ESD can destroy the i.c., the device-interface-board, AND the automatic tester. This could cause up to 1/2 million dollars in replacement costs!! Therefore, all ESD policies MUST be followed!

- Always carry your i.c. chips in an ESD guarded container. This will usually have ESD protection foam in an enclosed non-conducting case or be made of anti-static plastic. The parts room will have ESD cases which will be required for the purchase of i.c.'s. You should bring your ESD case to the parts room when you buy a new i.c. so that ESD does not destroy your device when you are walking from the parts room to the lab. Your i.c.'s should be placed into the case so that all pins are sticking into the anti-static foam.
- You MUST wear the grounding strap EVERY time you touch your chips, the device-interface-board, and/or the ATE. Make sure that the metal on the grounding strap touches your skin, or you are not grounded.
- An i.c. in a board and electronics on a device-interface-board are only safe if power and ground is supplied to the board. Integrated circuits have "pad protection circuitry" built into the pins, but they are only active if the chip is powered. Therefore, it is not wise to leave chips plugged into your boards and and leave the system powered off. Be sure to clean up the work area when you are done, removing all of your i.c.'s and placing them into you ESD container and replacing the device-interface-board back into it's ESD bag and in it's box. Place the diagnostic board back onto the ATE to protect it and the ATE from dust accumulation.
- If you have an ESD bag that contains chips or a board, note that the outside of the bag is conductive (this is how it performs the ESD protection). Placing a PC board or other electronics on top of the bag can short your electronics.