Homework 5: Due Tues, Oct 20

Problem 1 - DAC Specifications

A 3-bit resistive ladder DAC was fabricated and tested. The following table shows the DC characteristics from this DAC chip. .

$b_2b_1b_0$	Ideal V_O	Measured V_O
000	0.0V	-0.1V
001	0.15V	0.25
010	0.30	0.32
011	0.45	0.54
100	0.60	0.73
101	0.75	0.94
110	0.90	1.15
111	1.20	1.19

(a) Find the ideal V_{LSB}.

(b) Find the zero-scale error in LSBs. Given that this DAC is a resistive ladder DAC, what is the primary contributing factor to that causes this zero-scale error?

(c) Find the full-scale error in LSBs. What are the primary contributing factors that cause full-scale error?

(d) Find the DNL for each code in LBSs where the LSB is the ideal LSB. Which DNL should be datalogged?

(e) Find the INL for each code relative to the ideal line. Which INL should be datalogged?

(f) Find the slope and y-intercept for the end-point line representing the data.

(g) Find the INL for each code relative to an end-point line. Which INL should be datalogged?

(h) Which INL (part e or part g) could be calculated from the DNL? Explain your anwer.

(i) Find the slope and y-intercept of the best-fit line for this data.

(j) Find the INL for each code relative to the best-fit line. Which INL should be datalogged?

Problem 2 - DAC Datasheet

Use the LTC1450 datasheet to answer the following questions.

(a) Look at the schematic on page 1. What is the purpose of the output amp? Given the values of Vref and Vout at full scale, what should the gain factor of the op-amp be?

(b) Look at the "Parallel Interface" section on page 10 and the Truth Table/Timing Diagram on page 8. How should the digital control lines be set to continually load all binary combinations into the DAC. Hint: the input latches hold the next data while the DAC converts the data contained in the DAC latch. When data is loaded into the DAC latch, the conversion begins."Transparency" means the output of the latch sees the data on the input of the latch.

(c) Given your answer in part (b) and your understanding of this DAC, draw the schematic necessary to find the data necessary to calculate INL, DNL, Vos, and VFS.

(d) Look at page 9 where the datasheet describes the calculations for the DAC tests.

(i) Explain how they calculate the negative offset voltage given that the DAC has only 1 rail.

(ii) Given the Vos specification values, which code should be used to calculate the offset voltage error to ensure that a correct calculation would result?

(iii) Given that the DAC has one rail, which codes should be used for the end-point calculation for INL to ensure a good calculation reguardless of actual offset voltage measurement?

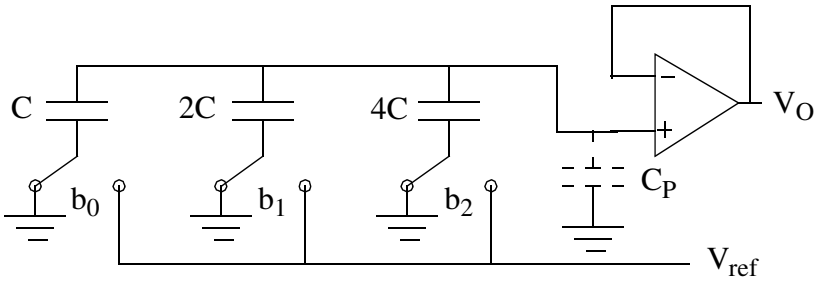
(iv) Explain how they calculated INL. How does their calculation correlate to the INL calculation described in class?

(d) Describe the test proceedure to find the data necessary to calculate INL, DNL, Vos, and VFS.

(e) How would each spec in part (d) be calculated for the datasheet limits given? Which order would each parameter have to be calculated?

Problem 3 - Binary Weighted Capacitive Array DAC

The following circuit shows a 3 bit version of the binary weighted capacitive array DAC shown in class.



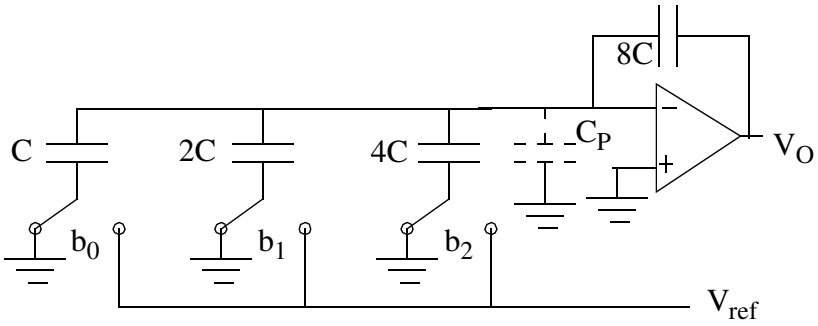
(a) One problem with this circuit is that it is sensitve to parasitic capacitances at the Vin+ node (shown as C_P). This parasitic capacitance is due to the FET gate capacitance at the input of the output amplifier and line capacitance.

(i) Find Vo for Din=001 without C_P.

(ii) Find Vo for Din=001 with C_P. Simplify so that you get an "error" term with C_P.

(b) What would you need to do to neglect this parasitic capacitance? What would be the impact on the circuit? (Consider the impact when you have 8 bits instead of 3).

(c) The following circuit shows another version of the binary weighted capacitive array DAC that is not sensitive to the parasitic capacitance. Show how this circuit works by finding V_O when Din=000, 001, and 010.



(d) Understanding how the circuit operates, how does this eliminate the problem with C_P?

(e) Would this version of the circuit allow for majority carrier testing? Explain your answer.