Homework 1: Due Thurs, Sept 10

Problem 1 - Introduction

(a) Describe how the design engineer, the test engineer, and the process engineer work together to produce a new integrated circuit.

(b) What is the advantage of getting your part to the market first? What is the disadvantage?

(c) Describe a process step that could produce a catastrophic error. Describe a process step that could produce process variation that may or may not allow the part to meet spec.

Problem 2 - TPE

(a) Describe the difference between characterization testing and production testing. Under what conditions in the lifetime of the design (e.g. design phase to obsolete phase) would you use one or the other?

(b) What in the datasheet tells you the part is production tested?

(c) Give 3 examples of how test accuracy and time are in trade-off.

(d) Give 2 examples of how test time can be decreased without effecting accuracy.

(e) The test instrument took 10 measurements of the supply current set in a low power mode with 10us between each measurement (see Table 1). These 10 measurements were averaged to produce the final *low power supply current* result. The test measurements are shown in the table below:

Table 1: Test Program Results for low power supply current (I_{DD}) in μA

1st	*2nd*	*3rd*	*4th*	*5th*	*6th*	*7th*	*8th*	*9th*	*10th*	I_{DD} *(avg)*
19.2	24.9	32.3	35.9	39.4	44.1	48	47.7	47.5	48.1	*38.7mV*

(i) Looking at the data, what would you expect the actual offset voltage to be approximately? Why does the calculated Vos result (*Vos avg*) not match your expectation? (Hint: if you're not certain, plot the data)

(ii) Name 2 methods you could employ to improve the results. Explain why each method will improve the results. Which do you think would be a more optimized solution?

(f) A product engineer performs a test-time-reduction on an existing part. (e.g. finds a way to reduce test time for a part). Should the new program be verified with only 1 chip? One test set-up (e.g. ATE, device-interface-board, etc.)? Explain your answer.

Problem 3 - Instrumentation

A voltmeter on an ATE has 5 intrument ranges (0.1V, 1V, 2V, 5V, 10V). The Vref for the 8 bit instrument ADC is 1.2V.

(a) What is the role of ranging in an instrument?

(b) What is the quantization noise seen in the ADC?

(c) I would like to use this instrument to measure the reference voltage on a DAC chip. This voltage can range between 2.75V and 2.85V. What instrument range should be used?

(d) Given your answer in part (c), find the PGA gain factor that will map the input appropriately to the instrument ADC. If the actual measurement was 2.842V,what value would come out of the PGA and go into the instrument ADC? Once the ADC adds the worst-case quantization noise and the computer scales the final value, find the worst case measurement that would be stored.

(e) If the instrument is placed in a high precision mode, the 2V DC offset can be removed from the measurement before going to the PGA. The instrument range will be automatically adjusted to the best range for the measurement without the 2V DC offset. What instrument range would be used?

(f) Given your answer in part (e), find the PGA gain factor that will map the input appropriately to the instrument ADC. What value would come out of the PGA and go into the instrument ADC? Once the ADC adds the quantization noise, and the computer scales the final value and adds the DC offset back in, find the worst case measurement that would be stored.

(g) What is the trade-off inherent in these two measurement techniques?