Homework 6: Due Tues, Oct 27

Problem 1 - DAC Datasheet and AC Tests

Use the AD7801 datasheet to answer the following questions.

(a) What kind of DAC structure is used in this part?

(b) What is the reference voltage for the default conditions?

(c) Find the V_{LSB} and full-scale voltage for the default conditions.

(d) Describe how data is loaded into this DAC. Specifically, what input starts a conversion?

(e) Draw a schematic that could be used to test the settling time using the default conditions.

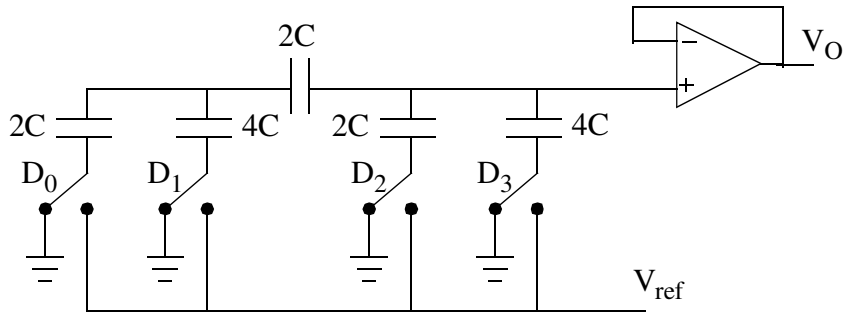
(f) What Din change should be used to obtain the worst case settling time? Draw a timing diagram of all digital inputs and Vo showing the expected result and how it would be measured.

(g) How would the schematic change for the glitch impluse and digital feedthrough specifications?

(h) What Din changes should be used to obtain the glitch impulse and digital feedthrough specifications? Draw a timing diagram of all digital inputs to force both of these test conditions (serially) and Vo showing the expected results and how they could be measured.

Problem 2 - Segmented DAC

The following circuit is common implementation of a segmented DAC .



(a) Find an expression for V_O for the following digital codes:

0001
0010
0100
0101
1000

(b) Given the structure, find an expression for V_{LSB}.

(c) Can this architecture be majority carrier tested? How do you know?

(d) What fabrication variation will result in nonideal behavior? Which testing specifications will catch each of these fabrication variations?

Problem 3 - Combination DAC

The following circuit is common implementation of a combination DAC. Note: the current steering DAC uses a thermometer code decoder to set the switches. A thermometer code decoder uses the following truth table, where a 1 changes the switch.

D5	D4	SA	SB	SC
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

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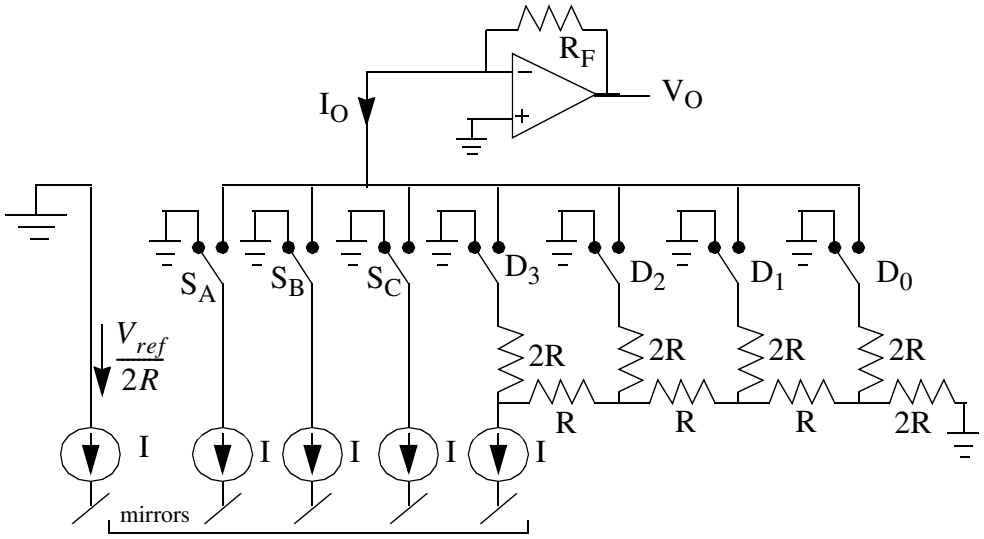

(a) Find an expression for I_O for the following digital codes:

00 0001

00 0010

01 0000 (these inputs show you how the combination works together)

01 0001

10 0000

10 0001

(b) Given the structure, find an expression for I_{OLSB} and the V_{OLSB}.

(c) Can this architecture be majority carrier tested? Explain your answer.

(d) The thermometer code for the MSBs minimized the switching transients, or digital glitches, in the summed current. Describe how this control scheme will help to minimize glitches.

(e) What fabrication variation will result in nonideal behavior? Which testing specifications will catch each of these fabrication variations?

(f) Name one advantage of this implementation over the Prob 2 implementation. Name one advantage of the Prob 2 implementation over this implementation.