Homework 4: Due Tues, Oct 13

Problem 1 -Measurement Variability

A GRR study was performed on the t_{prop} test for the MAX94_C. The follwing results were obtained.

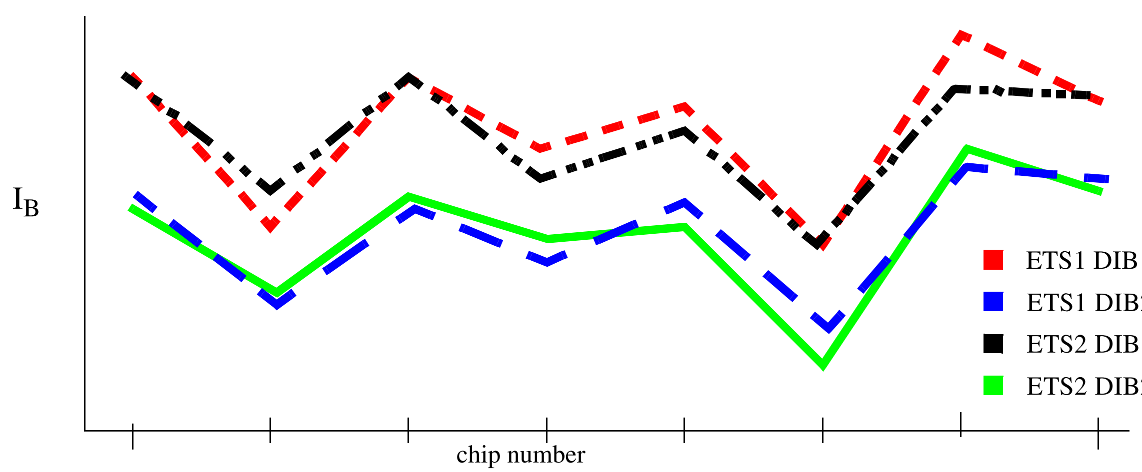
	t_{PD+}
σ_{repeat}	0.9ns
σ_{reprod}	4.3ns
σ_{fab}	32ns

(a) Find the GRR value due to repeatability. Should you move on to a reproducibility study with these numbers? Justfiy your answer.

(b) Find the GRR value due to both repeatability and reproducibilty. Is the program ready to move onto production?

(c) If the reproducibility did not pass GRR, name all of the DIB and instrument contributions that may cause reproducibility problems. Consider DIB components, measurement units, and sources.

(d) The following line chart was given for the reproducibility study using 8 different chips and 4 different test set-ups. What does this data indicate may be the reproducibility issue? How can this issue be rectified?.



(e) Using your method in (d), the standard deviation for repeatability and reproducibility have been improved to 2ns. Find the guardbanded test limits for t_{PD} that will maximize yield.

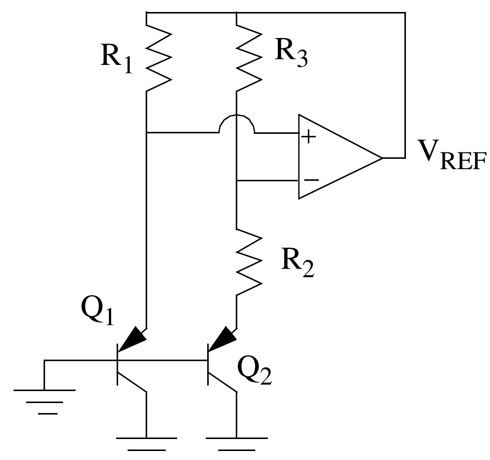
(f) A product engineer received the test program for the MAX94_C that had the following GRR results. Understanding the typical methods of testing each specification and the DIB schematic, what can the product engineer do to optimize <u>each test</u> in the program? BE SPECIFIC and explain why each answer will improve the program.

Table 1: Test Program Results

specification	Test Time	GRRrepeat	GRRreprod
Vos using linear sweep	30ms	5%	18%
I_b	5ms	6%	35%
V_{OH}	1ms	15%	32%

Problem 2 - V_{REF}.

A reference voltage is implemented using a bandgap reference as shown. Assume R_1=5.86kΩ, R_2=7.43kΩ, and R_3=73.8kΩ.



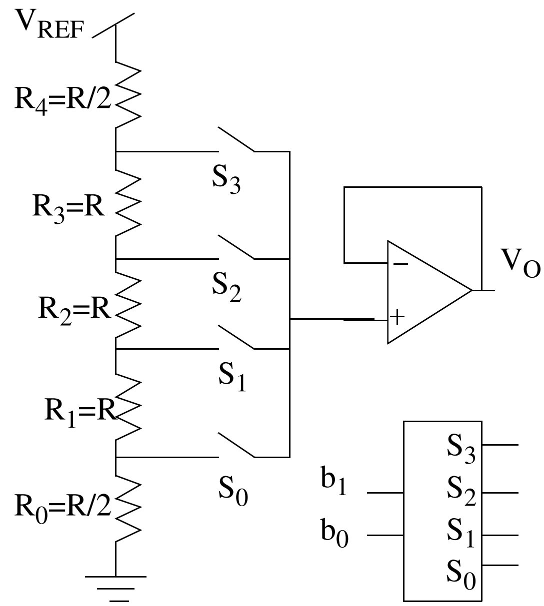
(a) Find V_{REF} at room temperature (T=300 degrees Kelvin). k/q=8.617X10^{-5} eV/K. Assume V_{EB}=V_D=0.65V at room temperature.

(b) Find V_{REF} if the temperature increases by 100 degrees K. Assume V_{EB} changes by -2mV/K.

(c) If R_3 is high by 15%, what is V_{REF} at room temperature?

(d) Redraw the schematic replacing R_3 with a 2 bit trim resistor. If R_3 can be off by +/- 20%, what value should you use for R_{LSB} and R_X so that the final R_3 will be approximately 73.8kΩ? Keep in mind that resistive trimming only increases the final resistance. Ignore tolerance in the R_{LSB} elements.

Problem 3 - R-Ladder DAC.



The following circuit shows another version of the 2-bit resistive divider DAC. Assume R=75kΩ. V_{REF} = 1.4V.

(a) Find the ideal tapped analog voltages for this converter. Draw the ideal transfer curve for the circuit.

(b) If Vref is 1% low, R_0 is high by 5%, R_1 is high by 8%, R_2 low by 2%, R_3 high by 6%, and R_4 high by 4%, find the tapped analog voltages for this converter. Sketch the resulting transfer curve. Be sure to show the ideal curve as well. Which individual code exhibits the worst-case error from the ideal?

(c) In addition to the resistor mismatches, the op-amp has an offset voltage of 3mV (e.g. V_{IP} - V_{IM} = 3mV). Find the tapped analog voltages including offset voltage in addition to resistor mismatch and Vref error. Sketch the resulting transfer curve. Be sure to show the ideal curve as well. Which code exhibits the worst-case error from the ideal?

(d) In addition to resistor mismatch and op-amp offset voltage, the gain of the op-amp is actually 1.15 instead of 1. Find the tapped analog voltages including all fabrication variation. Sketch the resulting transfer curve. Be sure to show the ideal curve as well. Which code exhibits the worse-case error from the ideal?

(e) If this DAC was used to create a voltage source inside the ATE, which factors would contribute to the resolution of the resource? How would the DAC structure have to be changed to improve this resolution? Which factors would contribute to the accuracy of the resource?