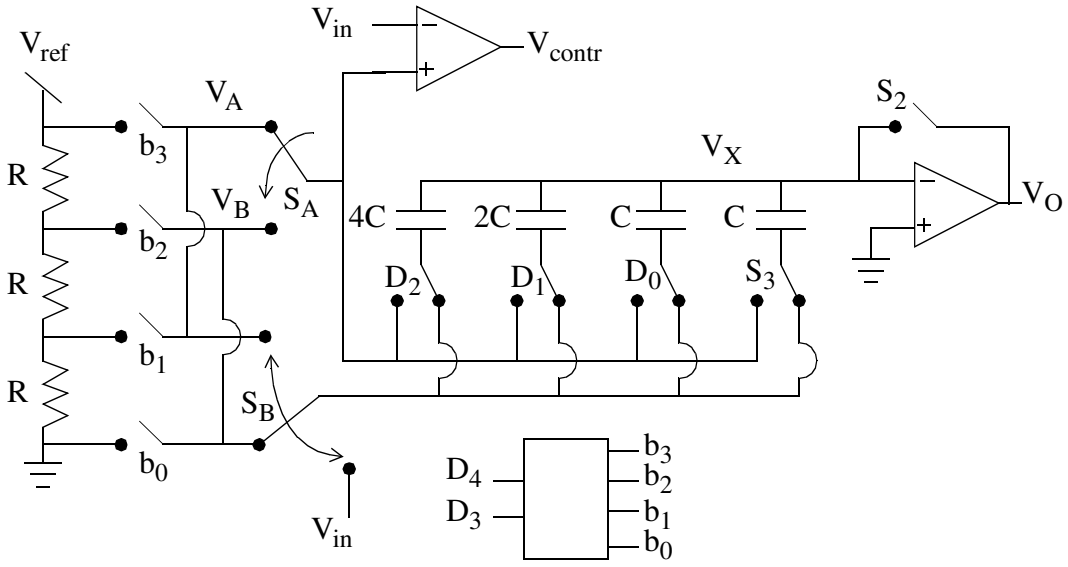
Homework 8: Practice Questions for the Final

Problem 1 - Hybrid ADC

The following circuit is the hybrind ADC shown in class.



(a) If Vref = 5V and Vin = 2.3V, walk through each stage of the conversion. What happens in each phase? Describe how each switch is changed and the resulting voltages at V_A, V_B, V_X, and V_O as each bit is tested.

(b) Fabrication variation in which elements will contribute to Vos error? Gain error? INL? DNL?

Problem 2 -Delta-Sigma Modulators

(a) How does a delta-sigma modulator achieve higher resolution that other converters?

(b) Explain how the loop shapes the noise without effecting the input signal.

(c) How is oversampling achieved in the delta-sigma DAC?

Use the AD1854 Datasheet to answer the next 2 questions.

Problem 3 -High Resolution delta-sigma DAC Clocking Scheme

(a) Look at the test conditions. If the input sample rate is 48kHz to generate a 1kHz signal, what percentage of codes are being tested in one cycle?

(b) If the data is being loaded serially, at what frequency should you run the vector editor?

(c) If the chip clock is 12.288MHz, what is being sampled 256 times?

(d) Sketch a waveform indicating how the 3 frequencies (chip clock, input signal, and sample rate) relate to one another. Every point does not need to be shown, but your diagram should clearly indicate what each clock really means.

(e) If a 61.44MHz master clock was used, what divide down ratios would be used to get the input clock and the vector editor frequency?

(f) If an FFT was to be executed on the digitized output, would you be able to use the same rate for the digitizer as the vector editor? Explain your answer. What digitizer rate could be used, given the master clock rate? How many measurements would be stored?

(g) Draw a schematic for the circuit showing the typical test conditions. Show digital resources for digital pins. If the pattern must be controlled by a vector editor, leave it as a DPU. If the resource is a continuous clock, list the clock frequency.

Problem 4 -High Resolution delta-sigma DAC Tests

(a) Look at the block diagram on the first page. Identify the components of the delta-sigma that we discussed in class. How does it map to the block diagram that I gave in class?

(b) The DAC is set up as discussed in problem 2. The output of the DAC is digitized and an FFT is performed on the result. Sketch the expected FFT showing dominant noise sources.

(c) Describe how the SNR specification without a message filter for the AD1854KRS would be calculated from the FFT.