Homework 3: Due Thurs, Sept 24

Problem 1 - Input Bias Current Test (Prob 4 from previous homework)

In this problem, you will design a test for the input bias current.

(a) How could you use the characterization curve for the input bias current as a function of common-mode voltage (see page 5) to determine which test conditions should be tested for this specification?

(b) Do you think you can measure the input bias current directly, or do you need to gain it up?

(c) Draw a schematic to test the input bias current. Be sure to label constant voltages with their values, changing values with variables, and show the instruments necessary for the test.

(d) Find value for Rb that would provide good production measurements. Valid QMS ranges include: 500mV, 1V, 5V, and 10V.

(e) If the resistor on the DIB has 5% tolerance, find the worst case resulting measurement. What voltage range should you use to perform the test?

(f) If the bias current was the typical value, would this be a good measurement or would it get lost in the quantization noise?

(g) List the steps necessary to perform this test.

(h) What calculations would be necessary to obtain the specifications in the units on the datasheet? Would you expect the current to be positive or negative? Explain your answer.

Problem 2 - Output Voltage Test

In this problem, I would like for you to combine the production level output voltage tests for normal operation (output-voltage swing) and shutdown mode (shutdown logic high and low).

(a) Could you use a single resource on the output to test both of the specifications? Explain your answer.

(b) Is the V_{OH}/V_{OL} output current condition relative to the chip or the instrument? What values should the instrument be set as for the V_{OH} test? For the V_{OL} test? Be sure to indicate the proper sign for the instrument.

(c) Why do you think this chip is tested for 2 output current conditions?

(d) Draw the schematic necessary to perform tests for all three specifications (V_{OH}, V_{OL}, and I_{LEAK}). Be sure to label your schematic clearly with all known voltages and/or currents and instruments.

(e) List the steps necessary to perform these tests.

(f) List any calculations that may be necessary and the datalog limits.

Problem 3 - Propagation Delay

In this problem, you will design a test for propagation delay. Since this specification is not indicated for the MAX941, please design this test for the MAX94_C.

(a) Draw the schematic necessary to perform this test.

(b) What threshold voltage should you give to the the input DPU going to the TMU for tprop? What threshold should you give the output DPU going to the TMU? Be sure and give your answer for both t_{PD+} and t_{DP-}.

(c) Sketch the input waveform that could be used to test both t_{PD+} and t_{DP-}. Clearly label the voltages and times necessary for this waveform. What should the period of this waveform be?

(d) Sketch the expected output that would result from this test. Clearly show how the prop delay would be calculated given these two graphs.

(e) In the graph for propagation delay vs input overdrive (page 4), notice how the prop delay changes with overdrive. Given your understanding of the comparator operation and overdrive, why does the data have this shape?

Problem 4 -Device Interface Board

Ove the last two homework assignments, you designed tests to determine 6 specifications for the MAX94x comparator (V_{OS}, I_b, V_{OH}, V_{OL}, I_{LEAK}, and t_{prop}).

Draw the schematic for the device-interface-board that could be used to test all of these production tests. Label each resource as an APU/SPU, QMS, or TMU. Be sure to use relays whenever necessary.