ECE531-01 – Digital Test and Product Engineering

Spring Quarter 2016

Instructor: Chris Miller

Office hours: MTRF/2,8 (or just stop by)

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Class room and time: MTF/6, 3:25pm-4:15pm, B105 in Moench Hall

Lab room and time: W/7-9, 1:35pm-4:15pm, B105/104 in Moench Hall

Required Text: Essentials Of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits. Michael L. Bushnell and Vishwani D. Agrawal, Springer, 2000, ISBN-10: 978-0-7923-7991-1.

Unofficial Text: Microchip PIC16F883 Data Sheet

General Policies

Homework: Late homework will be accepted with a grade reduction of 10% for each day that it is late. Once solutions are posted, late homeworks cannot be accepted. I must be able to follow your work easily. Your grade is not just a function of knowing the material, but also in being able to communicate it clearly. Sketches, schematics, and plots must be neat and labeled clearly

Lab reports: A brief memo describing your test procedure and resulting data will be expected for each lab. Late lab reports will be accepted with a grade reduction of 20% for each day that it is late.

Tests: There will be two exams near 5th and 10th week.

Grading Policy: Tentative grading policy, subject to change at instructor's discretion.

Homework:	20%
Labs, Project:	40%
Exams:	40%

Course Description

This course covers the theory and practice of fault analysis, test generation, and design for testability of digital systems. The topics to be covered include: circuit and system modeling; fault sources and models; fault simulation methods; test generation algorithms, including PODEM; testability measures; design-for testability techniques; memory testing. This is a lab course, which will make use of the Eagle Automatic Test Equipment to design and implement tests for an 8-bit microcontroller.

Tentative schedule (subject to change)

	Week	Description	Key Concepts
7-Mar	1	Introduction to TPE and Micrcontroller Architecture	TPE motivation, cost-accuracy tradeoff, basic testing equipment, microcontroller design and architecture, datasheets
14-Mar	2		micrcontroller architecture cont'd
21-Mar	3	Fault Modeling and Simulation	Common fault models, fault equivalency, and fault simulation
28-Mar	4		fault models cont'd
4-Apr		spring break	
11-Apr	5	Testability Analysis and ATPG	Testability measures, controllability, observability, automatic test-pattern generation (ATPG)
18-Apr	6		ATPG cont'd
25-Apr	7	Memory Testing	March tests, typical fault models for memory, RAM and ROM design
2-May	8		memory testing cont'd
9-May	9	Quiescent Current and Delay Tests	Fault detection and testing methods for IDDQ, path delay faults
16-May	10	Design for Testability	Design for testability (DFT) methods, scan design, cost of DFT

Tentative lab topics (topics or order may vary):

- Continuity test
- Programming test, I/O pin toggle test
- Test program via ATE
- Internal oscillator calibration
- Flash memory test
- RAM test
- Interrupt latency test
- Design project