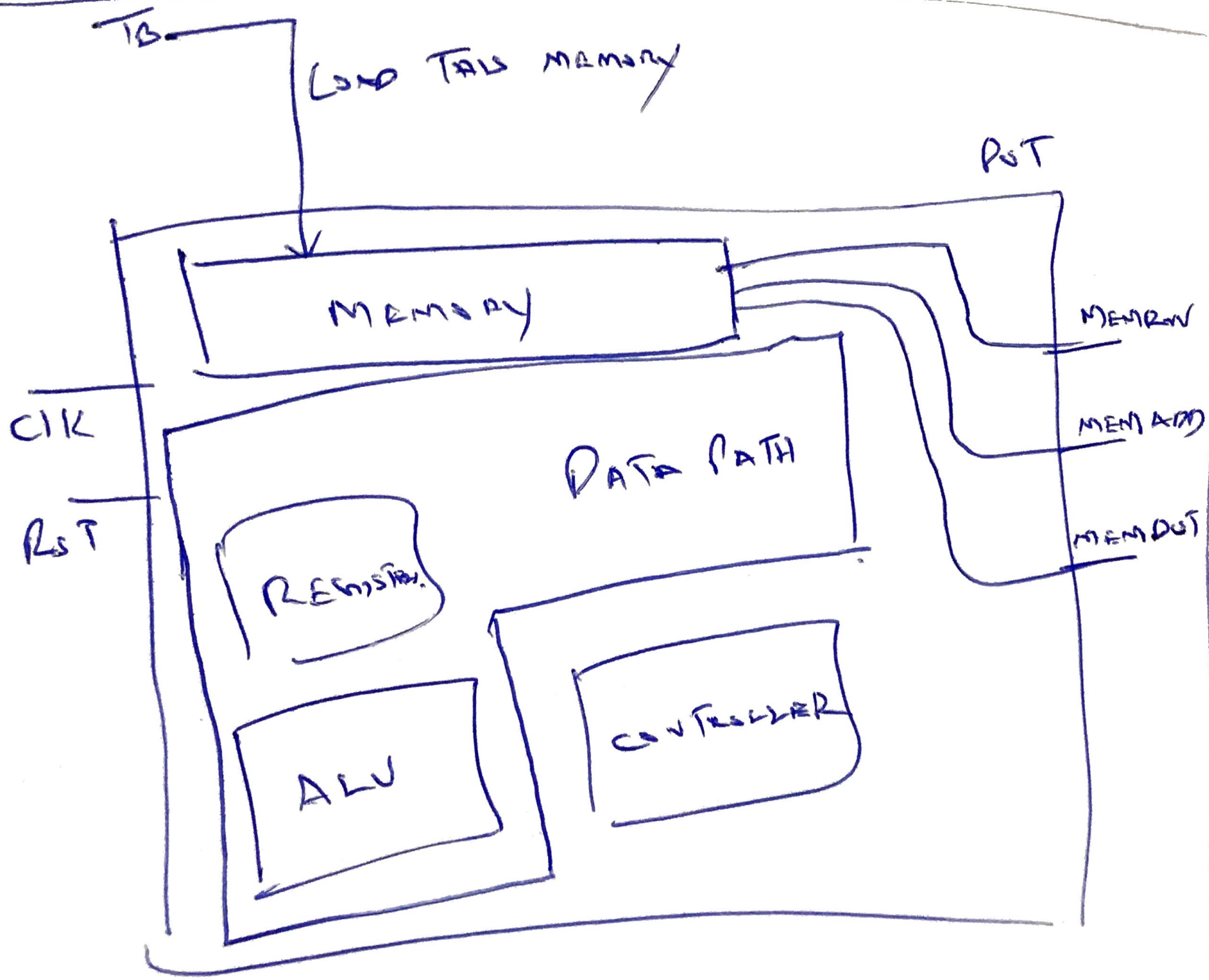
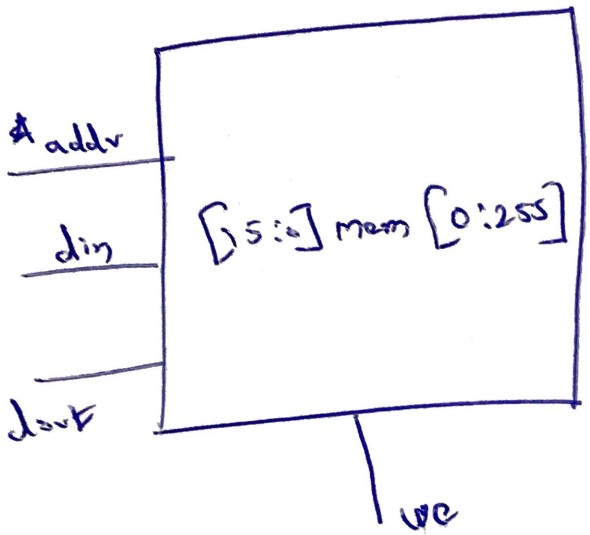

TB
LOAD TAU MEMORY
RST
MEMORY
MEMRW
MEMADD
MEMDOT
CLK
RST
DATA PATH
REGISTER
ALU
CONTROLLER

MEMORY MODULE



we — 1 ⇒ write

mem[addr] ≡ din

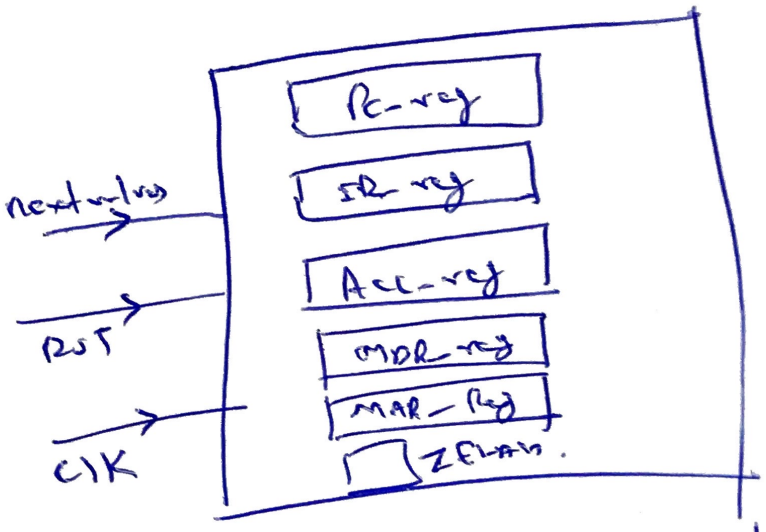
dout = 0

we — 0 ⇒ Read

default: dout ≡ mem[addr]

Load MEM IN TESTBENCH.

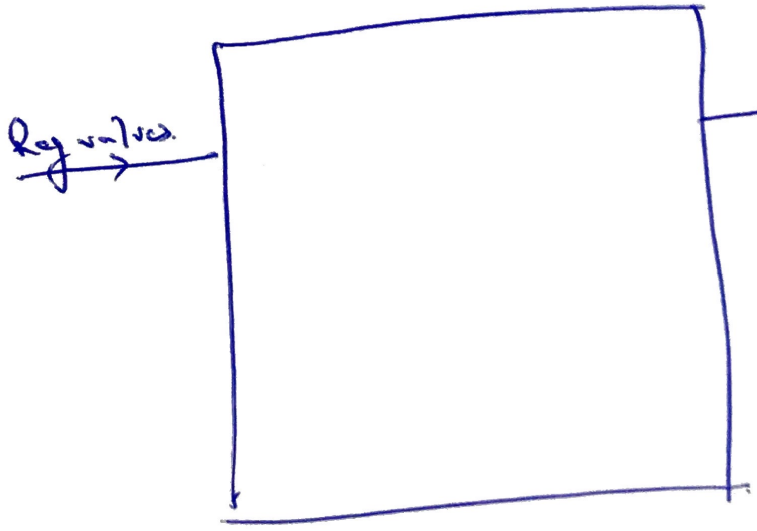
REGISTER MODULE



RST ⇒ set all to zero

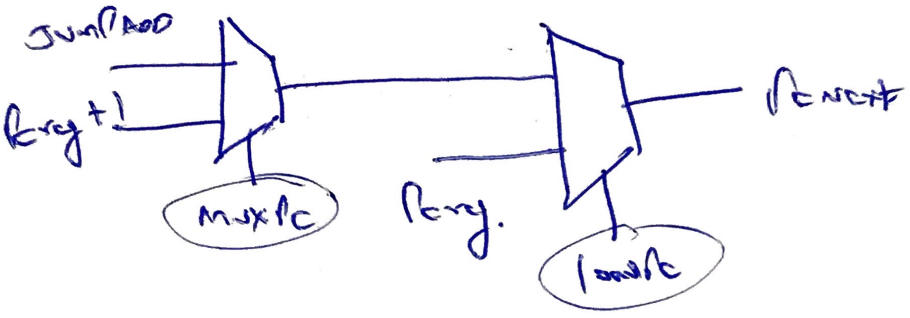
else ⇒ Reg ∈ next_value

DATAPATH

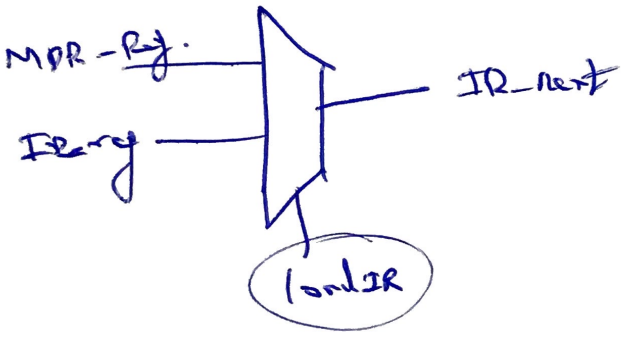


CONTROL ALL THE NEXT VALUES.

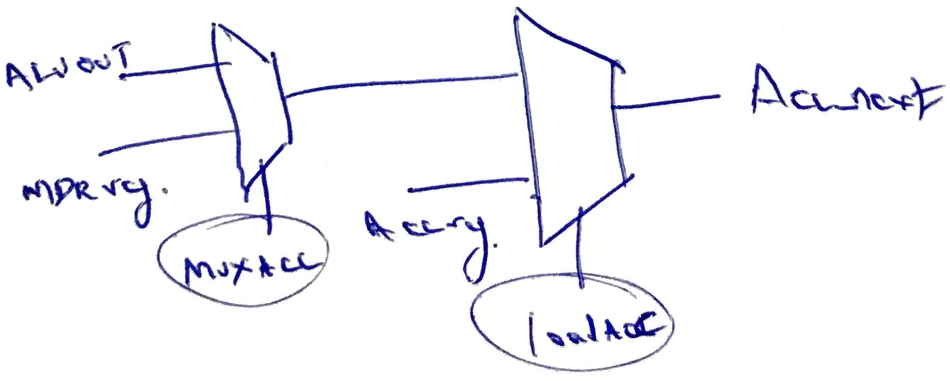
PC NEXT ⇒ COMBINATIONAL



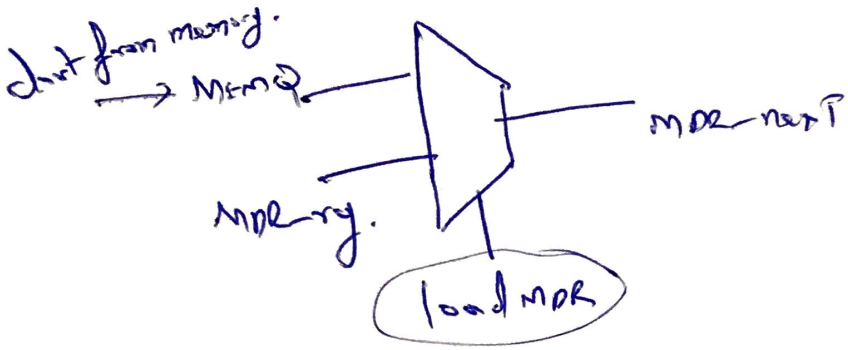
IR_NEXT



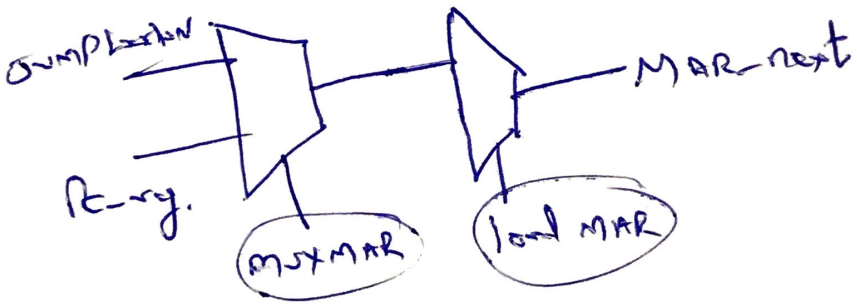
ACC_NEXT



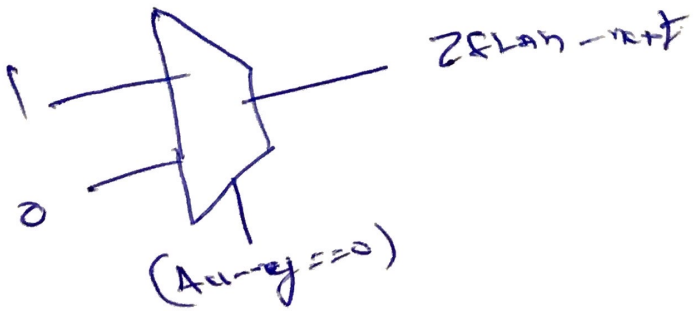
MDR_NEXT



MAR_NEXT



ZFLAG_NEXT



OPCODE = IR_ry[7:0]

MemAddr = MAR_ry.

MEMD = Acc_ry.

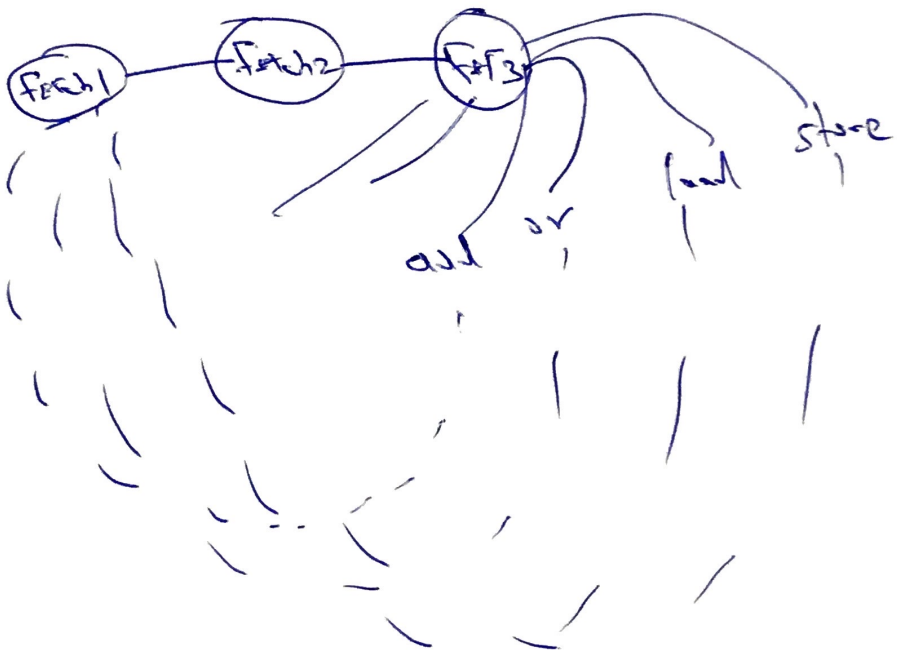
CONTROLLER

SEQ ⇒ Reset ⇒ my-state = fetch-1

else my-state = next-state.

SEQ ⇒ STATE CHANGES EVERY clock cycle.

INPUTS
- my-state
- opcode
- Zflg.



AT EVERY STATE ALL CONTROL signals need to be generated

COMBINATIONAL (if my-state = Fetch-1)

muxPC =
muxMAR =
muxAcc =
Load MAR =
Load PC =
Load Acc =
Load MAR =
Load IR
opALU =
MEMRW =