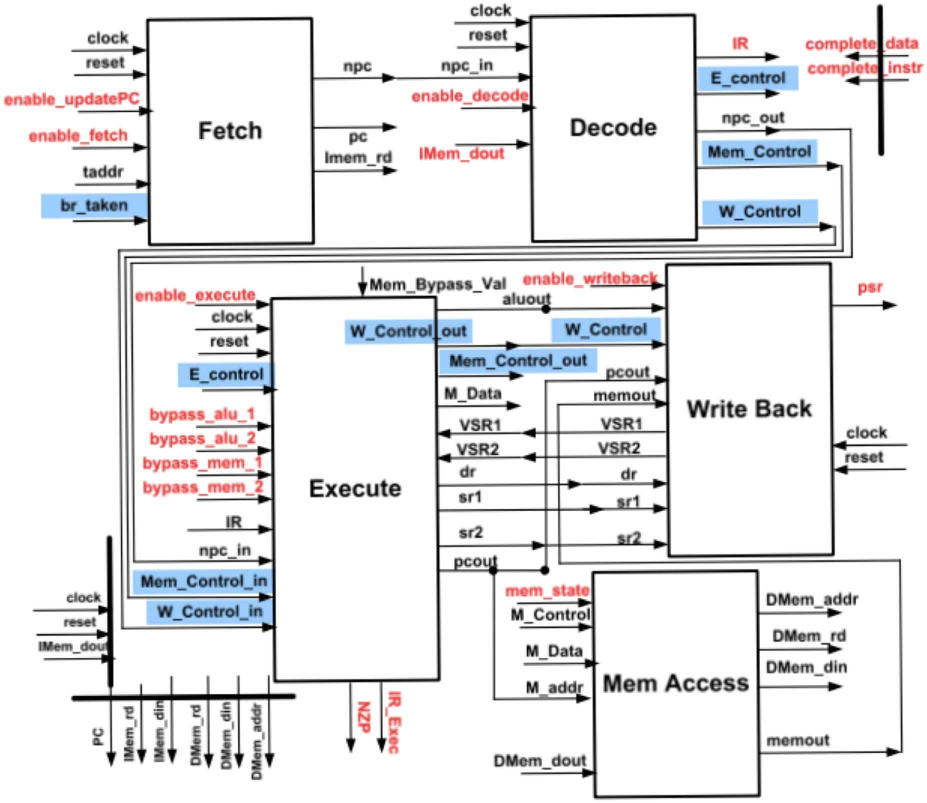
ECE 748

Advanced Verification with UVM

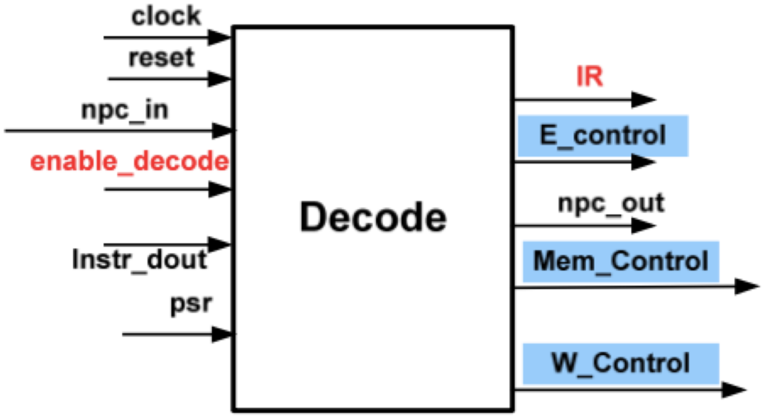
Class Projects – LC3

- Project 1
  - Create UVM interface package for decode input
  - Create a UVM interface package for decode output
- Project 2
  - Create a UVM environment and test bench for the decode block
- Project 3
  - Create a UVM environment and test bench for LC3 that includes the decode environment



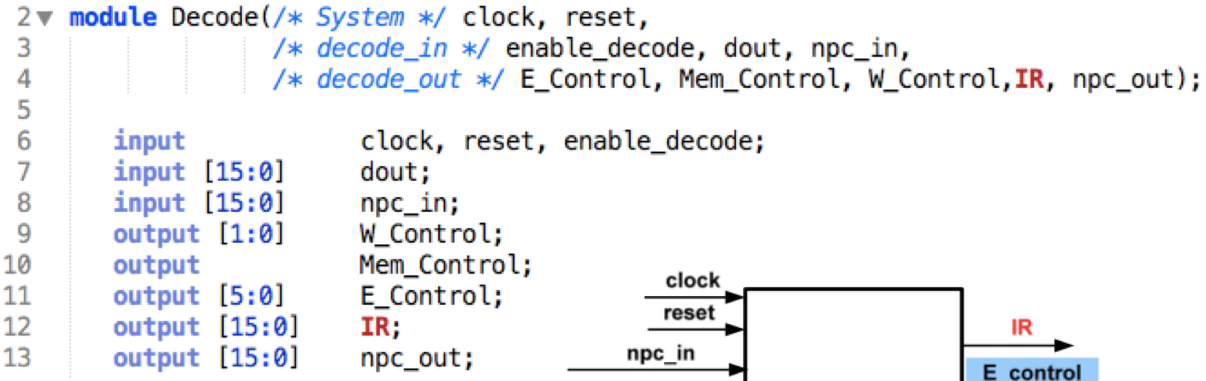
Project 1A – Decode_in Interface

- Project 1a – Three weeks
  - Create UVM interface package for decode input interface



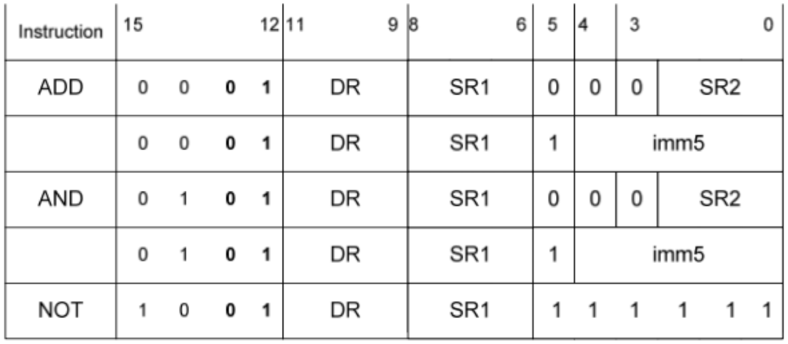
Project 1A – Decode_in Interface

- From the LC3 Specification you will need to identify
  - Signals used
  - Protocol signaling
  - Transaction variables
  - Type-definitions
  - Parameters
  - Functional coverage

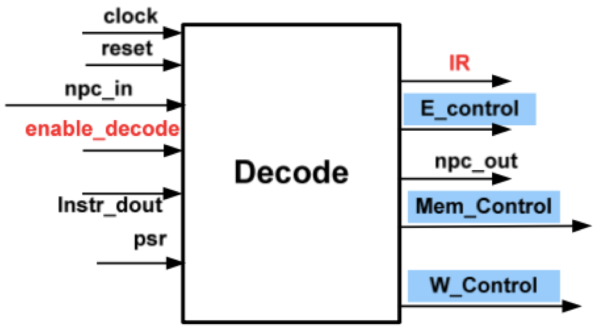


```
module Decode(/* System */ clock, reset,
              /* decode_in */ enable_decode, dout, npc_in,
              /* decode_out */ E_Control, Mem_Control, W_Control,IR, npc_out);

    input               clock, reset, enable_decode;
    input [15:0]        dout;
    input [15:0]        npc_in;
    output [1:0]        W_Control;
    output              Mem_Control;
    output [5:0]        E_Control;
    output [15:0]       IR;
    output [15:0]       npc_out;
```



Instruction	15			12	11 9	8 6	5	4	3			0
ADD	0	0	0	1	DR	SR1	0	0	0	SR2		
	0	0	0	1	DR	SR1	1	imm5				
AND	0	1	0	1	DR	SR1	0	0	0	SR2		
	0	1	0	1	DR	SR1	1	imm5				
NOT	1	0	0	1	DR	SR1	1	1	1	1	1	1



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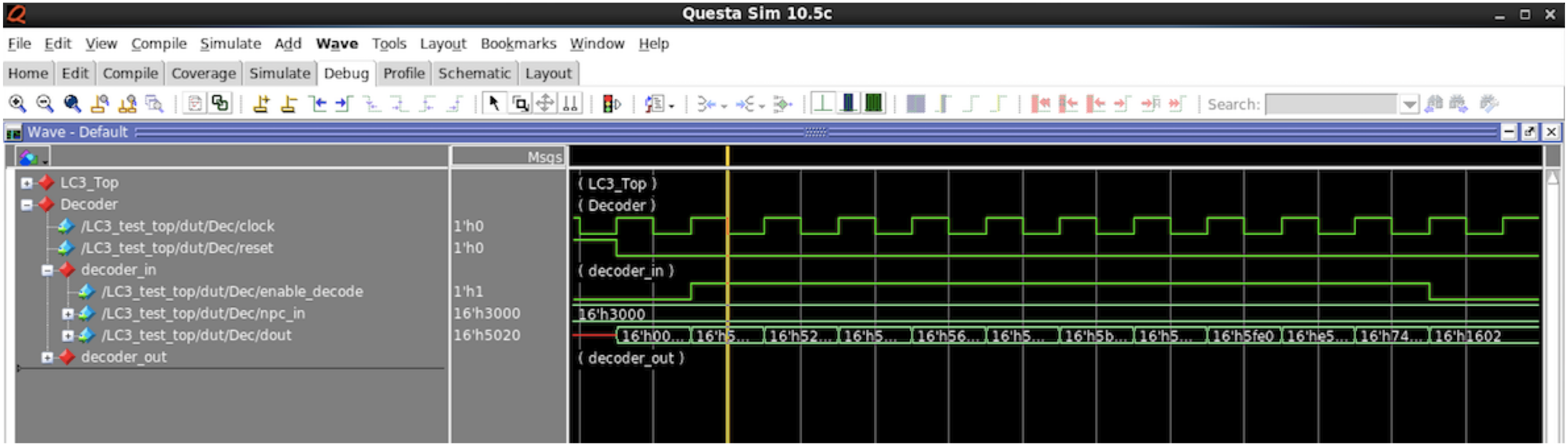
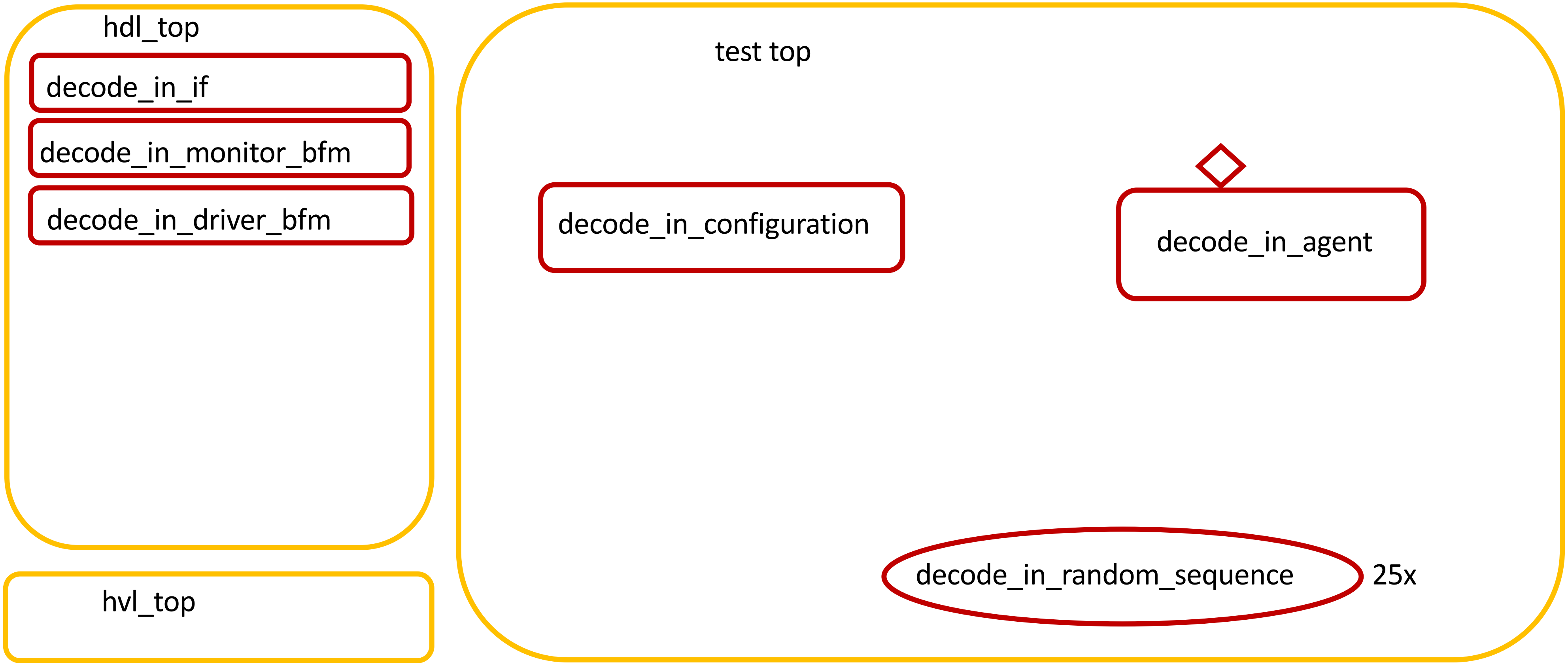
Project 1A – Decode_in waveforms


Questa Sim 10.5c
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Home Edit Compile Coverage Simulate Debug Profile Schematic Layout
Search:
Wave - Default
Msgs
(LC3_Top)
(Decoder)
(decoder_in)
16'h3000
16'h00... 16'h5... 16'h52... 16'h5... 16'h56... 16'h5... 16'h5b... 16'h5... 16'h5fe0 16'he5... 16'h74... 16'h1602
(decoder_out)

```
LC3_Top
Decoder
  /LC3_test_top/dut/Dec/clock            1'h0
  /LC3_test_top/dut/Dec/reset            1'h0
  decoder_in
    /LC3_test_top/dut/Dec/enable_decode  1'h1
    /LC3_test_top/dut/Dec/npc_in         16'h3000
    /LC3_test_top/dut/Dec/dout           16'h5020
  decoder_out
```

Decode Test Bench



hdl_top

decode_in_if

decode_in_monitor_bfm

decode_in_driver_bfm

hvl_top

test top

decode_in_configuration

decode_in_agent

decode_in_random_sequence

25x

Project 1A – Directory Structure

- Interface package location/name
  - verification_ip/interface_packages/decode_in_pkg
- Test package location/name
  - project_benches/decode/tb/tests/decode_test_pkg
- Top level modules location/name
  - project_benches/decode/tb/testbench/hdl_top.sv and hvl_top.sv
- Decode RTL location
  - No rtl necessary for this project
- Run simulation in
  - project_benches/decode/sim
- Run simulation command
  - make p1_debug – Use provided Makefile

Project 1A – Decode_in Instructions

- Lecture material and examples to be used as basis for completing decode_in interface package
- Instantiate decode_in agent, agent configuration, and decode random sequence in uvm_test extension named test_top
- Import decode_test_pkg in hvl_top module
- Run random sequence 25 times to generate 25 random transactions

Project 1A – Decode_in Requirements

- Stimulus flow as shown in lecture material
- Emulatable Analysis flow as shown in lecture material
- Covergroup(s) for coverage of ISA
- Transaction viewing in the wave window
- Package structure as shown in ECE745 lectures
- Agent and BFM hierarchy as shown in lectures
- Agent configuration containing BFM handles
- Agent configuration retrieves BFM handles using uvm_config_db
- Agent retrieves its configuration using uvm_config_db
- Stimulus flow including sequence item, sequence base and random sequence
- Transaction coverage within agent
- Convert2string method in transaction and configuration classes

Project 1A – Decode_in Submission

- Deposit all source in Moodle on due date
  - Parent directory name: <unityId>_p1a
    - Contains project_benches sub-directory
    - Contains verification_ip sub-directory
  - Be sure to remove compiled libraries from sim directory
    - Work directory
  - Compress the project into a single file for submission
    - File name: <unityId>_p1a.zip